The New Virtex FPGA Family

Much More Than Just a Million Gates...

Now, for the first time, you can create complete, highly complex, high-performance systems in a single programmable device. Using our new Virtex FPGAs and our new high-speed development tools, your creative ideas will reach full production more quickly, more easily, and less expensively than ever before. This is a revolution in logic design.

by Carlis Collins, Managing Editor of Corporate Communications, Xilinx, editor@xilinx.com

These are fast moving times; every day that you waste in unnecessary development, debugging, and manufacturing, is lost revenue and an invitation to your competitors. You have to manage your development time, and wisely leverage all of the available resources, to remain competitive; you have to think in extraordinary ways. That's the motivation behind our new Virtex family.

From the beginning, we coordinated our research and development, in both device and software technology, to create a complete, fully integrated solution for digital logic design. The Virtex solution is extraordinary and it's the wisest use of your time and resources for gaining a competitive advantage.

Virtex is Extraordinary

The Virtex architecture is a new concept in programmable logic technology, one that is both evolutionary and revolutionary. We built on our previous success and added many new features, ones that you requested, that allow you to create a true system on a single chip. These new ASIC-like features, combined with our new fast-compile software and lower pricing, now give you the best solution for all but the highest-volume applications. Designs that once required custom ASICs, can now go straight to production using Virtex FPGAs, saving you a lot of time, trouble, and expense.

There are four key features that make all of this possible:

Virtex Overview

The Virtex architecture includes many more features than can be adequately described in this article, that's why we included an abbreviated Virtex data sheet, starting on page 41. However, here's a review of the Virtex FPGA highlights:

- Nine Virtex devices, 50,000 to 1,000,000 system gates.
- 200MHz on-chip, 160MHz I/O performance.
- Delay-Locked Loop clocking.
- Flexible on-chip RAM.
- Support for 16 I/O standards.
- Core-friendly, fast, predictable routing.
- Very fast device programming.
- Dedicated carry logic for high-speed arithmetic.
- Dedicated multiplier support.
- Cascade chain for wide-input functions.
- Internal 3-state bussing.
- IEEE 1149.1 boundary-scan capability.
- 66-MHz/64-bit PCI compatible.
- Hot-swappable for Compact PCI.
- Die temperature sensing device, on-chip.
- 0.22µ, 5-layer metal process.
- 100% factory tested.
- Prices starting at less than $10 (50K gate XCV50, in high volumes).
- 1M and 300K gate devices available today.

1. Delay-Locked Loops (DLLs)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that eliminates skew by monitoring the input clock and the distributed clock, automatically adjusting a clock delay element, as described on page 50. This closed-loop system effectively eliminates clock-distribution delay, and can double your overall performance.

In addition, the DLL can provide four quadrature phases of the source clock, and can double the clock frequency, or divide it by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. The DLL can also operate as a clock mirror; by driving the output from a DLL off-chip and then back on again, it can thus be used to de-skew board-level clocks between multiple Virtex devices.

2. Enhanced Memory Architecture

The Virtex architecture supports three types of memory:

- **Block RAM** - Each Block SelectRAM+™ cell, as illustrated on page 47, is a fully synchronous dual-port 4096-bit RAM with independent data and control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion. Table 5 on page 47 shows the amount of Block SelectRAM+ memory that is available in each Virtex device; the smallest Virtex device (XCV50) has eight blocks and the largest device (XCV1000) has 32 blocks.
- **Distributed RAM** - Virtex function generators are implemented as 4-input look-up tables (LUTs) as shown on page 47. Each LUT can be used as a 16x1-bit synchronous RAM, and the two LUTs within a slice can be combined to create a 16x2-bit or 32x1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM. The LUT can also be used as a 16-bit shift register, ideal for capturing high-speed or burst-mode data.
- **200MHz Access to External Memory** - Using the built-in SSTL3 interface capability you can directly access external high-speed SDRAM, in addition to other types of RAM and ROM.

3. Simultaneous Interface to Multiple I/O Standards

The Virtex SelectI/O™ capability supports 16 different I/O standards, as shown on page 44. Each device includes eight separate I/O banks that can be independently configured for a different I/O standard allowing you to interface with up to eight different voltage and signal standards, simultaneously. All outputs are PCI compliant as well, giving you full 66MHz/64-bit PCI capability.

4. System Integration

To fill a million-gate device you will probably need to use predefined intellectual property, or cores. The Virtex architecture is designed to make this very easy because abundant routing resources of various lengths allow our LogiCORES™ to be placed anywhere, in any combination, with fast, predictable performance. Cores work the same way, every time, in Virtex designs, so you don't have to worry about "tweaking" or optimizing your final design.

Designed for Speed

The Virtex family was designed for speed, in all areas, including device development and programming. For example, with the Virtex family you can configure devices approximately 40 times faster than previous FPGAs. This means, for example, that you can completely configure our 100,000 gate XCV100 in less time than the vertical retrace on your video monitor. In addition, you can partially reprogram Virtex devices while they are operational. This opens a world of new possibilities such as Internet Reconfigurable Logic (IRL) as described on page 6.

Design development is faster as well, because our Alliance Series™ and Foundation Series™ tools are optimized for the Virtex architecture, which was optimized for use with High-level Description languages. This means that your compile times are significantly reduced, a real advantage for very large designs, helping you quickly evaluate design modifications.

Our development tools cover every aspect of design development from behavioral, schematic, and HDL design entry; through simulation, automatic design translation, and implementation; to the creation, downloading, and verification of your configuration bit stream. From top to bottom our software is easy to use and produces fast, accurate results.

Conclusion

FPGAs are no longer just for prototyping or low-volume logic replacement. Now you can benefit from the ease-of-use and time-to-market advantages of FPGAs for higher volume, system-on-a-chip applications. With the new Virtex family, your design possibilities are almost unlimited. Σ

For more information on Virtex see http://www.xilinx.com/products/virtex.htm.