Reed-Solomon Cores Excel in The Virtex Architecture

Integrated Silicon Systems has ported their Reed Solomon cores to the new Virtex architecture, which requires fewer CLBs while providing 28% better performance.

by David Mann, Marketing Communications, Integrated Silicon Systems, dmann@iss-dsp.com

Last year, Integrated Silicon Systems (ISS), a Xilinx AllianceCORE™ partner, began porting the DSP cores from their expansive semiconductor IP portfolio to the new Virtex FPGA technology. The Reed-Solomon Encoder and Decoder cores from ISS offer compact, high-performance FPGA implementations for applications from Digital Video Broadcasting (DVB) to data storage/retrieval systems (HDD, CD-ROM).

The ISS DVB Reed-Solomon cores, previously implemented in the XC4000 family, were developed using HDL techniques to make them portable across a range of technologies (such as ASIC and PLD) and processes (from 0.6µ to 0.18µ). The HDL source code originally produced by ISS for the Reed-Solomon cores had to be modified to use the new features of the Virtex device architecture. In particular, the SelectRAM™ previously used for memory elements was replaced with Block RAM. Many of the instantiated components in the Reed-Solomon core were automatically generated using LogiBLOX,™ the Xilinx component generation tool.

The Reed-Solomon decoder core is partitioned into modules as shown in **Figure 1**.

ISS DVB Reed-Solomon Decoder Block Diagram

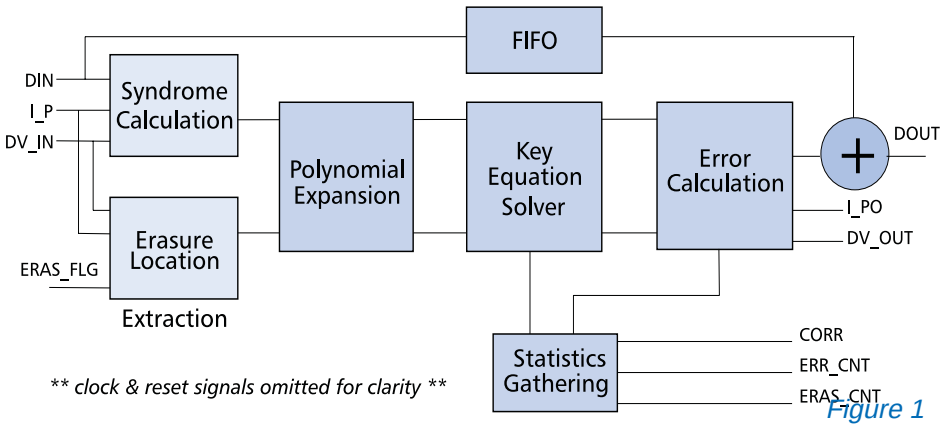

Figure 1

Targeted at the Xilinx XC4000XL series, a DVB-compliant R-S Encoder requires 105 CLBs. When retargeted at the Virtex architecture, the same core required 83 CLB slices (less than 42 Virtex CLBs). The performance of this core, as dictated by critical path timing constraints, was up from 55MHz (XC4005XL-3) and 72MHz (XC4005XL-1) to 82MHz (Virtex). So on a first pass in Virtex technology, performance was up 28%.

Conclusion

Trial implementations of the ISS-designed DVB Reed-Solomon AllianceCOREs in Virtex technology resulted in an immediate performance improvement of about 28%. Further work on optimization for the Virtex architecture is expected to provide even greater gains in performance.

About Integrated Silicon Systems

ISS is an established independent provider of reusable semiconductor IP for a wide range of applications. This silicon-proven IP is available to Xilinx FPGA designers, through the Xilinx AllianceCORE program, in the form of synthesizable or post-synthesis netlist cores. The package of deliverables for these AllianceCOREs includes design files (.xnf and constraint files) and test files (including testbenches and vectors).

For more information, e-mail info@iss-dsp.com