FlibGen, FlibTime, and ChipView – Power Tools for FPGA Design

No matter how awe-inspiring your latest FPGA design is, the next one will have to be even better. Three tools from Fliptronics can help you produce faster, denser designs in less time with less effort.

by Philip Freidin,
Fliptronics,
philip@fliptronics.com

Fliptronics has introduced three software power tools that can produce faster, more compact Xilinx FPGA designs. Using these tools, you can generate highly-optimized logic modules with predictable timing, and you can quickly view chip layout and critical timing paths.

Customized Modules (FlibGen)

The first tool, FlibGen, works in concert with Viewlogic ViewDraw to produce over 35,000 modules (Table 1) that have been optimized for speed and area. Using an intuitive module design menu invoked within ViewDraw (Figure 1), you can choose the function type, data width (from 2 to 32 bits) and other characteristics. FlibGen then creates a complete detailed schematic of the desired module, as well as a module symbol that can be placed in the design schematic.

FlibGen modules are particularly suited to high-performance designs, for the following reasons:

- Modules are consistently floorplanned, with two bits of datapath implemented in each CLB row. This consistency allows you to easily and efficiently tile the modules by attaching RLOC properties to the module symbols. The module schematic created by FlibGen contains a floorplanning diagram describing CLB usage, module shape, and bit assignments.
- Modules contain only the features and functions you specify.
- Because the modules are completely floor planned, they offer predictable timing.
- No special processing is required for functional simulation. Signals can be followed into and through modules.
- You can see exactly what's been built and, if desired, modify it.
- Modules are optimal. They are designed the same way a power user would design the function.

Predictable Timing (FlibTime)

The second tool, FlibTime, is an adjunct to FlibGen that reports detailed timing information for each module generated. Using FlibTime, you can:

- Create a detailed timing data sheet for any module (Figure 2). Included in this data is timing from any source pin to any destination pin, as well as timing starting and ending in internal registers.
- Quickly determine the differences in module timing among speed grades and Xilinx FPGA families.
- Make tradeoffs early in the design by determining the highest possible operating frequency for various key modules.

Suppose, for example, that a design depends on a 25-bit counter with parallel load running at 66MHz. The question, "What XC4000XL speed grade will support this requirement?" can be answered in a few seconds by specifying the module with FlibGen and analyzing its timing

Function Type	Types Available
Accumulators	23,808
Adders	2,232
Adder/subtractors	2,232
Comparators	310
Decrementors	1,116
Down counters	186
Incrementors	1,116
Incrementor/decrementors	1,116
Min/max Selectors	248
Multiplexers	868
Registers	62
Subtractors	2,232
Up counters	186
Up/down counters	186

Table 1

FlibGen can create over 35,000 building blocks optimized for high speed and low area.

(Continued)

with FlibTime. (The answer, by the way, is –09.) Similarly, you can determine the best performance obtainable from a given device type and speed grade, without generating any modules, or running place and route.

Viewing the Results (ChipView)

Once you have placed and routed your design, ChipView provides a quick way of viewing placement results and critical paths. Using PAR output files as its input, ChipView:

- Generates a 2-D plot of chip placement (Figure 3).
- Through shape and color coding, identifies function generators, flip-flops, single- and dual-port RAMs, ROMs, and carry logic.
- Shows the positions and names of all I/O pins, and indicates which are locked down.
- Identifies floorplanned and unfloorplanned portions of the design.

In addition to showing the layout, ChipView can also identify worst-case timing paths. It post-processes the output of the TRCE program, lists timing delays in a tree format, and graphically depicts timing paths on the chip layout diagram. By examining worst-case paths visually, you can quickly determine the portions of a design that need further floorplanning. One such path is shown in Figure 3; It starts at the green circle (R11C5), extends up column 5 and ends at the red circle (R3C1). ChipView works with both schematic- and HDL-based design flows.

Summary

FlibGen, FlibTime, and ChipView provide you with a means of generating highly-optimized building blocks with predictable timing, and of quickly appraising FPGA layout and timing-critical paths. All three programs include online context-sensitive help, run under Windows NT 4.0, and support the Xilinx XC4000E, XC4000XL, XC4000XLA, Spartan, andSpartanXL families. These programs can be purchased separately or together; the price of each is $500. Σ

For more information, call Fliptronics at (408) 737-0295, or visit the Fliptronics website at http://www.fliptronics.com.

FlibGen Menu for Building Adders

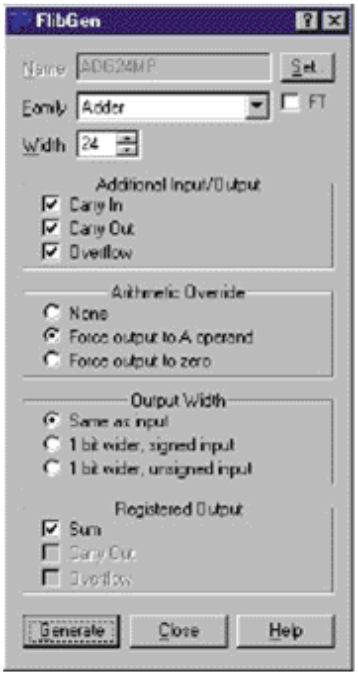

Figure 1

FlibTime Timing Report Window for 24-bit Adder, in XC4000E, -1 Speed Grade

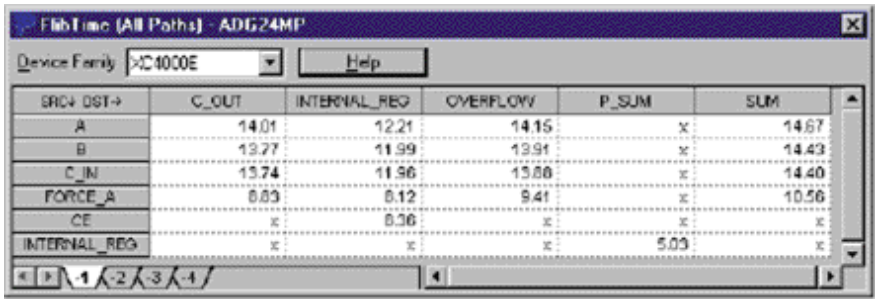

Figure 2

ChipView Displaying a 16 Bit RISC CPU

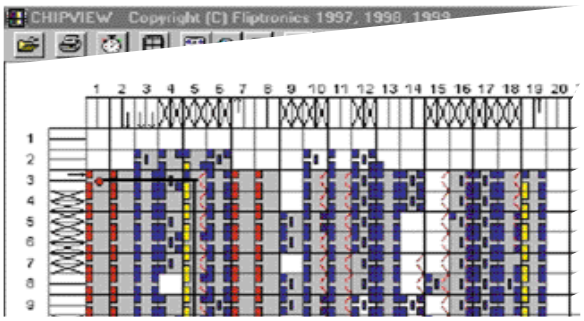

Figure 3