New WebPACK Integrated Synthesis Environment (ISE)

Free, comprehensive design environment for CPLDs available over the Web.

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Xilinx WebPACK™, the popular Internet-enabled Project Navigator-based CPLD design environment just got better. The new WebPACK ISE release extends your productivity and performance capabilities even further with an easier to use design interface and greater design control.

The free WebPACK tool modules include:

- Design Entry Module - Provides VHDL, Verilog, and ABEL HDL support as well as schematic capture design entry which is new to WebPACK with ISE.
- Fitter - Fitters for either the XC9500 or CoolRunner families.
- Programming - For device programming control.

In addition, the recently introduced BackPACK modules have been augmented for the WebPACK ISE release.

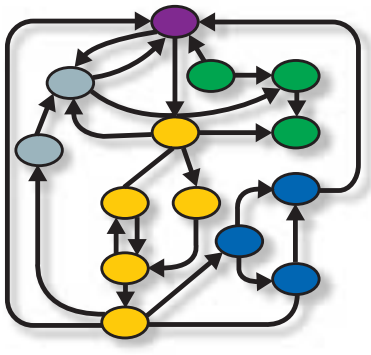
New BackPACK Capabilities

Xilinx introduced the concept of a WebPACK "BackPACK," or productivity enhancement module in April 2000. BackPACK modules are not required for CPLD design completion, but are useful in extending design flow functionality. The first BackPACK modules introduced were ChipViewer and Model Technology's ModelSim XE Starter Edition. WebPACK ISE includes updates to these two tools as well as offering schematic design libraries for use with schematic capture.

WebPACK ISE also introduces two new tools developed by Visual Software Solutions (VSS) for inclusion in Xilinx software: StateCad (www.statecad.com) and HDL Bencher (www.testbench.com).

StateCad

StateCad automates the state machine design process. It automatically looks for common design problems such as stuck-at-state, conflicting state assignment, and inde-



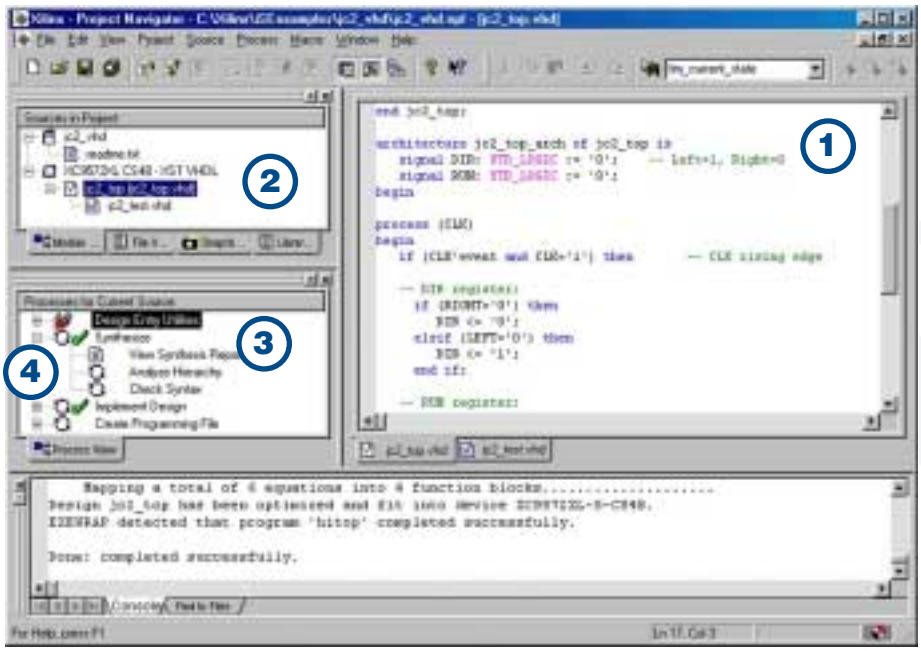
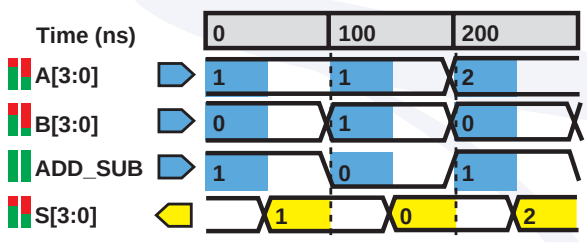


Figure 1 - Project Navigator design environment.

terminate conditions. Its automated error analysis insures that designs are logically consistent which reduces the simulation requirements and improves product reliability. StateCAD automatically produces HDL code for synthesis and simulation that eliminates manual translation efforts and coding errors. It simplifies complex state machine design allowing you to achieve peak hardware performance with less effort than before.

HDL Bencher

HDL Bencher is an automatic test bench generator allowing test benches to be created in minutes. A VHDL or Verilog design



file can be imported to HDL Bencher either manually or through the Project Navigator design environment. HDL Bencher analyzes the design I/O and creates a default stimulus waveform for each. The waveform may be easily modified to simulate the expected design performance. Final waveforms may be exported as a VHDL or Verilog file for use in many popular EDA simulators. The automatic nature of HDL Bencher allows test benches to be automatically updated as your design changes, thus eliminating stale test cases. Use of HDL Bencher ensures that your complex hardware designs are more robust and up-to-date than if coded manually all in a fraction of the time.

Easier to Use Design Interface

The upgraded Project Navigator design environment, shown in Figure 1, has a new look and feel. The basic Project Navigator structure is maintained and includes significant new flexibility enhancements, allowing you to fully customize the design environment.

Other ease of use improvements (as shown in Figure 1) include:

1 - HDL editor integration.

2 - Synthesis flow switching.

3 - Double-click design process property and options access.

4 - Augmented design processes grouped into four basic areas allowing as much or as little interaction with the design flow as you want.

Greater Control

In addition to the improved design environment and new tool integration the CPLD tools are augmented with the following new features and improvements:

- XC9500XV output banking support automatically assigns device outputs based on the desired output voltage standard.
- Improved design analysis included in the fitter and timing reports.
- Operating code cleanup and efficiency improvements.
- The ABEL language was upgraded to version 7.3 with the following changes:
  - ABEL-XST synthesis. ABEL designers can now choose ABEL-XST synthesis for similar synthesis results with improved software stability
  - WYSIWYG Support. New option for ABEL designers who want to assign the exact design implementation and not have the synthesis or fitting tools re-optimize the design
  - True bus notation for ABEL designs
- Improved design analysis included in fitter and timing reports.
- Operating code cleanup and efficiency improvements.

Conclusion

WebPACK ISE builds on the success of the original WebPACK with improvements to the Project Navigator design environment for improved ease of use. The Xilinx CPLD design implementation tool update included in WebPACK ISE provides design control, while the tight integration of new tools such as ECS, HDL Bencher, and StateCad extend the WebPACK functionality making WebPACK ISE the industry leader in design environments available over the Internet.

WebPACK ISE is a modular design tool available for free from the Internet at http://www.xilinx.com/products/software/webpowered.htm.