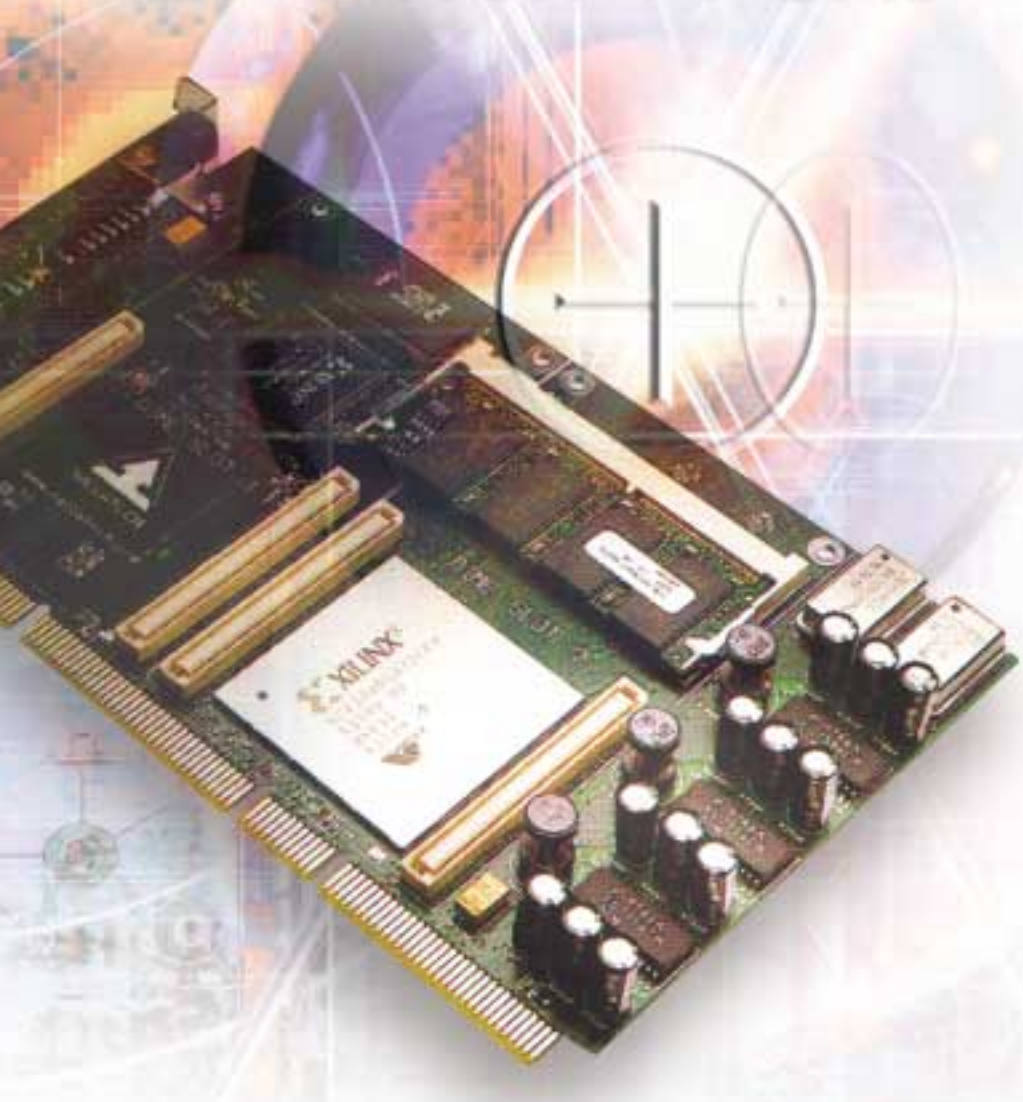
Elantec DC-DC Converter Solution for Virtex FPGAs



How to use the Elantec EL7564C DC-DC converter.

by Art Stryer
Sr. Field Applications Engineer, Elantec Semiconductor
astryer@elantec.com

For Virtex series FPGAs, separate supply voltages are used for the core circuitry and I/O interface power supplies; typically, the I/O interface requires 3.3V and the core circuitry requires either 2.5V or 1.8V. You need stable power supplies and you need to coordinate the power tracking and sequencing functions between supplies. Many board designs are challenged by these requirements.

Elantec Monopower™ Integrated-FET DC:DC Converters provide an optimal solution for Virtex FPGA designs. The EL7564C is a unique Synchronous Buck Converter with Integrated FETs and Internal Current Sensing. These features enable high efficiency, higher frequency (which leads to smaller inductors), and fewer external components, resulting in minimum board space.

Core	I/O
Frequency of Operation	Frequency of Operation
Logic Cell Utilization	Number of I/Os
Blockram Utilization	Toggle Rate
Toggle Rates	I/O Standard
Routing Density	Output Drive/Loading

Table 1 - Power Factors

The EL7564C can supply accurate voltages of 3.3V, 2.5V, 1.8V, and 1.5V in quantities up to 4 Amps. Devices can also be cascaded to deliver up to 8 Amps, or more. These devices meet power needs of the Virtex, Virtex-E, and Virtex-II FPGAs. In addition, the Elantec EL7564C is able to supply adjustable voltages for terminations, down to 1.0V.

Component	Label	Value	Manufacturer	Manufacturer's Phone Number	Part Number
Capacitor	C1a	330µF	Sprague	207-324-4140	293D337X96R3
Capacitor	C1b	0.1µF	Vitramon	203-268-6261	VJ0805Y104KXXA
Capacitor	C2, C10	2.2nF	Vitramon	203-268-6261	VJ0805Y222KXXA
Capacitor	C3, C6	0.22µF	Vitramon	203-268-6261	VJ0805Y224KXXA
Capacitor	C4	390pF, 5%	Vitramon	203-268-6261	VJ0805A471KXXA
Capacitor	C5	0.1µF	Vitramon	203-268-6261	VJ0805Y104KXXA
Capacitor	C7	330µF	Sprague	207-324-4140	293D337X96R3
Diode	D1		Telefunken	1-800-554-5565	BAT42W
Inductor	L1	4.7µH	Dale	605-665-9301	IDC-5020 4.7µF
Resistor	R1	1kΩ	Dale	402-563-6506	CRCW08051001
Resistor	R2	2320Ω	Dale	402-563-6506	CRCW08052321
Resistor	R4	22.1Ω	Dale	402-563-6506	CRCW080522R1

Table 2 - EL7564C Board Bill of Materials

An Example Design

The following design example will show you how easy it is to use the EL7564C. The following requirements are specified for the example:

- Input voltage range: V_{IN} = 4.5V - 5.5V
- Output voltage: V_O = 3.3V
- Max output voltage ripple: ΔV_O = 2%
- Output max current: I_O = 4A
- Switching Frequency: F_S = 350 Khz

The schematic is shown in Figure 1, and the bill of materials is shown in Table 2.

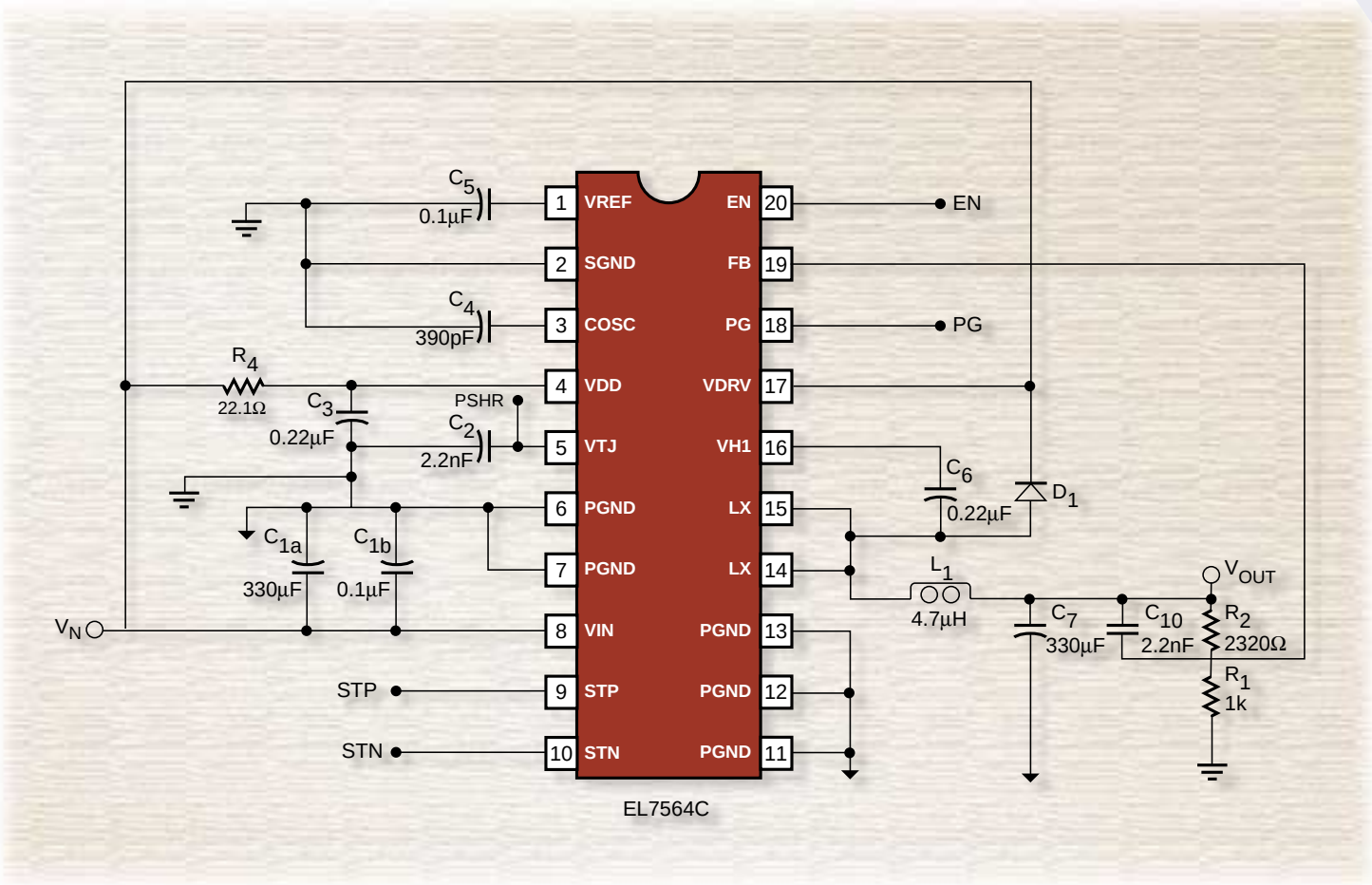


Figure 1 - EL7564C Board Circuit Schematic (VIN = 5V)

The following steps briefly outline how to choose the passive components. For a detailed design discussion, please refer to Elantec Application Note #18 "Designing a High Efficiency DC:DC Converter with the EL75XX."

Step 1 – Estimate your power requirements.

Go to www.xilinx.com/cgi-bin/powerweb.pl, and fill out the power estimator worksheet. This will tell you your power requirements.

The power requirements of your design are influenced by many factors, as shown in Table 1.

Step 2 – Choose the feedback resistor divider.

The feedback resistor divider determines the output voltage:

$$V_O = 1 + \left(\frac{R_2}{R_1}\right) * 1V$$

If R_1 is chosen to be 1kΩ, then $R_2 = 2.3k\Omega$

Step 3 – Choose the switching frequency.

Switching frequency has a great influence on the efficiency of the DC:DC converter and the size of the inductor. Usually, higher efficiency is achieved at lower frequencies as the switching losses of the semiconductors are lower. However, inductor component size decreases as frequency increases.

The EL7564C data sheet shows the F_S vs C_{OSC} curve. For F_S = 350 Khz, the curve indicates that C_4 = 390pF.

Step 4 – Choose inductor L1.

The EL7564C uses current mode control. A summing comparator generates the duty cycle of the internal power FETs. This comparator compares the feedback voltage with the internal preset reference voltage. Together with the patented current sense input, the comparator determines the ON and OFF time for the power FETs. For optimal operation, the inductor current ripple range should be less than 0.8A. The slope of the current ramp is a function of V_{IN}, V_{OUT}, and L_1.

If ΔI_L = 0.8A, then:

$$L = (V_{IN} - V_O) * \frac{1}{\Delta I_L} * \frac{V_O}{V_{IN}} * \frac{1}{F_S} = 4\mu H$$

Therefore, choose L_1 = 4.7µH

Step 5 – Choose output capacitor C7.

The output voltage ripple, ΔV_O , and output current ripple, ΔI_L, normally determine the C_7 value. The ESR (equivalent series resistance) of C_7 must be less than:

$$ESR = \frac{\Delta V_O}{\Delta I_{LMAX}} = 70m\Omega \quad Set\ \Delta V_O = 2\%$$

Assuming ΔI_L = 0.8A, Choose C_7 = 330µF (to meet ESR requirements) for output voltage ripple ΔV_O = 2%.

Step 6 – Choose input capacitor C1a.

If all the AC current is handled by the input capacitor C_{1a}, its RMS current is calculated as:

$$I_{IN},rms = \sqrt{[D*(1-D)]} * I_O$$
$$where\ D = duty\ cycle = \frac{V_O}{V_{IN}}$$

This yields 2A when D = 50%. Therefore you should choose a capacitor with 2A current handling capability. However, an additional capacitor is sharing current with it, thus the current requirement of C_{1a} can be reduced.

Choose: C_{1a} = 330µF and C_{1b} = 0.1µF

Step 7 – Choose the additional external components.

The Bill of Materials, shown in Table 2, specifies choices for the other required external components.

Layout Considerations

Many ICs contain low voltage and current level analog functions. They also require high current, high speed outputs for driving larger power loads. Integrating both of these functions within a single chip is difficult, due to the simultaneous yet opposing requirements for low noise and high power. To alleviate this, many newer ICs have separate "signal ground" and "power ground" pin connections. The goal is to localize the high current, high speed output noise into an "independent" loop which does not interfere with the more sensitive low level analog control functions.

The layout is very important for the converter to function properly. Signal Ground (SGND) and Power Ground (PGND) should be separated to ensure that the high pulse current in the Power Ground never interferes with the sensitive signals connected to Signal Ground. They should only be connected at one point (normally at the negative side of either the input or output capacitor.) In addition, the bypass capacitor C_3 should be as close to pins 2 and 4 as possible.

The heat of the chip is mainly dissipated through the PGND pins. Maximizing the copper area around these pins is preferable. In addition, a solid ground plane is always helpful for the EMI performance.

Conclusion

It's easy to power your Virtex designs using the Elantec EL7564C DC:DC converter. For data sheets, application briefs, and additional information contact Elantec online at www.elantec.com, or send an e-mail to: astryer@elantec.com.

The EL7564C DC-DC Converter

Features	Benefits
• Integrated FETs	• Low Board Space
• 4A Output Current	• No Heat Sinks
• Current Mode Control	• Cycle-by-cycle Limiting
• Synchronous Converter	• High Efficiency
• Over-current Protection	• No Short Circuits
• Over-temperature Protection	• Device Doesn't Blow Up
• Over-voltage Control	• Protects FPGAs, etc.
• Internal Current Sensing	• Accurate Feedback
• Die Temperature Monitor	• Simplifies Thermal Design
• Auxiliary Supply Tracking	• Power Sequencing