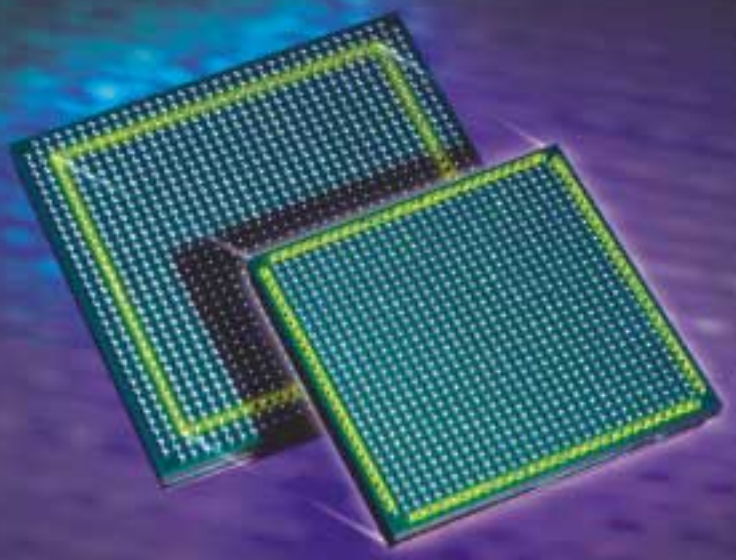
Footprints in Silicon:

Compatible Pinouts in Virtex-II Devices Enhance Design Flexibility

Advanced Virtex-II architecture allows you to change FPGA densities without changing PCB designs.



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Mid-production design changes are common in today's fast-paced production environment. These changes often force you to create new PC boards, and incur long delays, because you require a larger (or smaller) FPGA to meet your new design requirements. Design changes are inevitable, but now there is a way make them much easier, faster, and far less expensive.

The Virtex™-II FPGA family offers unique pinout/package migration paths that maintain PCB footprint compatibility across different device densities and packages. You can increase or decrease density from 40K to 10M system gates on the same PCB footprint. What's more, you can change some chip packages without losing footprint compatibility. With a little planning, you won't have to replace your PC boards when you upgrade to a new FPGA.

The Virtex-II family consists of 12 devices offered in 10 different packages. While, of course, they are not completely interchangeable, strategic Xilinx engineering has delivered unparalleled design migration flexibility. This article explains the rules and advantages of compatible device/package pinouts and footprints – and features a special transparency overlay that graphically illustrates compatible pinout migration.

Packaging

All 10 Virtex-II packages are ball grid arrays (BGAs):

- CS denotes wire-bond chip-scale BGA (0.80 mm pitch)
  - CS144 in 0.8 mm pitch
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch)
  - FG256
  - FG456
  - FG676
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch)
  - FF896
  - FF1152
  - FF1517

- BG denotes standard BGA (1.27 mm pitch)
  - BG575
  - BG728
- BF denotes flip-chip BGA (1.27 mm pitch)
  - BF957

For more details, see the Virtex-II Data Sheet (www.xilinx.com/partinfo/ds031.htm), or Chapter 4 of the *Virtex-II Platform FPGA User Guide* (www.xilinx.com/products/virtex/handbook/).

Pin Types

Virtex-II devices have the following pins:

- Programmable user I/Os (from 88 in the CS144 and FG256 packages to 1,108 in the FF1517 package)
- Power and ground pins
- Control pins, including configuration, JTAG, and special purpose pins such as VBATT.

All the pin types are similar regardless of the device/package combination. The number of control pins is always 16, including VBATT. The number of power/ground pins and user I/O pins, however, depends on each device/package combination.

The total number of user I/Os available for each device/package is based on two limitations:

- Maximum number of pins on the package (See Virtex-II Data Sheet – Module 1, "Wire-Bond Packages Information" and "Flip-Chip Packages Information.")
- Maximum number of pads on the die (different for wire-bond versus flip-chip applications).

For example, the FF1517 package limits the maximum number of user I/Os to 1,108 pins in the XC2V10000 device.

I/O Banking

Virtex-II user I/Os are split into eight banks to provide more flexibility in I/O standards choices and XCITE capabilities. The VCCO and VREF voltages, necessary to support I/O standards from 1.5V to 3.3V, are connected to pins that serve banks of I/O pins.

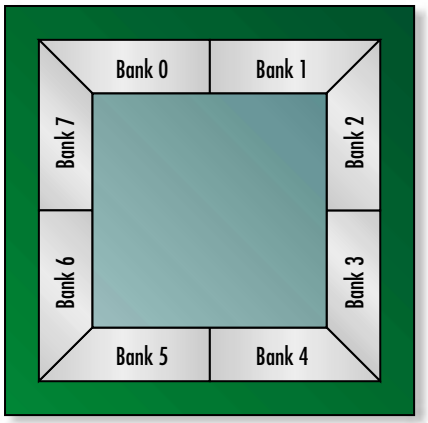


Figure 1 - Virtex-II I/O banks for wire-bond packages (CS, FG, and BG)

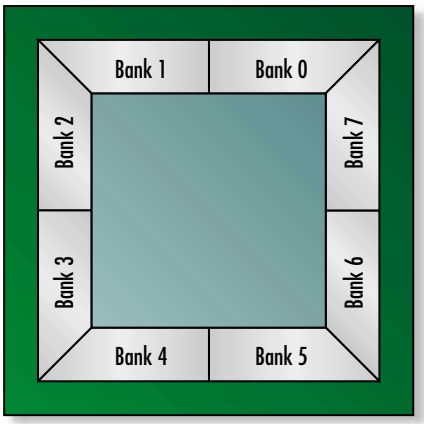


Figure 2 - Virtex-II I/O banks for flip-chip packages (FF and BF)

The bank organization depends on the package type. Figure 1 represents a top view for wire-bond packages (CS, FG, and BG) with banks in clockwise order, and Figure 2 shows a top view for flip-chip packages (FF and BF) with banks in counterclockwise order. All the pinout diagrams provided in Chapter 4 of the *Virtex-II Platform FPGA User Guide* are top views of the package.

For example, Table 1 illustrates the maximum number of pins per bank for the FG256 package. The user I/O count includes the VREF, VRP/VRN, and non-dedicated configuration pins. The definition of each pin type is in the Virtex-II Data Sheet – Module 4.

Device	XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000
Total user I/Os	88	120	172	172	172
Bank 0 - user I/Os	12	12	20	20	20
Bank 0 - V_{CCO_0}	3	3	3	3	3
Bank 1 - user I/Os	12	12	20	20	20
Bank 1 - V_{CCO_1}	3	3	3	3	3
Bank 2 - user I/Os	10	18	22	22	22
Bank 2 - V_{CCO_2}	3	3	3	3	3
Bank 3 - user I/Os	10	18	22	22	22
Bank 3 - V_{CCO_3}	3	3	3	3	3
Bank 4 - user I/Os	12	12	22	22	22
Bank 4 - V_{CCO_4}	3	3	3	3	3
Bank 5 - user I/Os	12	12	22	22	22
Bank 5 - V_{CCO_5}	3	3	3	3	3
Bank 6 - user I/Os	10	18	22	22	22
Bank 6 - V_{CCO_6}	3	3	3	3	3
Bank 7 - user I/Os	10	18	22	22	22
Bank 7 - V_{CCO_7}	3	3	3	3	3
Dedicated pins	16	16	16	16	16
VCCAUX (3.3 V)	4	4	4	4	4
VCCINT (1.5V)	8	8	8	8	8
Ground	32	32	32	32	32

Table 1 - Pinouts in the FG256 package

Pinout Compatibility

Pinout compatibility across different devices gives you a major advantage when designing your application. All the devices in a particular package are 100% pinout compatible. The 16 control pins are always located on the same package balls. All power and ground balls are at the same package ball location. Each programmable user I/O has the same ball name in the same bank, and the same package ball location, including LVDS (Low Voltage Differential Signaling) pairs. The main benefit here is that you can re-use the same PCB footprint for as many as six devices of different densities in one package.

For example, a BF957 package with its fixed ball assignment accommodates the XC2V2000, XC2V3000, XC2V4000, XC2V6000, XC2V8000, and XC2V10000 devices. This represents a 5X density ratio in a single footprint.

Table 2 summarizes the pinout compatibility of the entire Virtex-II family.

The full pinout compatibility of each of the 10 packages can be found in the individual package pinout tables in Module 4 of the Virtex-II Data Sheet. No Connect (NC) information is provided for the smaller devices in each package. When two devices have a No Connect, the NC of the larger device matches the NC of the smaller one to facilitate pinout migration.

Pinout Compatibility Across Packages

Virtex-II devices offer even more flexibility, because two package pairs are both pinout and footprint compatible. In other words, devices that are already pinout compatible within a package type are also footprint compatible with another package type. The two pinout/footprint compatible package pairs are wire-bond FG456 & FG676 and flip-chip FF896 & FF1152.

This additional flexibility allows you to produce a single PCB that can accommodate anything from the XC2V1000 in FF896 to the XC2V10000 in FF1152. This represents footprint compatibility across eight devices, for a density ratio of 10X.

As shown in Figure-3, the FF896 pinout diagram is drawn on a transparent page to demonstrate the footprint compatibility with the FF1152. Complete definitions of all the pin types listed in the pinout diagram are available in Module 4 of the Virtex-II Data Sheet.

Package	CS144	FG256	FG456 & FG676	FF896 & FF1152	FF1517	BG575	BG728	BF957
Min User I/Os	88	88	200	432	912	328	456	624
Max User I/Os	92	172	484	824	1,108	408	516	684
XC2V40	✓	✓						
XC2V80	✓	✓						
XC2V250	✓	✓	✓					
XC2V500		✓	✓					
XC2V1000		✓	✓	✓		✓		
XC2V1500			✓	✓		✓		
XC2V2000			✓	✓		✓	✓	✓
XC2V3000			✓	✓			✓	✓
XC2V4000				✓	✓			✓
XC2V6000				✓	✓			✓
XC2V8000				✓	✓			✓
XC2V10000				✓	✓			✓

Table2 - Virtex-II pinout compatibility

All the control pins and power/ground pins match the FF896 and FF1152 balls. All user I/Os are 100% footprint compatible – except the LVDS pairs. Because of the migration from one package to another, a particular user pin could have a different pin name at the same physical location. Pad locations across the two different packages use the following rules:

- The FF1152 has two more rows of balls on the top, bottom, left and right edges.
- A particular FF896 package location in the FF1152 location is calculated as follows;
  - Pin location is referenced by "Letter/Number" (for example, A2).
  - "Letter" indicates a row.
  - "Number" indicates a column.
  - FF1152 Letter/Number = FF896 Letter + 2 / Number +2

For example, the A2 pin of FF896 is the C4 pin of FF1152.

Using the above information, any user I/O of one package can be easily located in the second one. If digitally controlled impedance technology is used in Bank 4, you have the choice between:

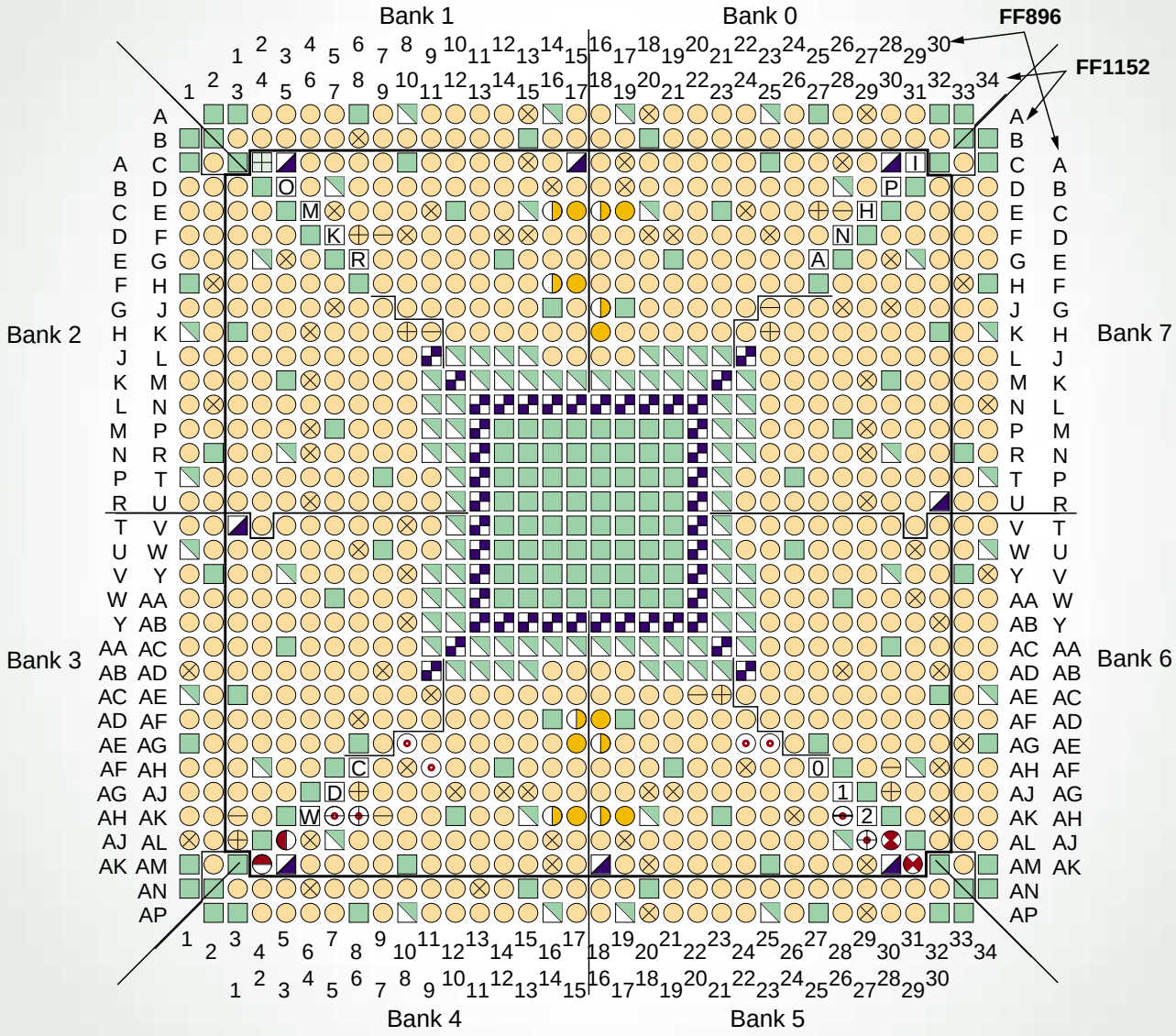
- If SelectMAP (parallel configuration) is not used, the alternative ALT_VRP and ALT_VRN pins can be used as reference resistors for Bank 4, and the two packages are fully pinout compatible.
- If the regular VRP and VRN pins in Bank 4 are used, however, then these two pins are not compatible.

In the pinout diagrams of Figure 3, dedicated pins are squares and programmable user I/Os are circles. All these pins match for each location.

Conclusion

The extreme flexibility of Virtex-II device pinouts facilitates early PCB prototyping. The large number of devices (as many as eight) fitting in one footprint offers you a choice of variable configurations for the same board, while reducing the cost of the overall Virtex-II solution.

Figure 3 - Pinout Compatibility Diagram
FF896/FF1152



User I/O Pins	Dedicated Pins	
IO LXXY #	C CCLK	N DXN
Dual-Purpose Pins:	P PROG B	A DXP
DIN/D0-D7	D DONE	VBATT
CS B	2 1 0 M2, M1, M0	RSVD
RDWR B	H HSWAP EN	VCCO
BUSY/DOUT	K TCK	VCCAUX
INIT B	I TDI	VCCINT
GCLKx (P)	O TDO	GND
GCLKx (S)	M TMS	n NO CONNECT
VRP	W PWRDWN B	
VRN		
VREF		
Triple-Purpose Pins:		
D2, D4/ALT_VRP		
D3, D5/ALT_VRN		

Corresponding Pinouts

FF896	FF1152
A2	C4
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AK29	AM31