

HyperTransport High Speed I/O

The Virtex-II Series expands programmable I/O flexibility and performance with 800 Mbps per channel.

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The Virtex®-II series provides a new low-voltage differential-signaling standard called “HyperTransport™” (formerly known as Lightning Data Transport or LDT) which is an I/O configuration available on all user I/O pins. HyperTransport is a new high-performance interconnect proposed by Advanced Micro Devices, Inc. (AMD) for interfacing to processors, memory, and I/O devices, and is a source-synchronous, point-to-point interface.

In a Virtex-II FPGA, when an I/O is configured for HyperTransport, the adjacent I/O pin is automatically determined by software and configured with a fast, very low-skew route for the N side of the differential pair. The HyperTransport buffer itself is a current-mode driver that produces the desired differential signal on chip, with no need for external source termination. This, along with the new dedicated easy-to-use Double Data Rate (DDR) registers in the input/output block (IOB), makes the implementation of HyperTransport in Virtex-II devices very user-friendly.

HyperTransport Overview

The HyperTransport interface takes data from the I/O interface to the device core and vice versa. For example, an 8-bit HyperTransport link goes from 8 bits of command/data at the I/O interface to 64 bits into the device core at a quarter of the input clock frequency. The 8-bit link consists of 1 bit for control, 1 clock, and 8 bits of command/data, which can operate at 400, 600, 800, 1000, 1200, or 1600 Mbps per channel. These data rates apply to one channel of data (one differential pair) clocked on both edges of the clock (DDR). Therefore, a 400 Mbps link has a 200 MHz clock and a total throughput of 3200 Mbps. Virtex-II devices can support up to 800 Mbps per channel.

The bus width can also be scaled to 2, 4, or 8 bits of data per clock, and with additional clocks it can be expanded to 16 or 32 bits of data. For example, 16-bit data requires 2 clocks, and 32-bit data requires 4 clocks.

Because HyperTransport is intended to be a very high-speed interface to a wide variety of components, signal integrity is crucial for this new standard to succeed. Low offset voltage, a low (tight) swing on VOD (Differential Output Voltage), and on-chip termination are some of the aspects of HyperTransport that contribute to a reliable, high-speed interface.

The I/O electrical specifications proposed by AMD call for low-voltage differential signaling similar to the IEEE LVDS I/O specifications. AMD has not proposed a bus/bi-directional implementation for HyperTransport, but such implementation is not precluded, because it is designed to be scalable at both bus-width and frequency levels.

Using HyperTransport in Virtex-II Devices

Implementing HyperTransport in Virtex-II devices is very straightforward. Simply instantiate the HyperTransport I/O buffer in HDL, and the software does the rest. Virtex-II devices have a new improved differential I/O buffer for HyperTransport (and LVDS). When one of these buffers is used, the software will automatically route the N channel to an adjacent IOB. Either the N channel or the P channel can be locked, and the soft-

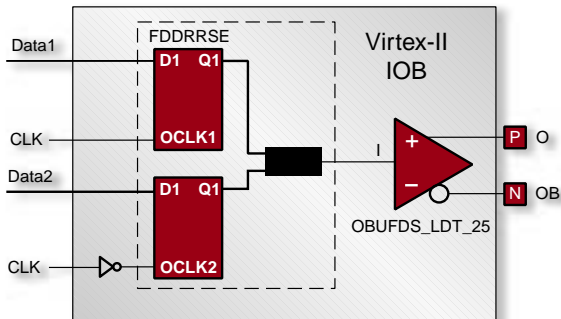


Figure 1 - Software implementation of HyperTransport and DDR implemented in a Virtex-II IOB

Table 1 provides the DC electrical characteristics of the Virtex-II HyperTransport I/O buffer, which provides on-chip source termination only; on-chip receiver termination is only necessary for higher speeds (1 Gbps and up).

Preliminary I/O Characterization Data

At this early stage in Virtex-II silicon characterization, not all aspects of the HyperTransport link have

been tested. However, the Eye diagram shown in Figure 2 demonstrates the Virtex-II HyperTransport I/O functioning at 840 Mbps DDR (I/O clock rate = 420 MHz). This test exercises one I/O interface only, stimulated by a 15-bit LFSR generating a pseudo-random pattern. The clock was generated using a 4x-multiply from the Virtex-II Digital Clock Manager (source clock = 105 MHz). These measurements were obtained using a differential probe and a 100-Ohm receiver-termination resistor. The scope capturing this Eye pattern was set to refresh every 10 seconds.

Conclusion

The new HyperTransport (formerly LDT) I/O standard gives you very high speed differential I/O capability. The HyperTransport interface, consisting of the HyperTransport I/O, two stages of mux/demux, and data alignment, will be available soon as a reference design and application note. Xilinx will offer various versions of HyperTransport cores (protocol layer) in Q2 or Q3 of 2001.

For more information about HyperTransport and Advanced Micro Devices, Inc., visit www1.amd.com/products/cpg/hypertransport/faq.

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	$R_T = 100 \text{ Ohm}$ across Q and Q signals	530	600	740	mV
Change in VOD Magnitude	ΔV_{OD}	$R_T = 100 \text{ Ohm}$ across Q and Q signals			30	mV
Output Common Mode Voltage	V_{OS}	$R_T = 100 \text{ Ohm}$ across Q and Q signals	550	600	680	mV
Change in VOS Magnitude	ΔV_{OS}				30	mV

Table 1 - Virtex-II HyperTransport DC electrical characteristics

ware automatically maintains the correct pin/pair orientation.

Because HyperTransport calls for double data rate, the DDR registers in the IOB are used. DDR is the equivalent of dual-edge clocking, but is implemented with two registers, clocked 180 degrees apart and multiplexed; the resulting output is twice the frequency of the clock. Virtex-II devices are designed with double data rate and differential signaling applications in mind, so the routing, resources, and timing are easily accommodated.

The Virtex-II IOB contains DDR registers for input, output, and 3-state implementations. To use the output or 3-state DDR registers, instantiation of the correct primitive is all that is required, and the DDR input registers can be inferred from your source code. Figure 1 demonstrates DDR and HyperTransport implemented in a Virtex-II IOB, and illustrates the correct primitive names.

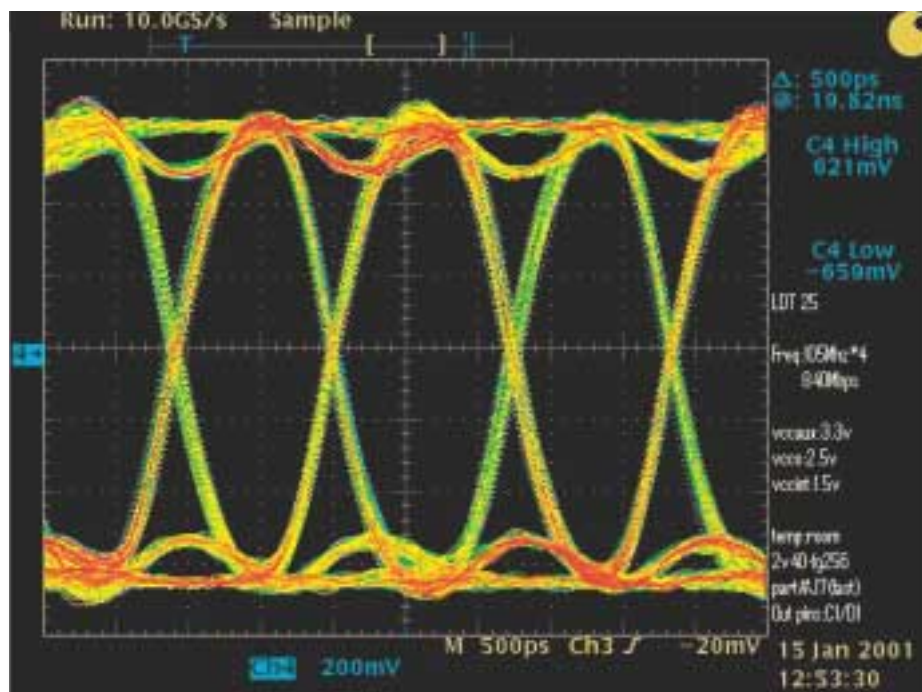


Figure 2 - Virtex-II HyperTransport I/O operating at 840 Mbps (420 MHz clock)