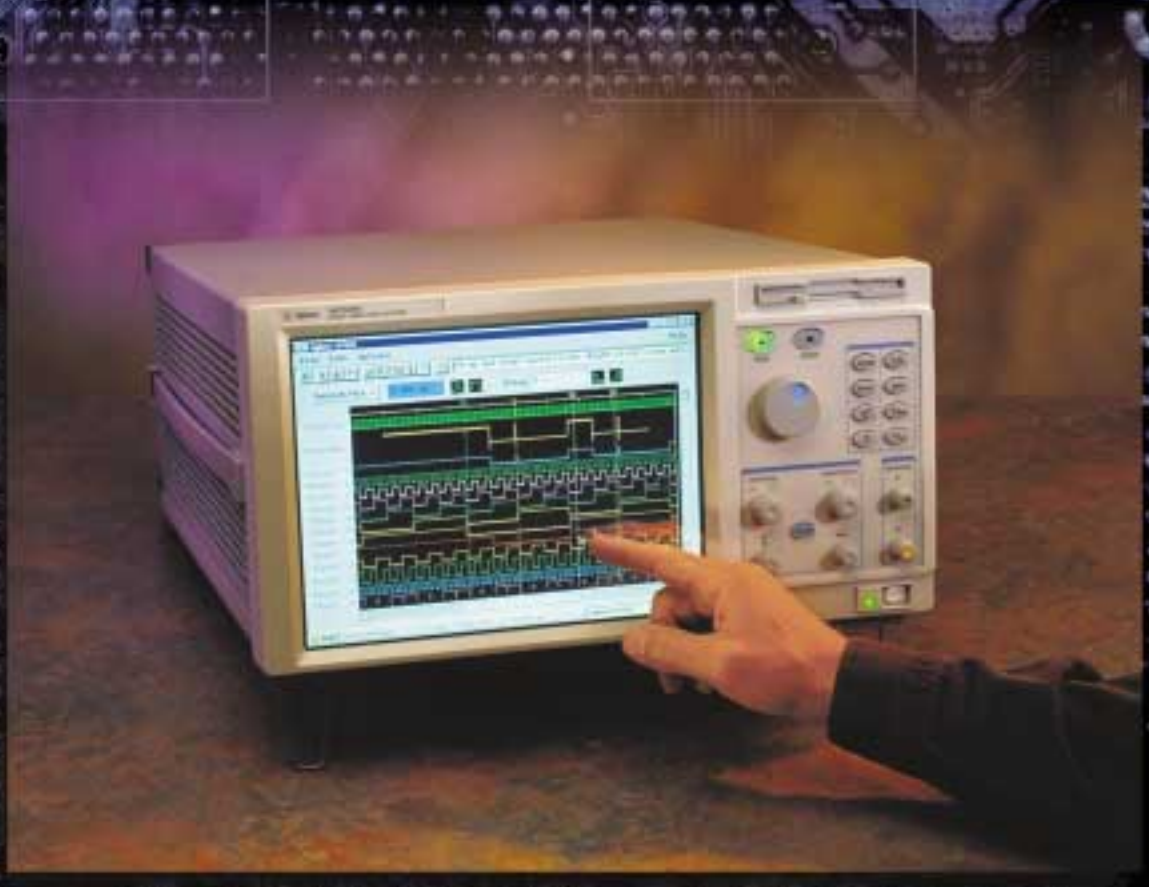
Debugging LVDS Signals in Virtex-II FPGAs

Many tools exist for simulating your design, but eventually you have to verify the operation of the actual device.



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Debugging complex, high performance FPGA designs can be a challenge. With single-ended signals you can simply connect a logic analyzer to all of the lines going into and out of a complex device and gather data to verify the system or locate the cause of a failure. Today, however, many high-speed designs are using differential signaling, such as LVDS, to minimize switching and crosstalk noise, and to allow data rates greater than one gigibit per second. The Virtex-II FPGA family includes LVDS capability on all I/O pins.

The Agilent Solution

The challenge you face when debugging differential signals is connecting them to a logic analyzer. The Agilent approach allows you to connect directly to the FPGA's LVDS signals. The Agilent 16760A state- and timing-analysis module (for the 16700 series logic analyzers) allows you to directly capture differential signals with an input amplitude as low as 200 mV p-p at speeds up to 1.25 Gbps. This module operates up to 800 Mbps state analysis and 1.25 Gbps in half-channel mode. It has a memory depth of 64 MB and a 500 ps setup and hold time capability. Each module contains 34 channels, or 17 channels when using time tags. Up to 170 channels can operate on a single time base and trigger.

The 16700 series logic analyzers provide many tools to assist in analyzing the data once it is acquired. For example, the Agilent B4640B Data Communications Tool Set adds many protocol analysis capabilities. It provides a high-abstraction view of the data and powerful time-correlation features to assist you in finding complex system-level problems.

Low Capacitance Probes

The probes for direct LVDS analysis must be designed into your system. Mating connectors are placed on the board, and the logic analyzer probe is connected directly to these connectors, shown in Figure 1. At very high speeds, the capacitive loading is critical; a highly capacitive probe will introduce reflections in addition to reducing slew rates and changing critical timing in your circuit.

The probes for the 16760A have only 1.5 pF of probe-tip capacitance, including the connector. These high-density connectors have ground pins located between every pair of signal pins, providing excellent channel-to-channel isolation at high speeds, thus enabling high-fidelity signal capture.

Figure 1 - Differential connectors

Automatic Setup and Hold Time Adjustment

Another difficulty presented by ever increasing data rates is that the data-valid window continues to shrink. Reliable measurements require that the logic analyzer's combined setup and hold window must be smaller than the data-valid window of the signal it is acquiring. The 16760A has a combined setup and hold time as low as 500 ps, matching the data-valid window of very high-speed buses.

Agilent's proprietary eye finder technology automatically adjusts the setup and hold window on each logic analyzer channel with 10-ps resolution. This eliminates the need for manual adjustment and ensures the highest confidence in accurate state measurements at speeds to 1.25 Gbps. Automation not only relieves you of the burden of making these tedious adjustments manually, but also allows you to optimize the logic analyzer so you don't waste time acquiring faulty data. In addition, as the system temperature or voltage changes, or you move to a different system, you can use eye finder to quickly optimize the logic analyzer and have confidence in the data.

Single-Ended Signals

At times you may find it easier to use single-ended signals so you can interface to legacy ASICs or other prototypes. The Virtex-II FPGAs allow you to create your design for differential signaling and then set the I/O pins to a single-ended I/O standard. When full-speed verification is needed, the FPGA can be reconfigured to the LVDS I/O standard with the same pinout – the development software will automatically grab an adjacent pin for the N-channel of the differential pair. The 16760A can also analyze single-ended signals and then convert to LVDS analysis along with the Virtex-II FPGA.

Conclusion

Debugging high performance systems that use differential signaling is now much easier with the Agilent 16760A state- and timing-analysis module.

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