Virtex-II Platform FPGAs Support System Packet Interface Standards for Optical Networks

The production release of SPI-4 Phase 2 cores to Xilinx communication customers worldwide, is a critical technology boost for multi-service, packet, and cell-based networking equipment.

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Xilinx has developed a suite of LogiCORE™ intellectual property blocks to perform the System Packet Interface (SPI) function between the Physical (PHY) and Data Link layer devices for POS/SDH (Packet Over SONET/Synchronous Digital Hierarchy) fiber optic applications. The cores address the exploding demands of network IP (Internet Protocol) traffic by ensuring Xilinx devices are compatible with the Optical Internetworking Forum's (OIF) SPI-4 Phase 2 standard as well as the SATURN® Development Group POS-PHYTM Level 4 (PL4) interface. The cores assure compliance with the OC-192 data transfer standard by moving IP packets at a data rate in excess of 10Gb/s.

Just in Time to Market

The interface cores, referred to as PL4 cores, make use of unique features available only in the Xilinx Virtex™-II Platform FPGA architecture – including DCM (Digital Clock Manager), enhanced Block RAM, and high-speed LVDS I/O buffers. Combined with Platform FPGA DDR (Double Data Rate) registers, the PL4 cores can support data rates up to 832Mb/s per pin pair.

Xilinx is working with the OIF and the ATM (Asynchronous Transfer Mode) Forum to promote the SPI-4 Phase 2 standard. Along with other industry-leading networking developers Xilinx is facilitating the design and deployment of data switching and routing products using interoperable optical networking technologies. The improved efficiencies and lower cost per Mbit of POS/SDH packet transfer makes it an enabling technology for gigabit routers, terabit and optical cross-connect switches, and a wide range of multi-service DWDM (Dense Wave Division Multiplexing) and SONET/SDH-based transmission systems. The PL4 cores implemented in Virtex-II FPGAs allow next-generation network developers to reduce their system time to market.

In addition to providing fully standard-compliant cores, Xilinx is collaborating with leading network device developers – including PMC-Sierra, AMCC, and Conexant – to ensure interoperability between the Xilinx networking cores and the latest industry products. By combining the leading-edge performance of Virtex-II devices, Xilinx PL4 cores, and PMC-Sierra's or Conexant's OC-192 PHY devices, a complementary solution is available to our mutual customers. With IP traffic on network backbones doubling every six to nine months, it is critical to provide a high performance, scalable, system solution.

Interfacing the PHY and Data Link Layers

The POS/SDH Physical Layer Level 4 (POS-PHY L4) interface allows the interconnection of Physical Layer devices to Data Link Layer devices in 10Gb/s POS, ATM, and Ethernet applications. While the Xilinx PL4 core can perform the interface functions on both sides of the PL4 bus as shown in Figure 1, the FPGA implementation is generally intended to operate on the Data Link Layer side.

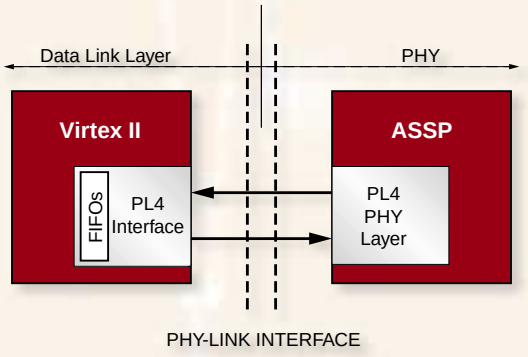

Figure 1 - OIF SPI-4 Phase 2 System Reference Model

The SPI-4 (PL4) interface has the following general characteristics:

- Point-to-point connection (such as between a single PHY Layer and a single Data Link Layer device)

- Support for 256 ports, suitable for STS-1 granularity in SONET/SDH applications (192 ports) and Fast Ethernet granularity in Ethernet applications (100 ports)
- Transmit/receive data path: 16-bits wide
- Source synchronous clocking where the source of the data provides a data clock
- In-band port address, start/end-of-packet indication, error-control code
- LVDS I/O (IEEE 1596.3 – 1996 [1], ANSI/TIA/EIA-644-1995 [2])
- 622 Mb/s minimum data rate per line using double data rate I/O
- Packet address, delineation information, and error-control coding sent in-band with data in both transmit and receive modes.

In addition to supporting the listed PL4 interface features, the Xilinx PL4 cores were developed with configurable FIFO buffers using Virtex-II Block RAM. The Virtex-II Block RAM provides high-performance data read/write access times and a four times increase in density over previous architectures. The Block RAM allows appropriate buffering to match the required channel support for the external PHY ASSP.

The cores use LVDS I/O buffers paired with dedicated DDR registers in the data path and LVTTL I/O buffers in the FIFO status path. The internal data rate is reduced by expanding the 16-bit words in DDR format on the PL4 interface to a 64-bit (four-word) single-edge clocked format running at half the PL4 clock rate. The core utilizes the Virtex-II DCM as shown in Figure 2. The DCM generates internal and external clocks to meet the aggressive system jitter requirements.

The cores implement "static alignment" of the received data to the clock by using the DPS (Digital Phase Shift) function of the DCM. The DPS module permits very fine-grained adjustments (under 50 ps) of the RDCLK (Received Clock) relative to the RDAT (Received Data). The fine resolution allows the RDCLK to be adjusted to the optimal sampling point relative to the RDATs eye pattern.

Not shown in Figure 2 are the PL4 FIFO interface blocks for implementing the single or multiple links or ports. The PL4 sink block stores data received for a particular link in a single FIFO buffer along with the link address information decoded from the control word preceding the data burst. When data is received, the address information is extracted from the received control word. The address and data are written into the sink FIFO. Two-bit dual-port Block RAMs are used to pass the per-channel FIFO status between the PL4 interface and the user's application. The PL4 sink block transmits the FIFO status information according to the contents of the FIFO status memories.

The PL4 source section decodes the FIFO status channel (flow control) information and writes it to the dual-port block RAM for each channel. The flow control information is used by the PL4 core to determine the channel status of the bus. Once the core receives the flow control information, it determines the link (address) and amount of data to send. The core monitors the fill level of the source FIFO to determine whether to send data or idle control words on the PL4 interface.

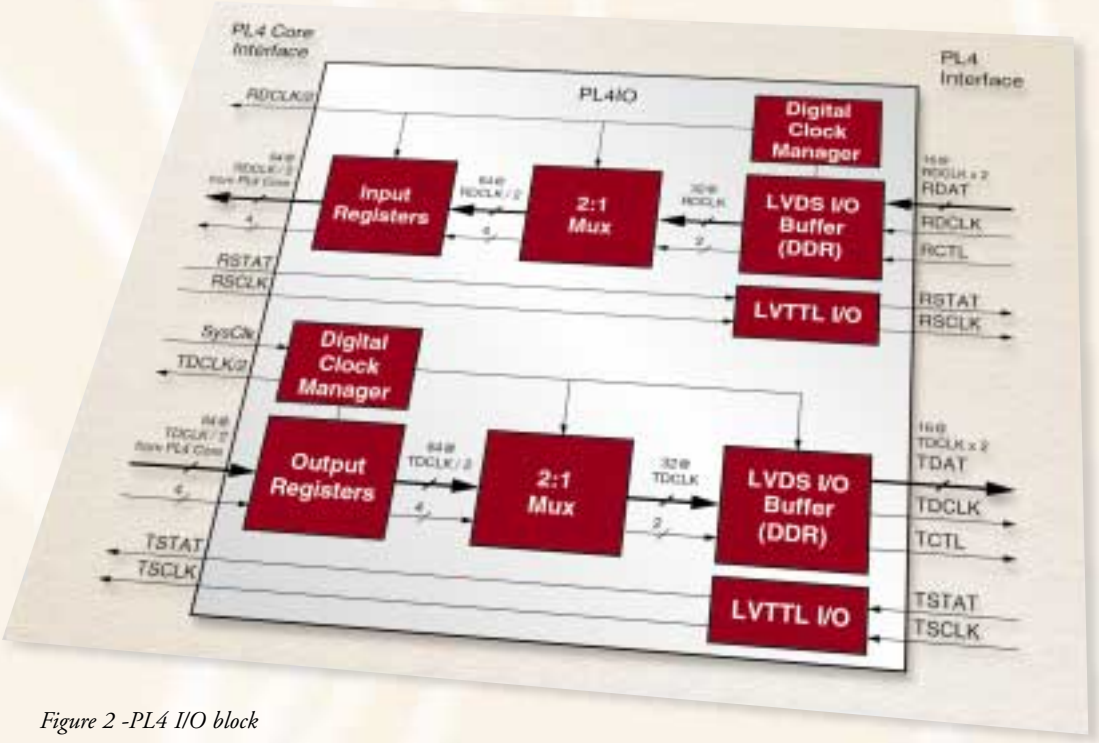

Figure 2 -PL4 I/O block

Conclusion

The Xilinx POS-PHY Level 4 cores are available as fixed netlists designed to interoperate with industry leading POS/ATM framers and mappers to achieve carrier-class performance. The cores have been configured to interface to a single-channel OC-192 device, a 10-channel by 1Gb/s device, and a 4-channel by 2.5Gb/s device.

Working in collaboration with engineering teams from PMC-Sierra and others, Xilinx is verifying the cores by using reference designs provided by each standard product developer. The Xilinx team solves system developers' 10 Gbps performance requirements by offering interoperable, standards-compliant, Packet-Over-SONET cores.