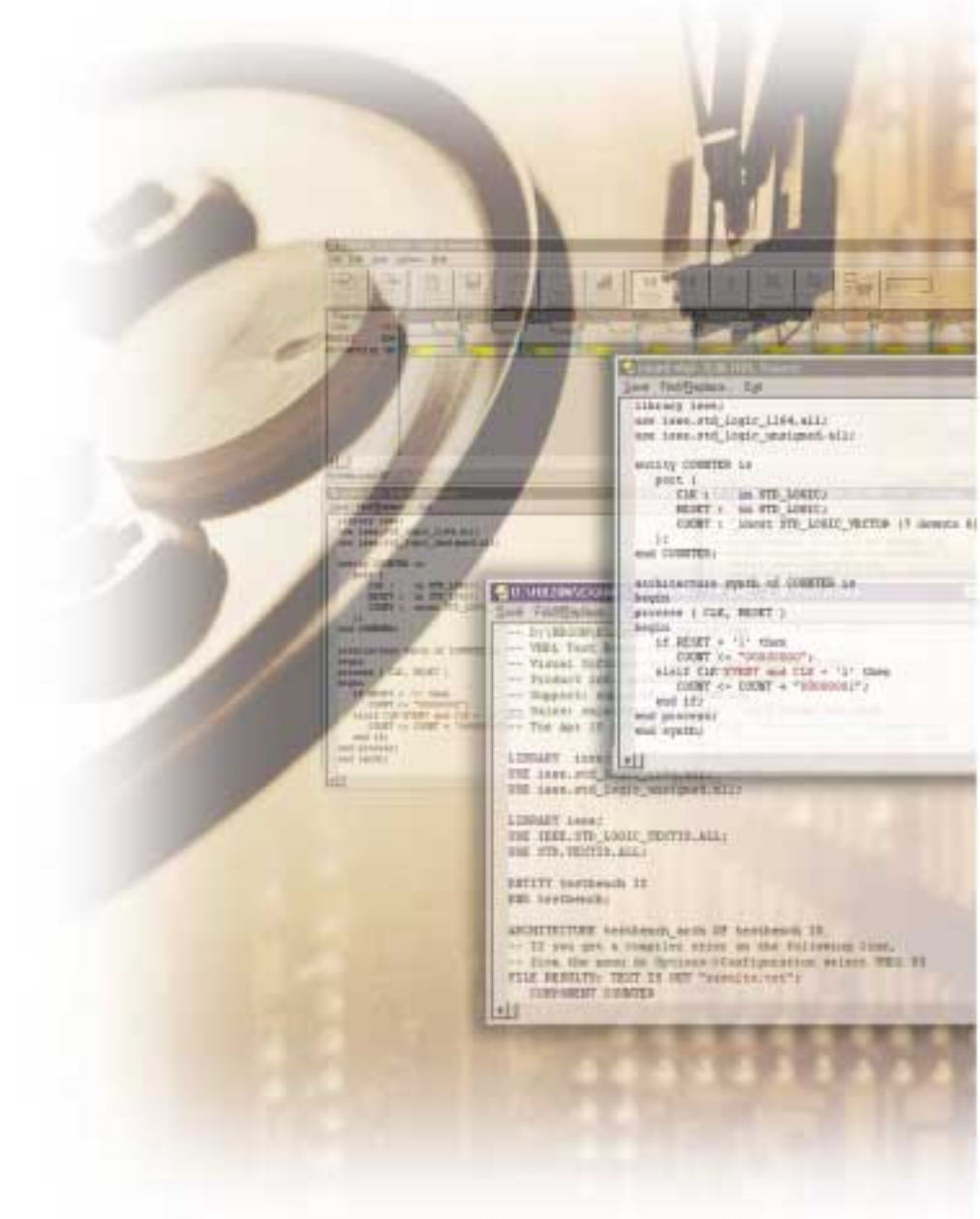
Verification for Platform FPGA Design

The Xilinx ISE software offers a wide range of design verification options.



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Virtex-II® designs can be very large and complex. A common strategy to complete these large density designs is to partition them into modules. To verify these individual modules, and then verify the final design, you need the robust verification capabilities contained in the new ISE software from Xilinx.

Checkpoint Verification

The Xilinx ISE software allows you to verify your design at each stage of development. These "checkpoints" help you identify any potential problems early in your design, where they are easier to correct.

HDL Simulation

HDL simulation is a solid verification method for individual design modules. Xilinx integrates the flexibility of HDL simulation into the ISE implementation tools, so each module can be verified at different stages of design work:

- During HDL creation – To verify logic functionality
- After synthesis – To check design functionality before going to Place and Route
- After Place and Route – Using back-annotated device path delays.

The Xilinx ISE Foundation software includes a version of the well-known ModelSim™ family of HDL simulators offered by Model

Technologies. ModelSim gives you the speed and ease-of-use needed for high-density HDL simulation. The ISE software also supports the various HDL simulators offered by other EDA software suppliers.

Testbench Generation

For HDL simulation, you must create test vectors for each module; a task that rapidly expands as your designs become larger, particularly when HDL simulation is used to verify the overall device. To automate this process, Xilinx now offers the HDL Bencher™ software, as part of the ISE software package (shown in Figure 1). With the HDL Bencher software, you can quickly and easily create a testbench for each design module, early in the design process.

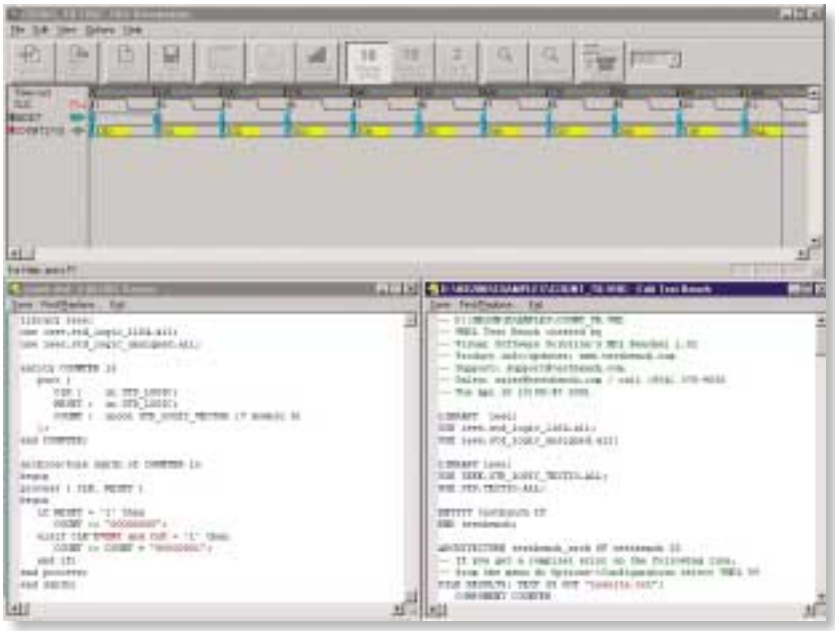

Figure 1 - HDL Bencher

With the HDL Bencher software you don't have to spend time generating test vectors or learning a scripting language because the graphic interface supports quick extraction of a test suite at either a beginner or expert level. This automatic testbench generation capability enhances the checkpoint verification strategy, operating as a "known-good" evaluation criteria that tracks each module during design.

Design Module to Chip Verification

There are various verification methods and tools available for both the individual design modules, and for verifying the overall device. HDL Simulation is an example of a verification option that works at the module level or overall device level. However, high-density design requirements are driving the use of new verification strategies as well.

Static Timing Analysis

Static timing analysis (STA) is now well established as a chip design checkpoint, and has been considered the "sign-off" level timing verification for FPGAs for several years. Xilinx Static Timing Analysis is delivered as part of the ISE software and you can easily use it as your final programmable device checkpoint. With the upcoming version 4.1i of ISE software, you will also have the option of using Synopsys PrimeTime™ for FPGA verification.

You can also create a STAMP model for any finished Xilinx high-density device. STAMP models let you integrate FPGA pin-to-pin delays into system-level PC board tools, so the FPGA is accurately represented in your overall system level analysis.

Formal Verification

In the upcoming version 4.1i of Xilinx software, formal verification tools from Synopsys and Verplex will be supported. Formal verification is a unique new technology brought about by the transition into even higher density design projects.

As the potential gate counts of designs have grown, the need for test vectors has grown accordingly at a geometric rate. Device verification therefore becomes a daunting task. This has led to the growth of formal verification strategies for large-scale programmable designs.

In the "equivalence checking" version of formal verification, mathematical algorithms are used to verify the logic at each phase of the design against the pre-synthesis version. By comparing blocks of logic, equivalence checkers can compare designs in a matter of minutes, instead of the hours or days that are required using traditional gate-level simulation techniques. Whenever a new stage of the design flow has been completed, you can quickly and efficiently run the equivalence checker to verify that the design is still accurate.

Verification In-System

Using a logic analyzer is a common way to verify the accuracy of hardware, so Xilinx created a debugging tool that integrates a logic analyzer onto the silicon itself. Our ChipScope software, combined with the Integrated Logic Analysis (ILA) core, allows real-time access to any node in the FPGA, with an easy-to-use GUI interface. You can easily and quickly verify device functionality, without the added overhead of creating bed-of-nails tests and fixtures. For Platform FPGA design, particularly in leadless packages, ChipScope ILA delivers real-time, on-chip de-bugging.

Conclusion

The Xilinx ISE software contains a variety of verification methodologies that enable you to verify your Virtex-II designs. At the module level or the device level, you can ensure that your designs will work correctly in the real world.

For more information on Xilinx ISE software go to: http://www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=Design+Tools