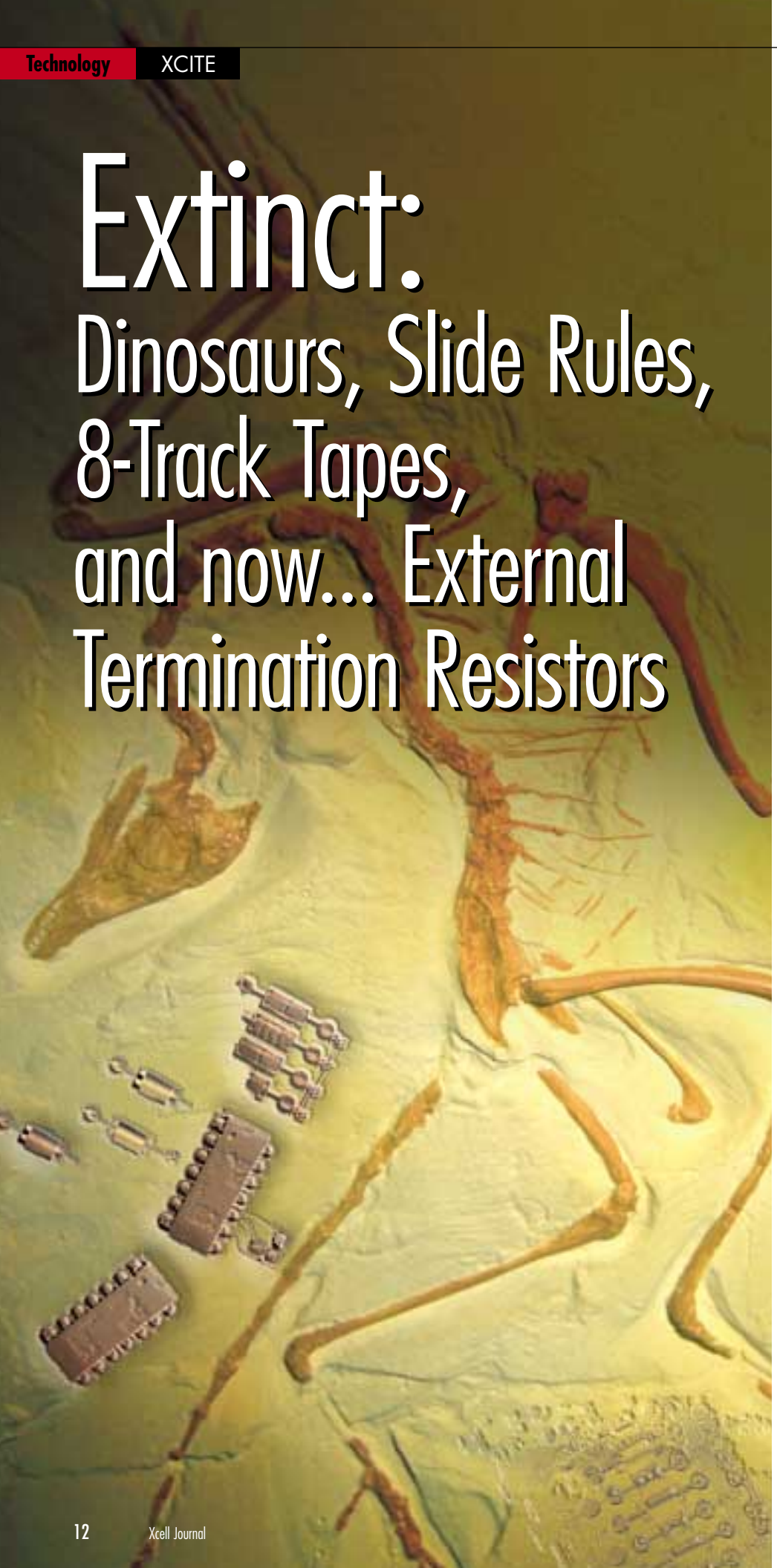
Extinct: Dinosaurs, Slide Rules, 8-Track Tapes, and now... External Termination Resistors



Xilinx Virtex-II Platform FPGAs now feature the world's first on-chip digitally controlled impedance-matching technology.

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Termination resistors as we know them are about to vanish. XCITE (Xilinx Controlled Impedance TEchnology) – the adaptive on-chip termination system now available in the Virtex®-II family of FPGAs – banishes external resistors, making PCBs (Printed Circuit Boards) less expensive, easier to design, and more reliable.

High performance systems require signal frequencies in the hundreds of megahertz, necessitating impedance matching between device I/Os and PCB traces. In the past, as clock speeds increased and I/O standards changed, system engineers and PCB designers learned signal termination techniques, using external resistors to match impedances. Over time, more and more resistors were required to account for the increasing widths of large data busses. With the advent of 1,500-pin packages, discrete resistor placement became a major challenge.

External termination resistors necessitate more board traces and increased PCB part counts, making the layout process more time consuming. These factors lead to higher manufacturing costs and longer times to market. Additionally, sky-high part counts do not help system reliability either – each additional part increases the risk of a system failure.

Here at Xilinx, our Virtex-II team wanted designers to have a worry-free solution to terminating high-speed signals, so we invented XCITE I/O. All Virtex-II I/O pins are equipped with XCITE, making impedance matching a pre-engineered solution.

XCITE can be used to terminate a variety of I/O standards. All variants of HSTL (High-Speed Transistor Logic), SSTL (Solid State Track Link), GTL (Gunning Transceiver Logic), and LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) are supported. Designers need only specify their signal I/O standard in the software. In the case of the bidirectional standard HSTL Class II, the external resistors usually required for the source and destination are implemented on-chip (see Figure 1). The PCB designer only has to route a 50Ω trace from the output of one Virtex-II device to the input of another (see Figure 2).

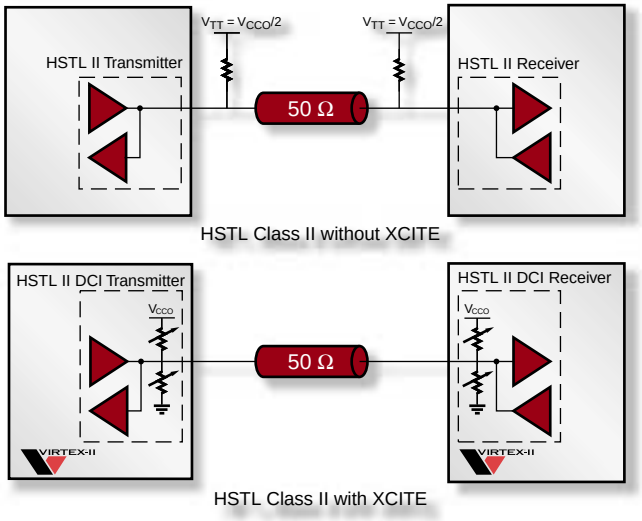

Figure 1 - Termination resistors on-chip

Not only does XCITE make PCBs less complicated, it actually improves signal quality. With termination residing inside the device instead of a few centimeters away, stub reflection is eliminated as a design factor.

XCITE is a better solution than discrete resistors because it continually adjusts the termination impedance to match the PCB trace impedance. In conventional systems, temperature and voltage variations can play havoc with the carefully engineered impedances of a signal path. With XCITE, the termination impedance of the driver or receiver is continually compared against a reference resistor. Over the full range of temperature, voltage, and process variations, XCITE maintains a tight impedance match.

I/O counts will continue to increase, and so will clock speeds. The Virtex-II architecture makes this situation livable by offering the latest high-speed I/O standards without the difficulties of external termination resistors (or punchcards).

For more information on XCITE, consult Chapter 2 of the Virtex-II Platform FPGA Handbook, which can be found online at www.xilinx.com/products/virtex/handbook/.

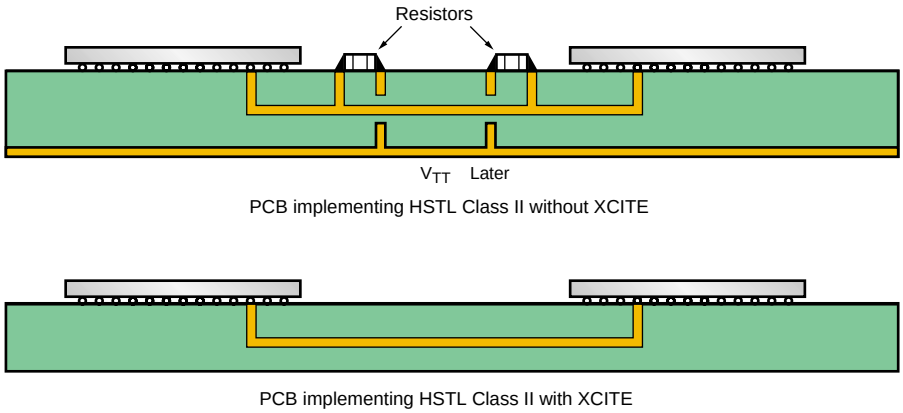

Figure 2

How XCITE Works

Both series and parallel termination schemes can be implemented with XCITE. While parallel termination is realized on-chip with pull-up and pull-down resistors, series termination is realized with a controlled impedance driver. The output impedance of this driver is set to equal the impedance of the PCB trace. XCITE transmitters can operate with parallel termination, a controlled-impedance driver, or a combination of the two; XCITE receivers can operate with parallel termination. Because of the way it is implemented, parallel XCITE termination may terminate to either the full VCCO voltage or to a VCCO/2 (as in the HSTL Class II standard).

XCITE matches its impedance to a pair of external reference resistors. These reference resistors are connected to dual-function pins on the Virtex-II device. Each of the eight I/O banks has two of these dual-function pins, VRN and VRP. If XCITE is not used in a bank, these pins are available for user I/O.

Reference resistors are chosen to have the same impedance value as the PCB trace. XCITE can match any impedance from 25Ω to 100Ω. The XCITE I/O matches the reference value by selectively enabling or disabling parallel transistors. A coarse impedance adjustment is made during the device startup sequence, accounting for process variation. During device operation, fine adjustments are continually made to ensure that I/O impedance stays matched as temperature and voltage drift.

XCITE is implemented in software either by direct HDL instantiation or through the IOSTANDARD attribute in the constraints file. The following are examples of each:

VHDL

```
HSTL_DCI_buffer: OBUF_HSTL_I_DCI
port map (I => data_out, O => data_out_DCI);
```

UCF or NCF

```
NET <net name> IOSTANDARD =
OBUF_LVDCI_25;
```

(Where <net name> is the name of the net between the IPAD and IBUF, or OPAD and OBUF. For HDL designs, this name is the same as the port name.)