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XILINX VIRTEX FPGAs

http://www.xilinx.com/products/platform/

		Virtex-II Pro (1.5V)					Virtex-II (1.5V)											Virtex-E (1.8V)												V-EM (1.8V)	
		XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP50	XC2V40	XC2V80	XC2V250	XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000	XCV50E	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E	XCV1600E	XCV2000E	XCV2600E	XCV3200E	XCV405E	XCV812E
Pins	**Body Size**	**I/O's**	204	348	396	564	852	88	120	200	264	432	528	624	720	912	1104	1296	176	176	284	316	404	512	660	724	804	804	804	404	556
PQFP Packages (PQ)																															
240	32 x 32 mm																	158	158	158	158	158	158	158							
HQFP Packages (HQ)																															
240	32 x 32 mm																		158				158								
Chip Scale Packages — wire-bond chip-scale BGA (0.8 mm ball spacing)																															
144	12 x 12 mm						88	92	92									94	94	94											
BGA Packages (BG) — wire-bond standard BGA (1.27 mm ball spacing)																															
352	40 x 40 mm																		196	260	260										
432	40 x 40 mm																				316	316	316								
560	42.5 x 42.5 mm																					404	404	404	404	404			404	404	
575	31 x 31 mm										328	392	408																		
728	35 x 35 mm												456	516																	
FGA Packages (FG) — wire-bond fine-pitch BGA (1.0 mm ball spacing)																															
256	17 x 17 mm	140	140				88	120	172	172	172							176	176	176	176										
456	23 x 23 mm	156	248	248					200	264	324									284	312										
676	27 x 27 mm											392	456	484								404	444						404		
680	40 x 40 mm																						512	512	512	512					
860	42.5 x 42.5 mm																							660	660	660					
900	31 x 31 mm																						512	660	700					556	
1156	35 x 35 mm																							660	724	804	804	804			
FFA Packages (FF) — flip-chip fine-pitch BGA (1.0 mm ball spacing)																															
672	27 x 27 mm	204	348	396							432	528	624																		
896	31 x 31 mm			396	556						432	528	624																		
1152	35 x 35 mm				564	692								720	824	824	824														
1517	40 x 40 mm					852									912	1104	1108														
BFA Packages (BF) — flip-chip fine-pitch BGA (1.27 mm ball spacing)																															
957	40 x 40 mm				564	584							624	684	684	684															

Note: All devices in a particular package are pin-out (footprint) compatible
Virtex-II packages FG456 and FG676 are footprint compatible
Virtex-II packages FF896 and FF1152 are footprint compatible.
Important: Verify all Data with Device Data Sheet (http://www.xilinx.com/products/virtex2pro/platform.htm)

Numbers indicated in the matrix are the maximum number of user I/O's for that package and device combination.

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Platform FPGAs

			CLB Resources					BLK RAM		DSP	CLK Resources				I/O Features				Speed						
		System Gates (see note 1)	CLB Array (Row X Col)	Number of Slices	Logic Cells (see note 2)	CLB Flip-Flops	Max. Distributed RAM Bits	# Block RAM	Block RAM (kbits)	# Dedicated Multipliers	DLL Frequency (min/max)	# DLL's	Frequency Synthesis	Phase Shift	Digitally Controlled Impedance	Number of Differential I/O Pairs	Max. I/O	I/O Standards	Commercial Speed Grades (slowest to fastest)	Industrial Speed Grades (slowest to fastest)	Serial PROM Family		Config. Memory (Bits)	Rocket I/O Transceiver Blocks	PowerPC Processor Blocks
	Virtex-II Pro Family — 1.5 Volt																								**.13um Nine Layer Copper Process**
VIRTEX-II PRO	XC2VP2	*	16 x 22	1,408	3,168	2,816	44K	12	216	12	24/420	4	DCM	DCM	YES	100	204	LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVPECL-25, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V) SSTL2I, SSTL2II, SSTL3 I, SSTL3 II	-6 -7 -8	-6 -7	ISP	OTP	1.30M	4	0
	XC2VP4	*	40 x 22	3,008	6,768	6,016	94K	28	504	28	24/420	4	DCM	DCM	YES	172	348		-6 -7 -8	-6 -7			3.01M	4	1
	XC2VP7	*	40 x 34	4,928	11,088	9,856	154K	44	792	44	24/420	4	DCM	DCM	YES	196	396		-6 -7 -8	-6 -7			4.49M	8	1
	XC2VP20	*	56 x 46	9,280	20,880	18,560	290K	88	1,584	88	24/420	8	DCM	DCM	YES	276	564		-6 -7 -8	-6 -7			8.21M	8	2
	XC2VP50	*	88 x 70	22,592	50,832	45,184	706K	216	3,888	216	24/420	8	DCM	DCM	YES	420	852		-6 -7 -8	-6 -7			19.0M	16	4
	Virtex-II Family — 1.5 Volt																								**.15um Eight Layer Metal Process**
VIRTEX-II	XC2V40	40K	8 x 8	256	576	512	8K	4	72	4	24/420	4	DCM	DCM	YES	44	88	LDT-25, LVPECL-33, LVDS-33, LVDS-25, LVDSEXT-33, LVDSEXT-25, BLVDS-25, ULVDS-25, LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I, HSTL II, HSTL III, HSTL IV, SSTL2I, SSTL2II, SSTL3 I, SSTL3 II, AGP-2X	-4 -5 -6	-4 -5	ISP	OTP	0.4M		
	XC2V80	80K	16 x8	512	1,152	1,024	16K	8	144	8	24/420	4	DCM	DCM	YES	60	120		-4 -5 -6	-4 -5			0.6M		
	XC2V250	250K	24 x16	1,536	3,456	3,072	48K	24	432	24	24/420	8	DCM	DCM	YES	100	200		-4 -5 -6	-4 -5			1.7M		
	XC2V500	500K	32 x 24	3,072	6,912	6,144	96K	32	576	32	24/420	8	DCM	DCM	YES	132	264		-4 -5 -6	-4 -5			2.8M		
	XC2V1000	1M	40 x 32	5,120	11,520	10,240	160K	40	720	40	24/420	8	DCM	DCM	YES	216	432		-4 -5 -6	-4 -5			4.1M		
	XC2V1500	1.5M	48 x 40	7,680	17,280	15,360	240K	48	864	48	24/420	8	DCM	DCM	YES	264	528		-4 -5 -6	-4 -5			5.7M		
	XC2V2000	2M	56 x 48	10,752	24,192	21,504	336K	56	1008	56	24/420	8	DCM	DCM	YES	312	624		-4 -5 -6	-4 -5			7.5M		
	XC2V3000	3M	64 x 56	14,336	32,256	28,672	448K	96	1728	96	24/420	12	DCM	DCM	YES	360	720		-4 -5 -6	-4 -5			10.5M		
	XC2V4000	4M	80 x 72	23,040	51,840	46,080	720K	120	2160	120	24/420	12	DCM	DCM	YES	456	912		-4 -5 -6	-4 -5			15.7M		
	XC2V6000	6M	96 x 88	33,792	76,032	67,584	1056K	144	2592	144	24/420	12	DCM	DCM	YES	552	1104		-4 -5 -6	-4 -5			21.9M		
	XC2V8000	8M	112 x 104	46,592	104,832	93,184	1456K	168	3024	168	24/420	12	DCM	DCM	YES	412	824		-4 -5	-4			29.1M		
	Virtex-E Family — 1.8 Volt																								**.18um Six Layer Metal Process**
VIRTEX-E	XCV50E	72K	16 x 24	768	1,728	1,536	24K	16	64K	NA	25/350	8	YES	YES	NA	88	176	LVTTL, LVCMOS2, LVCMOS18, PCI33, PCI66, GTL, GTL+, HSTL I, HSTL III, HSTL IV, SSTL3 I, SSTL3 II, SSTL21, SSTL211, BLVDS, LVDS, LVPECL	-6 -7 -8	-6 -7	ISP	OTP	0.6M		
	XCV100E	128K	20 x 30	1,200	2,700	2,400	37.5K	20	80K	NA	25/350	8	YES	YES	NA	98	196		-6 -7 -8	-6 -7			0.9M		
	XCV200E	306K	28 x 42	2,352	5,292	4,704	73.5K	28	112K	NA	25/350	8	YES	YES	NA	142	284		-6 -7 -8	-6 -7			1.45M		
	XCV300E	412K	32 x 48	3,072	6,912	6,144	96K	32	128K	NA	25/350	8	YES	YES	NA	158	316		-6 -7 -8	-6 -7			1.88M		
	XCV400E	570K	40 x 60	4,800	10,800	9,600	150K	40	160K	NA	25/350	8	YES	YES	NA	202	404		-6 -7 -8	-6 -7			2.7M		
	XCV600E	986K	48 x 72	6,912	15,552	13,824	216K	72	288K	NA	25/350	8	YES	YES	NA	256	512		-6 -7 -8	-6 -7			3.97M		
	XCV1000E	1,569K	64 x 96	12,288	27,648	24,576	384K	96	384K	NA	25/350	8	YES	YES	NA	330	660		-6 -7 -8	-6 -7			6.6M		
	XCV1600E	2,188K	72 x 180	25,920	34,992	51,840	486K	144	576K	NA	25/350	8	YES	YES	NA	362	724		-6 -7 -8	-6 -7			8.4M		
	XCV2000E	2,542K	80 x 120	19,200	43,200	38,400	600K	160	640K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			10.2M		
	XCV2600E	3,264K	92 x 138	25,392	57,132	50,784	793.5K	184	736K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			13M		
	XCV3200E	4,074K	104 x 156	32,448	73,008	64,896	1014K	208	832K	NA	25/350	8	YES	YES	NA	402	804		-6 -7 -8	-6 -7			16.3M		
	Virtex-EM Family — 1.8 Volt																								**.18um Six Layer Metal Process**
	XCV405E	1.31M	40 x 60	4,800	10,800	9,600	150K	140	560K	NA	25/350	8	YES	YES	NA	202	404	Same As Virtex-E	-6 -7 -8	-6 -7	ISP	OTP	3.43M		
	XCV812E	2.54M	56 x 84	9,408	21,168	18,816	294K	280	1120K	NA	25/350	8	YES	YES	NA	278	556		-6 -7 -8	-6 -7			6.52M		

Note: 1. System Gates include 20-30% of CLBs used as RAM
2. A Logic Cell is defined as a 4 input LUT and a register
DCM – Digital Clock Management

Important: Verify all Data with Device Data Sheet (http://www.xilinx.com/products/virtex2pro/platform.htm)

* System gate count not meaningful for Virtex-II Pro devices with embedded special blocks such as PowerPC processors and multigigabit transceivers.