Application Brief Summaries

XBRF001 **XC4000E Select-RAM™ Memory: Flexibility with Speed** **XC4000E/EX FPGAs**

The Xilinx XC4000 Select-RAM memory offers the best size flexibility and at the same time offers high speed operation with very little waste.

XBRF002 **Low Power Benefits of XC400E/X: Overview** **XC4000E/EX FPGAs**

The Xilinx XC4000E/EX/XL families offer low power architectures which have been optimized for high speed, high density operation, giving the customer reliable operation with many package options while satisfying the need for very high performance designs. Xilinx devices consume one half to one third the power of competitive devices.

XBRF003 **XC4000E SelectRAM Maximum Configurability** **XC4000E/EX FPGAs**

XC4000E SelectRAM Maximum Configurability

XBRF005 **XC4000EX Routing: A Comparison with XC4000E and ORCA** **XC4000E/EX FPGAs**

The new XC4000EX family includes large amounts of new routing resources, necessary to support today's larger designs. These resources are detailed and compared with the XC4000E, and with ORCA devices from Lucent Technologies (formerly AT&T).

XBRF006 **PLL Design Techniques and Usage in FPGA Designs** **FPGAs**

This paper examines some general concepts concerning Phase Locked Loop (PLL) usage and their application in programmable logic devices. A critique of a newly-announced PLL implementation for FPGAs also is included.

XBRF007 **XC4000 Series FPGAs: The Best Choice for Delivering Logic Cores** **FPGAs**

Reusable logic cores provide an efficient means of embedding common logic functions in high-density FPGA designs. The rich feature set of the XC4000-Series FPGA devices makes them the ideal choice for core-based system design.

XBRF011 **An Alternative Capacity Metric for LUT-Based FPGAs** **FPGAs**

As an alternative to "gate counting", the capacity of look-up table-based FPGAs can be measured more directly and objectively by examing the number of available "logic

XBRF014 **A Simple Method of Estimating Power in XC4000XL/EX/E FPGAs** **FPGAs**

A simple method is presented for estimating power dissipation in XC4000X Series FPGAs. This method is targeted for early estimates during design conceptualization before detailed design information is available. A second application note, “Estimating Power Consumption in XC4000XL/EX/E devices”, will describe how to make more accurate estimates of power dissipation when more information is known about the design.

XBRF015 **Speed Metrics for High-Performance FPGAs** **FPGAs**

Performance data (in terms of circuit speed) is provided for several key logic and routing functions implemented in XC4000XL-09 FPGAs, for purposes of overall system performance estimation. Performance data also is provided for equivalent implementations in the Altera FLEX 10K-2 family devices.

XBRF017 **XC9500XL vs. MAX7000A Architecture Comparison** **XC9500XL CPLDs**

This discussion focuses on comparing the Xilinx XC9500XL CPLD family with the Altera MAX7000A (including MAX7000AE) family. Both families address the high speed 3.3V ISP CPLD marketplace, where new developments in low voltage systems demand new solutions from CPLDs. The newer XC9500XL architecture may be viewed as a functional superset of the older Max7000A base architecture, and it provides more architectural flexibility, more logic resources, and higher level of quality and reliability for new leading edge 3.3V systems.