DataSource CD-ROM Q4-01

Xilinx Application Notes

Application Notes

- Summaries

Title	Size	Summary	Family	Design
Loadable Binary Counters	40 KB	XAPP004	XC3000	VIEWlogi OrCAD
Register Based FIFO	60 KB	XAPP005	XC3000	VIEWlogi OrCAD
Boundary Scan Emulator for XC3000	80 KB	XAPP007	XC3000	VIEWlogi OrCAD
Complex Digital Waveform Generator	10 KB	XAPP008	FPGAs	
Harmonic Frequency Synthesizer and FSK Modulator	20 KB	XAPP009	FPGAs	VIEWlogi OrCAD
Bus Structured Serial Input/Output Device	20 KB	XAPP010	XC4000	
LCA Speed Estimation: Asking the Right Question	10 KB	XAPP011	FPGAs	
Quadrature Phase Detector	20 KB	XAPP012	XC3000	
Using the Dedicated Carry Logic in XC4000E	100 KB	XAPP013	XC4000	
Ultra-Fast Synchronous Counters	40 KB	XAPP014	FPGAs	VIEWlogi OrCAD
Using the XC4000 Readback Capability	60 KB	XAPP015	XC4000	
Boundary Scan in XC4000/XC5200 Device v3.0 (11/99)	100 KB	XAPP017	XC4000 XC5200	
Estimating the Performance of XC4000E Adders and Counters	40 KB	XAPP018	XC4000	
Adders, Subtracters and Accumulators in XC3000	60 KB	XAPP022	XC3000	VIEWlogi OrCAD
Accelerating Loadable Counters in XC4000	30 KB	XAPP023	XC4000	VIEWlogi OrCAD
XC3000 Series Technical Information	110 KB	XAPP024	XC3000	
Multiplexers and Barrel Shifters in XC3000 Series	40 KB	XAPP026	XC3000	VIEWlogi OrCAD
Implementing State Machines in FPGA Devices	30 KB	XAPP027	FPGAs	
Frequency/Phase Comparator for Phase Locked Loops	40 KB	XAPP028	FPGAs	VIEWlogi OrCAD
Serial Code Conversion between BCD and Binary	20 KB	XAPP029	XC3000	VIEWlogi OrCAD

Title	Size	Summary	Family	Design
Megabit FIFO in Two Chips: One LCA Device and One DRAM	20 KB	XAPP030	XC3000	
Improving XC4000 Design Performance	160 KB	XAPP043	XC4000	
XC4000 Series Technical Information	30 KB	XAPP045	XC4000	
Synchronous and Asynchronous FIFO Designs	120 KB	XAPP051	XC4000	
Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators	70 KB	XAPP052	XC4000	
Implementing FIFOs in XC4000 Series RAM	220 KB	XAPP053	XC4000	VIEWlogi
Constant Coefficient Multipliers for the XC4000E	110 KB	XAPP054	XC4000	
Block Adaptive Filter	120 KB	XAPP055	XC4000	
System Design with New XC4000X I/O Features	70 KB	XAPP056	XC4000	
Using SelectRAM Memory in XC4000 Series FPGAs	140 KB	XAPP057	XC4000	
Xilinx In-System Programming Using an Embedded Microcontroller v3.0 (01/15/01)	590 KB	XAPP058	All	PC Solaris HP
Gate Count Capacity Metrics for FPGAs	80 KB	XAPP059	FPGAs	
Design Migration from XC4000 to XC5200	120 KB	XAPP060	XC4000 XC5200	
Design Migration from XC2000/XC3000 to XC5200	70 KB	XAPP061	XC2000 XC3000 XC5200	
Design Migration from XC4000 to XC4000E	60 KB	XAPP062	XC4000	
XC4000 Series Edge-Triggered and Dual-Port RAM Capability	50 KB	XAPP065	XC4000	
Using Serial Vector Format Files to Program XC9500 Devices In-System on Automatic Test Equipment and Third Party Tools	40 KB	XAPP067	XC9500	
In-System Programming Times	10 KB	XAPP068	XC9500	
Using the XC9500 JTAG Boundary Scan Interface	120 KB	XAPP069	XC9500	

Title	Size	Summary	Family	Design
Using In-System Programmability in Boundary Scan Systems	40 KB	XAPP070	XC9500	
Using the XC9500 Timing Model	60 KB	XAPP071	XC9500	
Designing with XC9500 CPLDs	100 KB	XAPP073	XC9500	
Pin Preassigning with XC9500 CPLDs	50 KB	XAPP074	XC9500	
Embedded Instrumentation Using XC9500 CPLDs	50 KB	XAPP076	XC9500	
XC9536 ISP Demo Board	50 KB	XAPP078	XC9500	ABEL VHDL
Configuring Xilinx FPGAs Using an XC9500 CPLD and Parallel PROM v1.1 (07/27/00)	100 KB	XAPP079	XC9500	
Supply Voltage Migration, 5 V to 3.3 V	30 KB	XAPP080	XC4000	
I/O Characteristics of the 'XL FPGAs	30 KB	XAPP088	Spartan XC4000	
FPGA Configuration Guidelines	60 KB	XAPP090	FPGAs	
Configuring Mixed FPGA Daisy Chains	20 KB	XAPP091	FPGAs	
Configuration Issues: Power-up, Volatility, Security, Battery Back-up	30 KB	XAPP092	FPGAs	
Dynamic Reconfiguration	20 KB	XAPP093	FPGAs	
Metastable Recovery	20 KB	XAPP094	FPGAs	

Set-up and Hold Times	10 KB	XAPP095	FPGAs	
Overshoot and Undershoot	10 KB	XAPP096	FPGAs	
Xilinx FPGAs: A Technical Overview for the First Time User	20 KB	XAPP097	FPGAs	
The Low-Cost, Efficient Serial Configuration of Spartan FPGAs	100 KB	XAPP098	Spartan	
Choosing a Xilinx Product Family	30 KB	XAPP100	All	
XC9500 Remote Field Upgrade	80 KB	XAPP102	XC9500	PC UNIX
The Tagalyzer - A JTAG Boundary Scan Debug Tool	130 KB	XAPP103	XC9500	
A Quick JTAG ISP Checklist	20 KB	XAPP104	XC9500	
A CPLD VHDL Introduction v2.0 (08/30/01) UPDATE!	333 KB	XAPP105	XC9500	
Synopsys/Xilinx High Density Design Methodology Using FPGA Compiler	240 KB	XAPP107	XC4000X	
Chip-Level HDL Simulation Using the Xilinx Alliance Series v2.0 (05/22/00)	165 KB	XAPP108	FPGAs	
Hints, Tips and Tricks for Using XABEL with Xilinx M1.5 Design and Implementation Tools	80 KB	XAPP109	All	
XC9500 CPLD Power Sequencing	30 KB	XAPP110	XC9500	
Using the XC9500XL Timing Model v1.3 (08/20/01) UPDATE!	72 KB	XAPP111	XC9500XL	
Designing With XC9500XL CPLDs	160 KB	XAPP112	XC9500XL	
Faster Erase Times for XC95216 and XC95108 Devices on HP 3070 Series Testers	30 KB	XAPP113	XC9500	
Understanding XC9500XL CPLD Power	90 KB	XAPP114	XC9500XL	
Planning for High Speed XC9500XL Designs	100 KB	XAPP115	XC9500XL	
Adapting ASIC Designs for Use with Spartan FPGAs	50 KB	XAPP119	Spartan	
How Spartan FPGAs -- The Gate Array Solution	87 KB	XAPP120	Spartan	
The Express Configuration of Spartan-XL FPGAs (v3.0) 4/19/01	141 KB	XAPP122	Spartan-XL	
Using Three-State Enable Registers in XLA, XV, and Spartan-XL FPGAs	40 KB	XAPP123	XC4000XLA XC4000XV Spartan-XL	PC UNIX
Using Manual Power Down Mode With Spartan-XL FPGAs	20 KB	XAPP124	Spartan-XL	
Conserving Power With Auto Power Down Mode in Spartan-XL FPGAs	20 KB	XAPP125	Spartan-XL	
Data Generation and Configuration for Spartan Series FPGAs	80 KB	XAPP126	Spartan	

Title	Size	Summary	Family	Design
Using the Virtex Block SelectRAM+ Features v1.4 (12/18/00)	95 KB	XAPP130	Virtex	
170 MHz FIFOs Using the Virtex Block SelectRAM+ Feature v1.5 (06/06/01)	75 KB	XAPP131	Virtex	PC UNIX
Using the Virtex Delay-Locked Loop v2.3 (09/20/00)	90 KB	XAPP132	Virtex	
Using the Virtex SelectI/O Resource v2.4 (04/17/00)	230 KB	XAPP133	Virtex	
Virtex Synthesizable High Performance SDRAM Controller v3.1 (02/01/00)	105 KB	XAPP134	Virtex	PC:VHDL PC:Verilog UNIX:VHDL UNIX:Verilo

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Virtex I/V Curves for Various Output Options	20 KB	XAPP135	Virtex	
Synthesizable 143 MHz ZBT SRAMInterface v2.0 (01/00)	90 KB	XAPP136	Virtex	PC UNIX
Configuring Virtex FPGAs from Parallel EPROMs with a CPLD	90 KB	XAPP137	Virtex XC9500	PC
Virtex Configuration and Readback v2.4 (07/25/01)	533 KB	XAPP138	Virtex	
Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary-Scan v1.2 (2/00)	88 KB	XAPP139	Virtex/-E	
In-System Programming Times for XC9500XL	10 KB	XAPP141	XC9500XL	
Designing CPLD Multi-voltage Systems v1.3 (03/00)	65 KB	XAPP144	CPLD	
Designing an Eight Channel Digital Volt Meter with the Insight Springboard Kit (v1.0) 4/30/01	58 KB	XAPP146	CoolRunner CPLD	
Low Power Handspring Springboard Module Design with CoolRunner CPLDs (v1.0) 1/25/01	56 KB	XAPP147	CoolRunner CPLD	
I/V Curves for Various Device Families	20 KB	XAPP150	All	
Virtex Series Configuration Architecture User Guide v1.4 (08/03/00)	245 KB	XAPP151	Virtex	
Virtex Power Estimator User Guide v1.1 (2/00)	90 KB	XAPP152	Virtex	worksheet
Status and Control Semaphore Registers Using Partial Reconfiguration	180 KB	XAPP153	Virtex	PC
Virtex Synthesizable Delta-Sigma DAC	60 KB	XAPP154	Virtex	
Virtex Analog to Digital Converter	50 KB	XAPP155	Virtex	
Board Routability Guidelines with Xilinx Fine-Pitch BGA Packages v1.0 (07/26/00)	1,800 KB	XAPP157	Virtex	
Powering Virtex FPGAs v1.4 (02/06/01)	70 KB	XAPP158	Virtex	
XC1700 and XC18V00 Design Migration Considerations	60 KB	XAPP161	XC1700E/L, XC1800	
Using Xilinx and Synplify for Incremental Designing (ECO)	40 KB	XAPP164	FPGA	PC UNIX
Using Xilinx and Exemplar for Incremental Designing (ECO)	70 KB	XAPP165	FPGA	PC UNIX
TAU/BLAST Support in 2.1i	20 KB	XAPP166	FPGA	
Getting Started With the MultiLINX Cable v1.2 (04/20/00)	180 KB	XAPP168	FPGA	
MP3 NG: A Next Generation Consumer Platform v1.0 (01/00)	360 KB	XAPP169	Spartan-II	
Implementing an ISDN PCMCIA Modem Using Spartan Devices v1.0 (7/99)		XAPP170	Spartan	
Implementing an ADSL to USB Interface Using Spartan Devices v1.0 (3/99)		XAPP171	Spartan	
The Design of a Video Capture Board Using the Spartan Series v1.0 (3/99)		XAPP172	Spartan	
Using Block SelectRAM+ Memory in Spartan-II FPGAs v1.1 (12/11/00)	100 KB	XAPP173	Spartan-II	
Using Delay-Locked Loops in Spartan-II FPGAs v1.0 (01/00)	120 KB	XAPP174	Spartan-II	PC UNIX
High Speed FIFOs In Spartan-II FPGAs v1.0 (01/00)	50 KB	XAPP175	Spartan-II	PC UNIX
Spartan-II FPGA Family Configuration and Readback v1.0 (01/00)	400 KB	XAPP176	Spartan-II	

DataSource CD-ROM Q4-01: Application Notes (continued)

Spartan-Family I/V Curves for Various Output Options v1.0 (01/00)	30 KB	XAPP177	Spartan-II	
Configuring Spartan-II FPGAs from Parallel EPROMs v1.0 (01/00)	100 KB	XAPP178	Spartan-II	PC
Using SelectI/O Interfaces in Spartan-II FPGAs v1.0 (01/00)	300 KB	XAPP179	Spartan-II	
SEU Mitigation Design Techniques for the XQR4000XL v1.0 (03/15/00)	105 KB	XAPP181	FPGA	
Configuration and Readback of Spartan-II FPGAs Using Boundary Scan (v2.0) 4/19/01	166 KB	XAPP188	Spartan-II	
Powering Xilinx Spartan-II FPGAs v1.1 (07/20/01)	78 KB	XAPP189	Spartan-II	
Interfacing a Virtex-E Device to a MIPS Processor v1.0 (12/15/00)	100 KB	XAPP192	Virtex	
Interfacing a Virtex-E Device to a Pentium Processor v1.0 (12/15/00)	70 KB	XAPP196	Virtex	
Synthesizable FPGA Interface for Retrieving ROM Number from 1-Wire Devices v1.0 (05/08/01)	165 KB	XAPP198	Virtex, Spartan-II	
Writing Efficient Testbenches v1.0 (06/18/01)	279 KB	XAPP199	Test Benches	PC UNIX
Virtex Synthesizable 1.6 Gbytes/s DDR SDRAM Controller v2.3 (03/21/00)	105 KB	XAPP200	Virtex	PC
An Overview of Multiple CAM Designs in Virtex Devices	40 KB	XAPP201	Virtex	
Content Addressable Memory (CAM) in ATM Applications v1.2 (01/06/01)	140 KB	XAPP202	Virtex, Virtex-II	PC
Designing Flexible, Fast CAMs with Virtex Slices	100 KB	XAPP203	Virtex	PC UNIX
Using Block RAM for High-Performance Read/Write CAMs v1.2 (05/02/00)	100 KB	XAPP204	Virtex	
Data-Width Conversion FIFOs Using the Virtex Block SelectRAM Memory v1.3 (08/10/00)	50 KB	XAPP205	Virtex	
An Inverse Discrete Cosine Transform (IDCT) Implementation in Virtex Devices for MPEG Video Applications v1.1 (01/00)	40 KB	XAPP208	Virtex	design
IEEE 802.3 Cyclic Redundancy Check v1.0 (03/23/01)	120 KB	XAPP209	Virtex-II	
Linear Feedback Shift Registers in Virtex Devices v1.2 (01/09/01)	85 KB	XAPP210	Virtex, Virtex-II	
PN Generators Using the SRL Macro v1.1 (01/09/01)	120 KB	XAPP211	Virtex, Virtex-II, Spartan-II	
CDMA Matched Filter Implementation in Virtex Devices v1.1 (01/10/01)	170 KB	XAPP212	Virtex, Virtex-II, Spartan-II	
8-Bit Microcontroller for Virtex Devices v1.0 (09/25/00)	380 KB	XAPP213	Virtex, Spartan-II	
Design Tips for HDL Implementation of Arithmetic Functions v1.0 (06/28/00)	78KB	XAPP215	Virtex	
Correcting Single-Event Upsets Through Virtex Partial Configuration v1.0 (06/01/00)	110 KB	XAPP216	Virtex	
Gold Code Generators in Virtex Devices v1.1 (01/10/01)	125 KB	XAPP217	Virtex, Virtex-II, Spartan-II	
Transposed Form FIR Filters v1.1 (01/10/01)	150 KB	XAPP219	Virtex, Virtex-II	
LFSRs as Functional Blocks in Wireless	135 KB	XAPP220	Virtex, Virtex-II,	

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200 MHz UART with Internal 16-Byte Buffer v1.1 (07/10/01)	150 KB	XAPP223	Virtex, Virtex-II, Spartan-II	
Data Recovery in Virtex and Virtex-II Devices v1.1 (01/10/01)	60 KB	XAPP224	Virtex, Virtex-II	
Data to Clock Phase Alignment v1.0 (09/18/01) NEW!	48 KB	XAPP225	Virtex Series	
The LVDS I/O Standard	70 KB	XAPP230	Virtex-E	
Multi-Drop LVDS with Virtex-E FPGAs	85 KB	XAPP231	Virtex-E	
Virtex-E LVDS Drivers & Receivers: Interface Guidelines v1.0 (11/99)	85 KB	XAPP232	Virtex-E	
Multi-Channel 622 Mb/s LVDS Data Transfer for Virtex-E Devices v1.2 (01/06/01)	260 KB	XAPP233	Virtex-E	
Virtex SelectLink Communications Channel v1.0 (12/99)	25 KB	XAPP234	Virtex-E	
Virtex Package Compatibility Guide v1.3 (06/20/00)	40 KB	XAPP235	Virtex	
LVDS System Data Framing v1.0 (12/18/00)	80 KB	XAPP238	Virtex-E	
High-Speed Buffered Crossbar Switch Design Using Virtex-EM Devices v1.0 (03/14/00)	80 KB	XAPP240	Virtex-EM	
Virtex-EM FIR Filter for Video Applications v1.0 (03/14/00)	60 KB	XAPP241	Virtex-EM	
Interfacing to Lara Networks Search Engine Using Virtex Devices v1.0 (06/08/00)	80 KB	XAPP242	Virtex-EM	
Eight Channel, One Clock, One Frame LVDS Transmitter/Receivere v1.0 (03/02/01)	148 KB	XAPP245	Virtex-E	
PowerPC 60X Bus Interface to a Virtex-E Device v1.0 (12/15/00)	165 KB	XAPP246	Virtex-E	PC
Hot-Swapping Virtex-II Devices v1.1 (08/15/01) UPDATE!	65 KB	XAPP251	Virtex-II	
Synthesizable 266 MBits/s DDR SDRAM Controller v1.0 (01/12/01)	155 KB	XAPP253	Virtex-II	
The Virtex-II SiberBridge v1.0 (01/12/01)	120 KB	XAPP254	Virtex-II	
FIFOs Using Virtex-II Shift Registers v1.0 (01/15/01)	50 KB	XAPP256	Virtex-II	
FIFOs Using Virtex-II Block RAM v1.2 (06/05/01)	60 KB	XAPP258	Virtex-II	
Data-Width Conversion FIFOs Using the Virtex-II Block RAM Memory v1.0 (01/10/01)	80 KB	XAPP261	Virtex-II	
Quad DataRate (QDR) SRAM Interface for Virtex-II Devices v1.0 (01/15/01)	80 KB	XAPP262	Virtex-II	
Parity Generation and Validation in Virtex-II Devices v1.0 (01/15/01)	45 KB	XAPP267	Virtex-II	
High-Speed DES and Triple DES Encryptor/Decryptor v1.0 (10/01/01) NEW!	151 KB	XAPP270	Virtex-II	
Color Space Converter v1.0 (07/11/01)	110 KB	XAPP283	Virtex-II	PC
3 x 3 Matrix Multiplier for 3D Graphics and Video v1.0 (07/11/01)&	75 KB	XAPP284	Virtex-II	PC
Common Switch Interface CSIX-L1 Reference Design v1.0 (08/10/01) NEW!	88 KB	XAPP289	Virtex-II	

DataSource CD-ROM Q4-01: Application Notes (continued)

Title	Size	Summary	Family	Desig
In-System Programming (ISP)	80 KB	XAPP300	CoolRunner	
Power Up Reset Characteristics of CoolRunner CPLDs v1.1 (12/00)	30 KB	XAPP310	CoolRunner	
Five Volt Tolerance and PCI v1.1 (2/00)	70 KB	XAPP311	CoolRunner	
Differences In ABEL and PHDL v1.0 11/99)	60 KB	XAPP312	CoolRunner	
Design of an MP3 Portable Player Using a CoolRunner CPLD v1.1 (12/99) >	450 KB	XAPP328	CoolRunner	
Understanding True CMOS Outputs v1.0 (02/00)	90 KB	XAPP329	CoolRunner	
Pin Locking in CoolRunner XPLA3 CPLDs v1.0 (01/07/00)	80 KB	XAPP332	CoolRunner	
CoolRunner XPLA3 I^2C Bus Controller Implementation v1.4 (07/21/00)	170 KB	XAPP333	CoolRunner	
Utilizing XPLA3 Universal Control Terms v1.0 (01/19/00)	65 KB	XAPP334	CoolRunner	
Macrocell Configurations in CoolRunner XPLA3 CPLDs v1.0 (04/17/00)	100 KB	XAPP335	CoolRunner	
Design of a 16b/20b Encoder/Decoder Using a CoolRunner CPLD v1.0 (07/15/00)	280 KB	XAPP336	CoolRunner	
Using Xilinx WebPACK and ModelTech ModelSim Xilinx Edition (MXE) v1.0 (04/12/00)	2,360 KB	XAPP338	CoolRunner	
Manchester Encoder-Decoder for Xilinx CPLDs v1.1 (04/17/00)	60 KB	XAPP339	CoolRunner	
UARTs in Xilinx CPLDs v1.2 (11/28/00)	35 KB	XAPP341	CoolRunner	
XPLA3 I/O Cell Characteristics v1.0 (04/06/01)	58 KB	XAPP342	CoolRunner	
In-System Programming of XPLA3 Devices v1.0 (08/30/00)	60 KB	XAPP343	CoolRunner	
IrDA and UART Design in a CoolRunner CPLD v1.0 (08/08/01) NEW!	132 KB	XAPP345	CoolRunner	
Low Power Tips for CoolRunner Design v1.0 (10/16/00)	285 KB	XAPP346	CoolRunner	
Decrease Processor Power Consumption Using a CoolRunner CPLD v1.0 (06/01/01)	82 KB	XAPP347	CoolRunner	
CoolRunner XPLA3 Serial Peripheral Interface Master v1.0 (11/29/00)	215 KB	XAPP348	CoolRunner	
CoolRunner CPLD 8051 Microcontroller Interface v1.0 (12/07/00)	105 KB	XAPP349	CoolRunner	
Implementing HDL with WebPACK ECS Schematic Editor v1.0 (12/20/00)	265 KB	XAPP350	CoolRunner	
The CoolRunner CPLD IRL Demo: An Example of Using the Internet to Configure a CoolRunner CPLD v1.0 (11/07/00)	557 KB	XAPP351	CoolRunner	
Utilizing a User Constraint File for CoolRunner CPLDs v1.0 (06/20/01)>	121 KB	XAPP352	CoolRunner	
CoolRunner XPLA3 SMBus Controller Implementation v1.0 (02/14/01)	179 KB	XAPP353	CoolRunner	
Using Xilinx CPLDs to Interface to a NAND Flash Memory Device v1.0 (08/30/01) NEW!	520 KB	XAPP354	CoolRunner	
Serial ADC Interface Using a CoolRunner CPLD v1.0 (04/30/01)	320 KB	XAPP355	CoolRunner	
CoolRunner Visor Springboard LED Test v1.1 (06/25/01)	320 KB	XAPP357	CoolRunner	
Understanding the Insight Springboard Development Kit v1.0 (04/30/01)	38 KB	XAPP359	CoolRunner	
Using the XC9500XV Timing Model v1.0 (08/20/01) NEW!	72 KB	XAPP362	XC9500XV CPLD	

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Constraining Virtex Design in 2.1i v1.0 (10/01/99)	125 KB	XAPP400	Virtex	
2.1i FPGA Editor v1.0 (10/13/99)>	60 KB	XAPP401	Virtex	
2.1i Floorplanner Support for Virtex FPGAs v1.0 (10/13/99)	530 KB	XAPP402	Virtex	
Using the Version 2.1i Xilinx Design Manager and Flow Engine (DMFE) v1.0 (09/27/99)	170 KB	XAPP403	Virtex	
Xilinx Alliance 3.1i Modular Design v1.2 (04/20/01)	690 KB	XAPP404	Virtex	
Cross Probing to Synplicity and Exemplar v2.0 (12/01/00)	325 KB	XAPP406	FPGA	
Rethinking Your Verification Strategies for Multimillion-Gate FPGAs v1.0 (10/07/00)	140 KB	XAPP408	FPGAs	
Simulating a Xilinx 3.1i CORE Generator VHDL Design v1.0 (06/18/01)	185 KB	XAPP409	FPGAs	
Simulating a Xilinx 3.1i CORE Generator Verilog Design v1.0 (06/18/01)	138 KB	XAPP410	FPGAs	
Architecting Systems for Upgradability with IRL (Internet Reconfigurable Logic) v1.0 (06/29/01)	150 KB	XAPP412	FPGA	
J Drive: In-System Programming of IEEE Standard 1532 Devices v1.1 (01/17/01)	150 KB	XAPP500	Virtex	
Configuration Quick Start Guidelines v1.2 (08/02/01) NEW!	360 KB	XAPP501	All	
Using a Microprocessor to Configure Xilinx FPGAs via Slave Serial or SelectMAP Mode v1.1 (01/08/02) NEW!	175 KB	XAPP502	FPGAs	
XGMII Using the DDR Registers, DCM, and SelectI/O Features in Virtex-II Devices v1.0 (10/23/01)	125 KB	XAPP606	Virtex-II	