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# High-Speed Transceiver Logic (HSTL)

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HSTL is a technology-independent interface standard for digital integrated circuits. It is a JEDEC standard developed for voltage scalable and technology independent I/O structures. The I/O structures required by this standard are differential amplifier inputs (with one input internally tied to a user-supplied input reference voltage, $V_{REF}$ for single-ended inputs) and outputs using output power supply inputs ($V_{CCO}$) that may differ from those operating the device itself.

Although the JEDEC specification states the maximum value of $V_{CCO}$ as 1.6V, several chip manufacturers with HSTL I/O standard require a $V_{CCO}$ of 1.8V. This results in $V_{REF}$ and $V_{TT}$ values having to track this higher $V_{CCO}$ value. As per the EIA/JESD8-6 specification, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

In order for Virtex™ devices to interface to chips with $V_{CCO}$ of 1.8V for HSTL, they have to be provided with the $V_{CCO}$, $V_{REF}$, and $V_{TT}$ values specified in the following sections.

# HSTL Voltage Specifications ($V_{CCO}$ of 1.8 V)

## HSTL Class I for Virtex, Virtex-E, and Virtex-II Devices

| Parameter | Minimum | Typical | Maximum |
|---|---|---|---|
| $V_{CCO}$ | 1.7 | 1.8 | 1.9 |
| $V_{REF}$ | 0.83 | 0.90 | 1.1 |
| $V_{TT}$ | - | $V_{CCO}$ x 0.5 | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

## HSTL Class II for Virtex-II Devices

| Parameter | Minimum | Typical | Maximum |
|---|---|---|---|
| $V_{CCO}$ | 1.7 | 1.8 | 1.9 |
| $V_{REF}$ | 0.83 | 0.90 | 1.1 |
| $V_{TT}$ | - | $V_{CCO}$ x 0.5 | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –16 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 16 | - | - |

## HSTL Class III for Virtex, Virtex-E, Virtex-II Devices

| Parameter | Minimum | Typical | Maximum |
|---|---|---|---|
| $V_{CCO}$ | 1.7 | 1.8 | 1.9 |
| $V_{REF}$ | - | 1.1 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

## HSTL Class IV for Virtex, Virtex-E, Virtex-II Devices

| Parameter | Minimum | Typical | Maximum |
|---|---|---|---|
| $V_{CCO}$ | 1.7 | 1.8 | 1.9 |
| $V_{REF}$ | - | 1.1 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 (for Virtex / Virtex-E devices)<br>48 (for Virtex-II devices) | - | - |

## Virtex Devices

1. Outputs will be noisier with HSTL at 1.8V, hence, the recommended number of Simultaneously Switching Outputs (SSOs) in the guidelines for the Virtex devices must be reduced by 25 percent. Therefore, 25 percent fewer outputs should be switching per power / ground pair for HSTL at 1.8V versus HSTL at 1.5V.
2. The user must select a $V_{REF}$ value based on the DC voltage specification that provides optimum noise margin.
3. In Virtex devices, different input buffers are used for $V_{REF}$ < 1V and $V_{REF}$ > 1V. Hence, users must specify an I / O standard that has a $V_{REF}$ greater than 1V when

using HSTL Class III or IV at 1.8V. For example, the user can specify in software SSTL2 Class I or II as the I/O standard.

4. Based on HSPICE simulation, the timing parameters for HSTL Class I, Class III, and Class IV at 1.8V are 200 ps slower versus HSTL Class I, Class III, and Class IV at 1.5V. Hence, the user must add 200 ps to the delays reported by software for HSTL at 1.8V versus 1.5V. After silicon characterization, this delay factor (200 ps) could be revised in future.
5. IBIS models for HSTL at 1.8V are not currently available. They are being generated.

### Virtex-E Devices

1. Outputs will be noisier with HSTL at 1.8V, hence, the recommended number of SSOs in the guidelines for the Virtex-E device must be reduced by 25 percent. Therefore, 25 percent fewer outputs should be switching per power/ground pair for HSTL at 1.8V versus HSTL at 1.5V.
2. The user must select a $V_{REF}$ value based on the DC voltage specification that provides optimum noise margin.
3. In Virtex-E devices, the same input buffers are used for $V_{REF} < 1V$ and $V_{REF} > 1V$. Therefore, in software, just specify the HSTL Class required.
4. Based on HSPICE simulation, the timing parameters for HSTL Class I, Class III, and Class IV at 1.8V are 200 ps slower versus HSTL Class I, Class III, and Class IV at 1.5V. Hence, the user must add 200 ps to the delays reported by software for HSTL at 1.8V versus 1.5V. After silicon characterization, this delay factor (200 ps) could be revised in future.
5. IBIS models for HSTL at 1.8V are not currently available. They are being generated.

### Virtex-II Devices

1. The number of SSOs for a Virtex-II device with HSTL at 1.8V are the same as the provided guidelines.
2. The user must select a $V_{REF}$ value based on the DC voltage specification that provides optimum noise margin.
3. In Virtex-II devices, the input buffers are the same for all HSTL Classes whether 1.5V or 1.8V. Therefore, in software, just specify the HSTL Class required and whether Digital Controlled Impedance (DCI) or non-DCI.
4. The timing parameters for HSTL at 1.8V are available in the Virtex-II data sheet.
5. IBIS models for HSTL at 1.8V are currently available.

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 01/02/02 | 1.0 | Initial Xilinx release. |