XAPP359 (v1.0) July 11, 2001

Understanding the Insight Springboard Development Kit

Summary

The Insight Springboard™ Development Card is designed such that the Xilinx CoolRunner™ CPLD serves as the central interface between the Handspring Visor™'s Springboard expansion slot and all other external devices (Flash, SRAM, and A/D Converter): see Figure 1. This means the CoolRunner is the only integrated circuit physically attached to the Springboard bus. The other components, namely the Flash, A/D, and SRAM, are also connected to the CoolRunner, but they do not have their data, address, and control lines connected directly to the Springboard expansion slot. Such a scheme is advantageous, but Springboard designers must be careful in order to avoid common pitfalls. This Application Note explains why such a design is preferable and will explain how to avoid common mistakes.

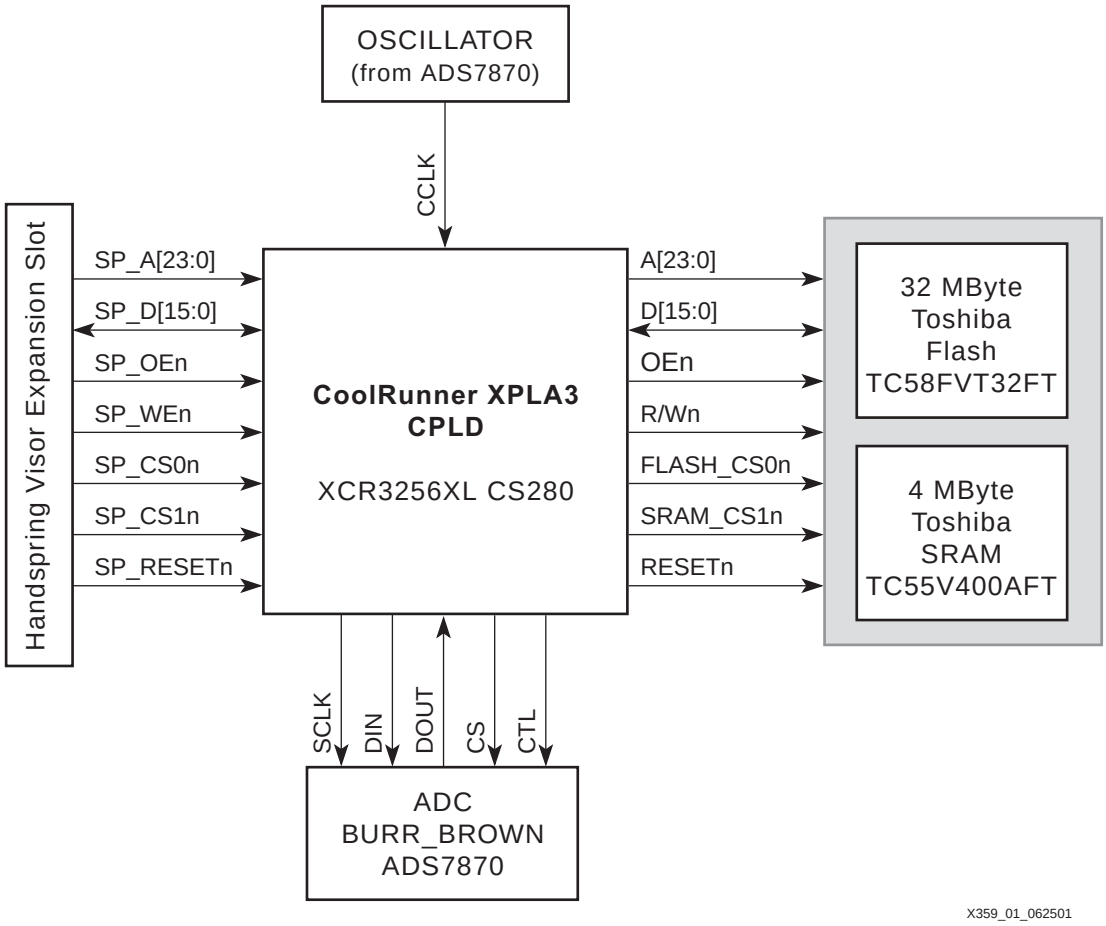

Figure 1: **Insight Electronics Springboard Block Diagram**

Benefits of a Central Interface

The Insight Springboard Development Kit provides Springboard developers with additional memory (Flash and SRAM) and an A/D Converter. The CoolRunner CPLD serves as the central interface between these external peripherals and the Motorola Dragonball Processor. The following section will describe the motivation behind such a design.

Flash Memory

For Springboard designs, flash is required for the Plug and Play aspect. It is used to store the module's application. Most Springboard designs use the on-board flash memory solely to store module applications. In this scenario, flash memory may be directly connected to the Springboard bus.

However, the Insight Springboard Development Kit was designed with maximum flexibility in mind. We wanted to provide a reasonably sized flash memory such that designers would be allowed to store other data on top of the module's application data, should they choose. Connecting the flash memory to a programmable logic device provides this flexibility. If designers have no other use for non-volatile flash memory other than to store the module's application, they can still retain that functionality through the XPLA3™ CPLD.

It is in the second case where the true advantage of connecting the flash to the CPLD can be seen. Suppose that a designer wants to store additional, non-module, application-related data in the non-volatile flash memory. This would still be possible if the flash were connected to directly to the Springboard signals. However, the Dragonball processors in the Handspring Visors typically have a very slow access times. By connecting the flash to the XPLA3, we take advantage of the faster hardware, and we can use the CoolRunner CPLD to access and manipulate the data at a faster rate. Therefore, all the high-speed data manipulation can be done in hardware and the Dragonball processor can be freed to do other tasks.

SRAM

The motivation for connecting the SRAM to the CoolRunner XPLA3 CPLD is similar to that of the Flash memory. First, the CoolRunner can access and manipulate data at a much higher rate than the Visor. Second, connecting the SRAM to the CoolRunner provides a direct path for data from external hardware (i.e. a parallel A/D Converter) to be stored in memory. If the SRAM were connected directly to the Springboard bus, the Visor would have to read data from external hardware and then write this data to the SRAM. Many bus cycles are saved by using the CoolRunner CPLD in this manner.

The Digital Voltmeter and the Oscilloscope reference designs, described in **XAPP146** and **XAPP149** respectively, utilize this concept.

A/D Converter

The Texas Instruments ADS7870 Data Aquisition System has a serial interface which requires a shift clock and serial data to be avaible on a rising or falling edge of the shift clock. The Springboard interface does not provide a serial interface, and therefore may not be directly connected to the ADS7870. Connecting the ADS7870 to the CPLD is the only solution. The CoolRunner can then be easily used to control, serialize, and/or deserialize data to/from the ADS7870.

The ADS7870 Interface, described in XAPP355, can be easily customized and ported to any Springboard design.

Pitfalls

SRAM and Flash Memory

Neither the SRAM nor the Flash memory is connected to the Springboard bus; both are instead connected to the CoolRunner CPLD. As a result, the designer must ensure that the Visor is allowed access to both the SRAM and Flash. This means that the CoolRunner CPLD must be programmed accordingly.

XAPP147 describes the basic functionality that will allow the Visor to interact with the Flash and SRAM. The "SRAM Test.vhd" program distributed along with XAPP147 will allow the Visor to do this. At the same time, when the CoolRunner CPLD is programmed with this file, all signals originating from the Springboard expansion area are available via the expansion connectors located on the user prototype section of the Insight Springboard Development Card. The plug

and play aspect of Springboard modules will also be retained in this case, as the Visor will be allowed to read and execute code stored within the Flash memory.

The SRAM Test program can be used as a utility for basic debugging purposes. SRAM Test makes the CPLD virtually transparent. It simply buffers all signals originating from the Visor through the CoolRunner and then routes those signals to the SRAM, Flash, and user expansion area. Therefore, the SRAM Test program can be utilized as the top level file for any future Springboard design.

The Visor will never be able to access SRAM and/or Flash memory if the XPLA3 CPLD does not grant the Visor access. If a designer needs to access memory, he must make sure that his program implements a proper buffering scheme such as the one illustrated in the SRAM Test program (Figure 2). Note that more complex designs require more logic. The scheme in Figure 2 will need to be modified accordingly for more advanced designs.

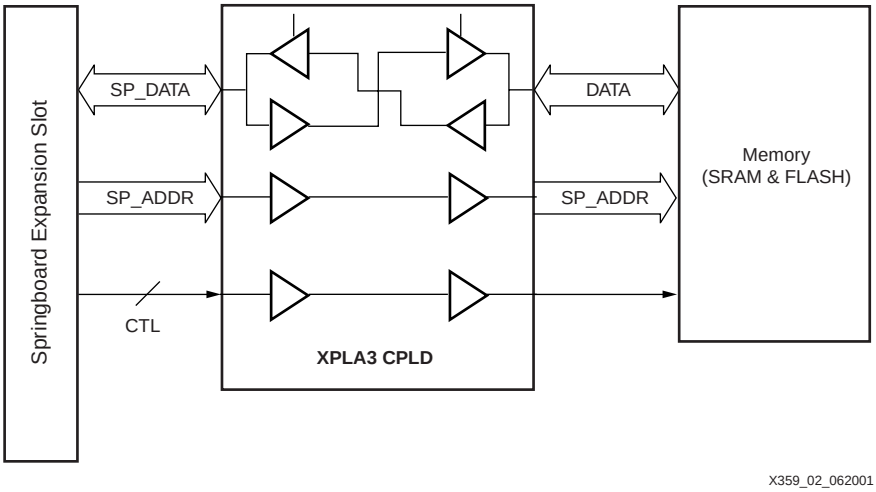

Figure 2: **SRAM Test Program**

User Expansion Area

Much like the memory, the signals that are accessible through the user expansion area also originate from the CoolRunner CPLD. Again, the SRAM Test program will route the Springboard address, data, and control signals to the user area.

If additional control signals, such as Chip Select 0 (CS0) and Chip Select 1 (CS1) need to be accessed on the user expansion area, the CoolRunner CPLD can route these signals to any user I/O pin. This is the beauty and flexibility of programmable logic.

Conclusion

When used correctly, the CoolRunner XPLA3 Programmable Logic Device will enable designers to rapidly prototype designs on the Insight Springboard Development Kit. The CoolRunner CPLD family is the only re-programmable, ultra-low power solution that can meet Springboard power requirements and at the same time, provide a wide option of small packages needed by space-contrained Springboard modules. With logic densities ranging from 32 to 512 macrocells, and speeds ranging from 6 ns to 12 ns, the CoolRunner can be used as a single chip solution for all digital logic functions.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/11/01	1.0	Initial Xilinx release.