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Power-On Requirements for the Spartan-II and Spartan-IIE Families

Author: Kim Goldblatt

Summary

Spartan™-II and Spartan-IIE Field Programmable Gate Arrays require a minimum supply current in order to power on. This application note begins by explaining the nature of the Power-On Surge (POS) current. It then considers the implications of the power-on current specifications as published in the Spartan-II and Spartan-IIE data sheets. Next is an explanation of the major factors that influence the POS current. Sections discussing board-level considerations and regulator selection follow. The last section introduces an approach to FPGA power-on in the presence of an over-current protection circuit.

Introduction

All Field Programmable Gate Arrays (FPGAs) require a minimum supply current to ensure a successful power up. This Power-On Surge (POS) current is specified in the Spartan-II data sheet as I_{CCPO}. The size of this current requirement varies according to the FPGA family. High performance FPGAs can require relatively high levels of POS current. The Spartan-II family requires 500 mA min. for junction temperatures above 0°C and 2A min. below 0°C. The Spartan-IIE family requires 500 mA min. for commercial devices and 2A min. for industrial devices.

While these requirements represent a significant amount of current, they apply for only a short period of time (usually on the order of milliseconds). It is important to note that many power supplies have no difficulty meeting the specifications, since they are capable of providing significantly more current on an instantaneous basis than they are rated for in terms of continuous output. Nevertheless, some designs with strict supply current budgets will require the FPGA to power-on with a current significantly less than that required in the specification. For these cases, a number of low-cost, simple capacitor-based solutions are presented in application note **XAPP451, "Power Assist Circuits for the Spartan-II and Spartan-IIE Families"**.

The Nature of the POS Current

The Power-On Surge is the current that an FPGA draws upon first applying power. It is a fundamental result of this device's RAM-based nature. FPGAs are programmed by storing configuration data in RAM cells that switch interconnect pathways. When the FPGA powers up, but before initialization, the RAM cells are briefly in a random state, which results in normal contention at the interconnect. It is this normal contention that accounts for the POS current draw during power-on.

The power-on current can be significant for high performance FPGAs, such as those of the Spartan-II and Spartan-IIE families, particularly since they employ extensive buffering for fast signal switching and propagation. During power-up, this buffering creates additional current paths between power and ground.

For the Spartan-II and Spartan-IIE families, the POS current is the total I_{CCINT} current entering all V_{CCINT} pins when power is applied. For both product families, the POS current occurs when V_{CCINT} is roughly between a 0.6V to 0.8V range, just as the transistors on the die are beginning to power on.

During this POS period, the FPGA can be modeled as a very low impedance element (typically 0.3Ω to 6.0Ω). Once power is applied to the FPGA, V_{CCINT} begins to ramp up. When V_{CCINT} reaches the lower voltage of the aforementioned range, the user can expect to see significant I_{CCINT} current draw. By the time V_{CCINT} reaches 0.8V, I_{CCINT} has fallen to its standby level

(typically between 10 mA and 15 mA for Spartan-II devices) and V_{CCINT} continues on to the nominal operating level (2.5V for the Spartan-II family and 1.8V for the Spartan-IIE family).

A core power-voltage level of V_{CCINT} min. (2.38V for the Spartan-II family and 1.71V for the Spartan-IIE family) is necessary and sufficient to confirm a successful power-up. As an alternative criterion, check for a Low-to-High transition on the $\overline{INIT}$ line.

Spartan-II Power-On Specification Summary

Xilinx publishes a power-on current specification (I_{CCPO}) in the data sheets of all FPGAs requiring significant power-on current. The Spartan-II data sheet specifies the POS current in the "Supply Current Requirements During Power-On" section of Module 3, which guarantees a successful power-on only if the following conditions are met:

1. The power supply must provide a minimum I_{CCINT} current of 500 mA for each Spartan-II FPGA (commercial or industrial) operating over a junction temperature range from 0°C to 100°C. The supply must source 2A minimum for each industrial FPGA only when the junction temperature can drop below 0°C.
2. The V_{CCINT} rise time is less than 50 ms.
3. V_{CCINT} rises steadily from GND to 2.5V (no negative dips in the voltage).

These specifications and recommendations are discussed in the sections that follow.

Spartan-IIE Power-On Specification Summary

The POS specification in the Spartan-IIE data sheet guarantees successful power-on when the following conditions are met:

1. The power supply must provide at least 500 mA of I_{CCINT} current for each commercial Spartan-IIE FPGA. The minimum I_{CCINT} current for each industrial Spartan-IIE FPGA is 2A.
2. The V_{CCINT} rise time is between 2 ms and 50 ms.
3. V_{CCINT} rises steadily from GND to 1.8V (no negative dips in the voltage).

Furthermore, it is important to apply power to V_{CCO} and V_{CCINT} at the same time.

These specifications and recommendations are discussed in the following sections.

The Minimum POS Current Requirement

IC power current specifications are usually thought of as maximum values; however, this is not the case for I_{CCPO}. It is important to recognize that I_{CCPO} is a minimum specification. For either a Spartan-II FPGA operating over a junction temperature greater than 0°C or a commercial Spartan-IIE FPGA, it is necessary and sufficient to supply at least 500 mA in order to have a guaranteed successful power-on. If this amount of current is not available, then V_{CCINT} may hang at an intermediate level, but never reach the recommended operating level for V_{CCINT} (2.5V for Spartan-II devices and 1.8V for Spartan-IIE devices). For Spartan-II applications operating at junction temperatures below 0°C, one can expect similar behavior if the 2A minimum specification is not met.

The minimum POS current requirement for Spartan-II and Spartan-IIE devices only applies while V_{CCINT} ramps from GND to its minimum recommended operating level (2.38V for Spartan-II devices and 1.71V for Spartan-IIE devices). The POS current typically occurs when V_{CCINT} is between 0.6V and 0.8V. It usually lasts only a few milliseconds. Accordingly, the POS current is more instantaneous than continuous. For this reason, when selecting a power-supply or regulator, one should consider its ability to source instantaneous as opposed to continuous current.

In order to charge up board capacitance efficiently when power is first applied, supplies are commonly designed to provide much more current instantaneously than they are rated for in terms of continuous output. It follows that for the majority of designs, the chosen power source will be able to meet the minimum I_{CCPO} requirement with no additional components required. Nevertheless, for special designs with stringent supply requirements, it is possible to power-up

Spartan-II FPGAs with less current than I_{CPPO} min. simply by adding a large capacitor. For details on this and related solutions, see application note **XAPP451, "Power Assist Circuits for the Spartan-II and Spartan-IIE Families"**.

The Maximum POS Current

A maximum limit for I_{CCPO} is not specified in the Spartan-II and Spartan-IIE data sheets. The upper bound on the size of the surge is determined by the amount of supply current available to the FPGA (i.e., the effective current limit). This is true because the FPGA takes on a very low power-to-ground impedance during the power-on period. If more supply current is available than what is necessary to satisfy I_{CCPO} min, the FPGA is likely to consume the excess. In practice, the POS current at room temperature can be on the order of an Ampere or more. For a description of POS behavior as related to the amount of supply current available, see **"Effects of Current Limit"**, page 5.

Beware of over-current protection circuits (e.g., trip/crowbar, foldback and fuse), since it is possible for these to inadvertently shut down power to the FPGA in the presence of a large POS current. (For more information, see "**"Regulator Selection"**, page 6.)

The Ramp Time Requirements

For the guaranteed power-on of both Spartan-II and Spartan-IIE devices, the V_{CCINT} ramp time, T_{CCPO}, must be no slower than 50 ms during power-on. This limit corresponds to the slowest ramp time for which the power-on current is formally characterized and tested. T_{CCPO} is measured with a load (i.e., a test board with FPGA) connected to the power supply.

The graphs in Figure 1 plot V_{CCINT} over time (the solid lines) for Spartan-II devices. They also show the slowest permissible V_{CCINT} ramp as a dashed line with a 0.05V/ms slope, which forms a triangle with the vertical axis. As long as the V_{CCINT} ramp remains completely within the triangle (Figure 1a), the T_{CCPO} requirement is satisfied. V_{CCINT} must not go outside the 0.05V/ms side of the triangle, even if it returns before reaching the nominal V_{CCINT} level (Figure 1b).

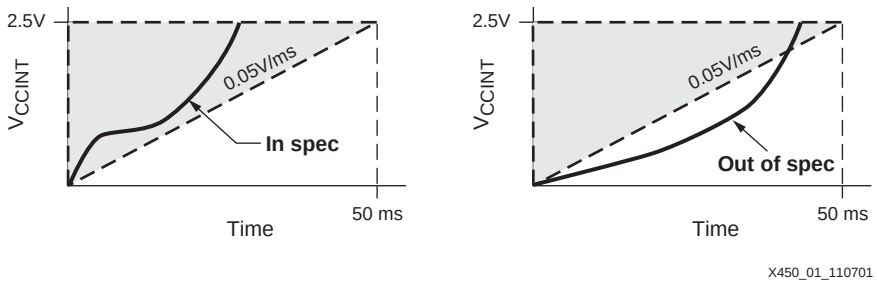

Figure 1: **Spartan-II Maximum V_{CCINT} Ramp Time Specification**

For Spartan-II devices, there is no limit to how fast V_{CCINT} can ramp up. No matter how fast the ramp time, the minimum I_{CCPO} specification does not change. Even though V_{CCINT} ramps up quickly (e.g., in less than 2 ms), as long as the I_{CCPO} specification is met, Spartan-II devices will power up successfully.

The Spartan-IIE devices have specifications similar to those just described for Spartan-II devices. Only in addition to the 50 ms maximum limit, there is also a minimum V_{CCINT} ramp time requirement of 2 ms. The graphs in Figure 2 plot the V_{CCINT} ramp (the solid line) for Spartan-IIE devices. The dashed line with 0.036V/ms slope represents the slowest permissible V_{CCINT} ramp. The dashed line with 0.90V/ms represents the fastest allowed V_{CCINT} ramp. These two lines form a triangle within which the V_{CCINT} ramp must stay (Figure 2a). If V_{CCINT} ventures outside of the triangle, the T_{CCPO} requirement is not satisfied (Figure 2, b and c).

For both families, ramp times in excess of 50 ms result in longer-lasting power-on current draw, since V_{CCINT} spends more time within the 0.6V to 0.8V range of the transistor turn-on threshold. Thermal stress is possible if the power supply provides a large current (e.g., on the order of Amperes) to the FPGA for a V_{CCINT} ramp time much longer than 50 ms (a case not

complying with the specification). As V_{CCINT} ramp times fall below 2 ms, the POS current increases slightly.

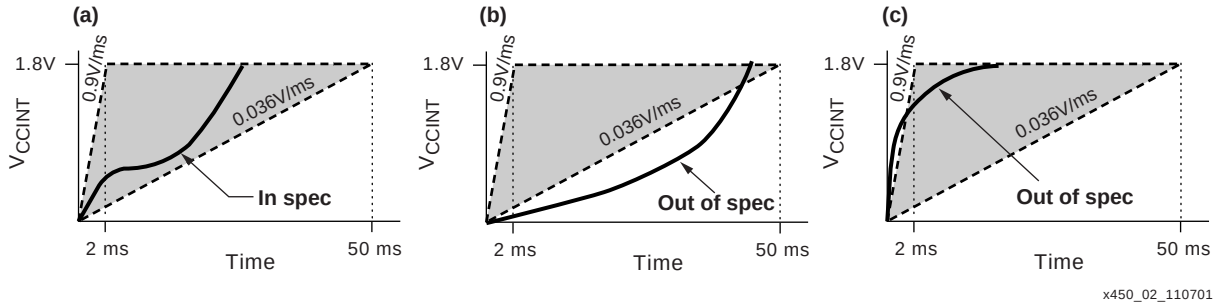

Figure 2: **Spartan-IIE Ramp Time Specifications**

Additional Requirements

The power supply, when connected to its load (e.g., board with FPGA) should exhibit a steadily increasing V_{CCINT} ramp (a positive slope, 0 or greater, over time). It is acceptable for the V_{CCINT} profile to level off to form a "shelf" before continuing on to the recommended operating V_{CCINT} voltage. This is the normal result of a current limit. (See **"Effects of Current Limit"** on page 5 for more information.) No dips in the negative direction are permitted.

The unloaded power supply should exhibit a steadily increasing voltage during turn-on. In this case, a shelf in the power-on voltage profile is unacceptable.

Recommended Spartan-IIE Power Sequence

For Spartan-IIE devices, power should be applied to the V_{CCINT} and the V_{CCO} lines simultaneously. If power is applied to V_{CCO} before V_{CCINT}, the FPGA may not put all of its I/Os in a high-impedance state. Furthermore, internal pull-up and pull-down resistors may be activated on various I/Os. Under these circumstances, I_{CCO} (the current drawn by all V_{CCO} lines) may rise to a relatively high level.

The power sequence has no effect on the I_{CCPO} specification of the Spartan-IIE family. For example, even though applying power to V_{CCO} before V_{CCINT} can cause the V_{CCO} lines to draw a momentary current surge during power-on, supplying a current of I_{CCPO} min. to the I_{CCINT} lines is sufficient to ensure successful power-on.

Testing the POS Specification

The power-on characteristics of all Spartan-II and Spartan-IIE FPGAs are tested twice: once during wafer sort and once again during final test. This test plan ensures that every FPGA shipped will power on successfully as long as the applicable data sheet specifications (e.g., I_{CCPO}, T_{CCPO}, etc.) are met.

Effects of Current Limit

The amount of supply current available to the FPGA determines the maximum size of the POS current surge. For a high current limit, the POS current will be relatively short in duration. In contrast, for a low current limit (e.g., 500 mA), the POS current will last longer. It is helpful to think of the FPGA as requiring a certain quota of energy in order to power-up successfully.

Figure 3 shows the effects of a current limit on the power path to the FPGA. The top graph shows the V_{CCINT} power-on profile over time. The lower graph shows the resulting POS current over time.

The solid curves show the case where a large amount of supply current is available to the FPGA so that there is effectively no limit. Here, a large, brief POS current is accompanied by a steadily rising V_{CCINT} ramp.

The dashed curves show what occurs when a current limit is present. In this case, the POS current can be no larger than the limit set, but lasts longer. At the same time, the V_{CCINT} profile exhibits a “shelf” lying roughly between 0.6V and 0.8V.

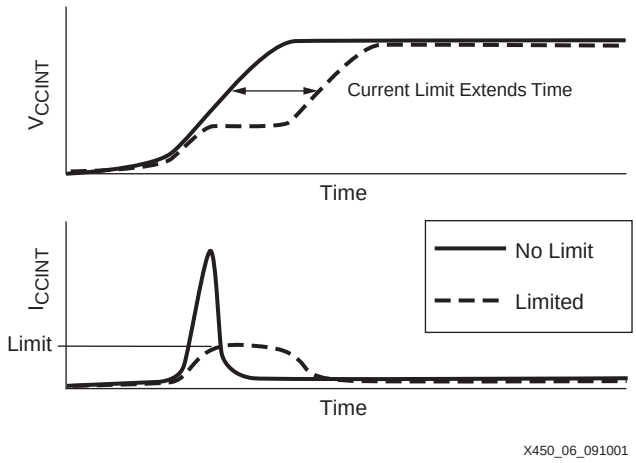

Figure 3: **The Effects of a Current Limit on the POS Current**

Board Power Considerations

When selecting a power supply for a board with FPGAs , it is important to consider not only the maximum current during user operation but also the total POS current requirement for the board. The latter is usually determined by adding together I_{CCPO} min. for all of the FPGAs. Keep in mind, different FPGAs may have different I_{CCPO} requirements.

For a relatively small FPGA, especially at junction temperatures below 0°C, I_{CCPO} min. can be greater than the operating current when in user mode. It follows that the total POS requirement for the board can exceed its maximum operating current when in the user mode. For this reason, the designer needs to select a power supply rated to provide a continuous current equal to or greater than the board's maximum operating current. Furthermore, the supply must be able to provide enough current on an instantaneous basis to satisfy the board's total POS requirement. In general, it is not difficult to meet the last condition since many power supplies can provide more current instantaneously than their continuous output rating would indicate.

At junction temperatures below 0°C, the total POS current for multiple Spartan-II FPGAs at 2A per FPGA can add up to several Amperes. Effective ways of managing such large POS requirements include staggering the application of power to FPGAs as well as adding a large capacitor to the power rail. These approaches are described in the "Powering on Multiple FPGAs" section of application note **XAPP451, "Power Assist Circuits for the Spartan-II and Spartan-IIE Families"**.

During the power-on period, Spartan-II and Spartan-IIE FPGAs do not ordinarily compete for power with other types of components on the board. Aside from FPGAs, integrated circuits in general do not draw significant current during power-on. Nor is there any risk of one FPGA depriving a second FPGA of power. This is explained in Figure 4, which shows four of the same FPGAs powering up together. Assume the supply can source just enough current to meet the total minimum POS current requirement (four times the applicable I_{CCPO} limit). Each FPGA can be modeled as a very low impedance element during power-on. According to this simplified perspective, the power-supply sees four low impedance elements in parallel. If one FPGA takes on a lower impedance value than the others, it will draw more POS current for a shorter time. The other FPGAs accept less current for a longer time. After this fashion, all four FPGAs receive the energy they require to power-on successfully.

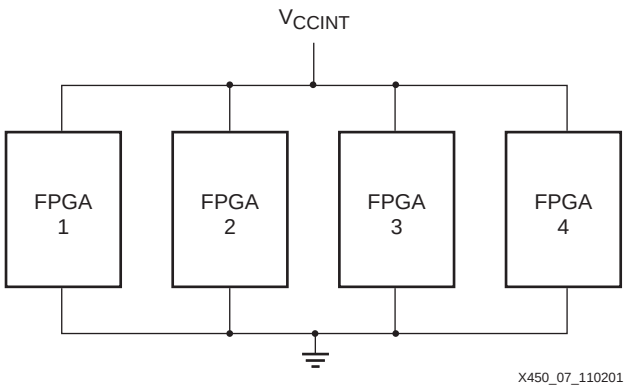

Figure 4: **Multiple FPGAs During Power-On**

Regulator Selection

Frequently, the power voltage applied to a board is higher than the nominal V_{CCINT} level that the FPGA accepts (2.5V for Spartan-II devices, 1.8V for Spartan-IIE devices). In this situation, regulators are commonly used to perform the required DC-to-DC conversion of the power voltage. Low-Drop-Out (LDO) Regulators are an excellent choice for level conversions from either 5V or 3.3V down to the desired V_{CCINT} voltage, since they are designed to operate with only a small voltage drop from input to output.

Satisfying the minimum POS current specification is simply a matter of verifying that the regulator can provide at least I_{CCPO} min. throughout the FPGA power-on period, which will always be less than the V_{CCINT} ramp time.

Many regulators have a current boost feature at turn-on. In this case, the regulator may be able to supply significantly more current to the FPGA during power-on than its guaranteed output rating would indicate. As a result, the V_{CCINT} ramp time may be short (e.g., 2 ms or less) with the POS duration even shorter. See **"The Minimum POS Current Requirement"** on page 2 for more information.

Some regulators specify a short circuit current limit (I_{LIMIT}) which measures the current that results when the output is momentarily connected to ground. During the power-on period, an FPGA connected as a load to the regulator output approximates such a short circuit condition. For this reason, it is appropriate to compare the I_{LIMIT} min. specification to the FPGA's I_{CCPO} min. specification. As an example, Table 1 shows specifications from the MAX1818 2.5V LDO regulator data sheet. This regulator meets the I_{CCPO} min. requirement of 500 mA for Spartan-II devices operated above 0°C as well as commercial Spartan-IIE devices since I_{LIMIT} min. (at 0.55A) is greater.

Table 1: **Selected MAX1818 LDO Regulator Specifications**

Description	Symbol	Parameters		Min	Typ	Max	Units
Guaranteed output current (RMS)	I_{OUT}	$V_{IN} \geq 2.7V$		500	-	-	mA
Short-circuit current limit	I_{LIMIT}	$V_{OUT} = 0V$, $V_{IN} \geq 2.7V$		**0.55**	0.8	**1.8**	A
In-regulation current limit		$V_{OUT} > 96\%$ of nominal value, $V_{IN} \geq 2.7V$		-	1.6	-	A
Dropout voltage	$V_{IN} - V_{OUT}$	$I_{OUT} = 500$ mA	$V_{OUT} = 5V$	-	100	220	mV
			$V_{OUT} = 3.3V$	-	120	215	
			$V_{OUT} = 2.5V$	-	210	**360**	
$\overline{SHDN}$ input threshold	V_{IH}	$2.5V < V_{IN} < 5.5V$		**1.6**	-	-	V
	V_{IL}	$2.5V < V_{IN} < 5.5V$		-	-	0.6	V

If the data sheet for a given regulator does not provide a minimum value for the short circuit current, the guaranteed output current (I_{OUT}) can be used instead, though this continuous current may make the comparison more conservative than necessary.

Many regulators feature some kind of over-current and/or thermal protection circuit. As a general recommendation, avoid regulators that employ internal over-current protection circuits, such as trip/crowbar and foldback, since these, if activated by a POS current, can prevent the FPGA from powering up. Regulator data sheets do not always clearly describe the kind of over-current protection circuit employed. The MAX1818 has no such protection. Figure 5 shows an example of a different regulator's foldback characteristic. As its output voltage is loaded down, this regulator cuts back on the amount of current it supplies.

The presence of a short circuit current specification in the data sheet serves as an indication that a given regulator has no foldback feature. For a short circuit condition to exist, a regulator must be able to stay in a current-limited state without shutting down.

The POS current is so brief that there is no risk of inadvertently triggering thermal protection circuits.

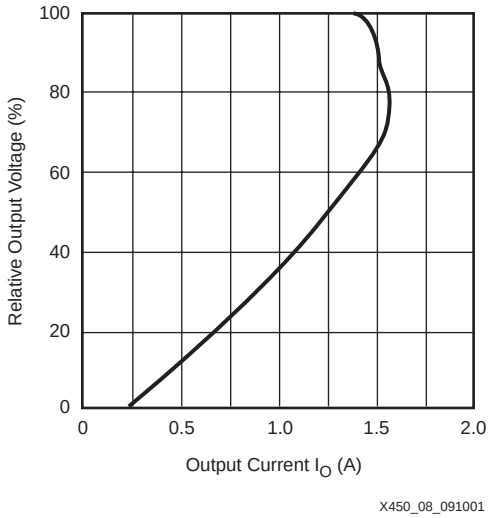

Figure 5: **Regulator Foldback Characteristics**

Using FPGAs in the Presence of Over-Current Protection

Despite the general caveat expressed in the preceding section, with special attention to the power path, over-current protection circuits and FPGAs can coexist on the same board. This is accomplished simply by ensuring that there is a suitable current limit on the power path to the FPGA. The limit may be a natural result of components already existing on the board (e.g., the maximum short circuit current of a regulator) or it can be created (e.g., using a P-channel MOSFET in saturation). Figure 6 shows a block diagram of a board whose supply, equipped with a foldback feature, powers a Spartan-II FPGA, among other components. The limit must be set such that the FPGA can draw a current of at least I_{CCPO} min, but never so much as to activate the foldback feature. This is shown graphically in Figure 7, where the limit is situated between I_{CCPO} min. and the trip point. The margin by which the trip point exceeds the limit represents the amount of current the rest of the board can draw during the power-on period without causing foldback. This margin need not be large, since, aside from FPGAs, most ICs do not draw significant current during power-on.

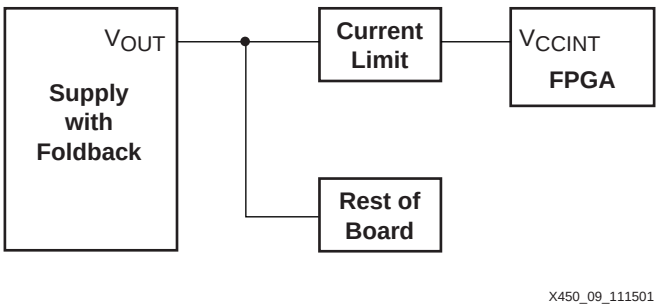

Figure 6: **Limit on Power Path Avoids Foldback**

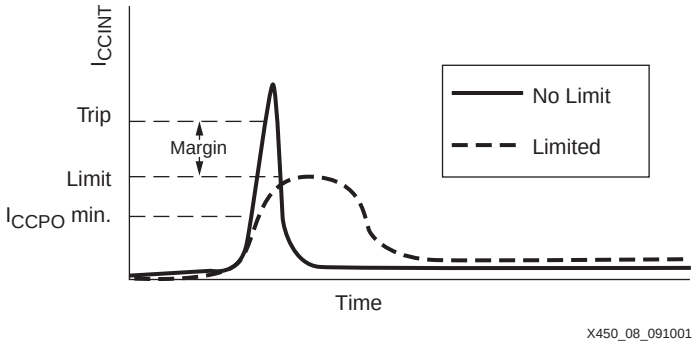

Figure 7: **Selecting a Current Limit to Avoid Foldback**

The approach of setting a limit, as described above, can also be used to prevent a fuse from blowing in the presence of a large POS current; nevertheless, using a slow-blow fuse is the preferred solution, since it is simpler to implement. This kind of fuse can blow only after a fixed time delay. Select the fuse so that the specified time delay is greater than the maximum POS period. In the presence of a current limit, the longest-lasting power-on current for Spartan-II devices will occur at the coldest operating temperature.

References

Power-Assist Circuits for the Spartan-II and Spartan-IIE Families (**XAPP451**)

Powering Xilinx Spartan-II FPGAs (**XAPP189**)

Spartan-II 2.5V FPGA Family: DC and Switching Characteristics (**Module 3 of the Spartan-II Data Sheet**)

Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics (**Module 3 of the Spartan-IIE Data Sheet**)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/15/01	1.0	Initial Xilinx release.