Virtex™-II Electrical Characteristics

Virtex-II devices are provided in –4, –5, and –6 speed grades, with –6 having the highest performance.

Virtex-II DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a –4 speed grade industrial device are the same as for a –4 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal Supply voltage relative to GND	–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.0	V
V_{REF}	Input Reference Voltage	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (user and dedicated I/Os)	–0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temp.	+220	°C
T_J	Operating junction temperature	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
	Internal Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	3.0	3.6	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.6	V
V_{BATT}	Battery voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.0	3.6	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:
1. If V_{CCAUX} and V_{CCO} are both at 3.3 V, they must use a common supply voltage.
2. If battery is not used, do not connect V_{BATT}.
3. For LVDS operation, V_{CCAUX} min is 3.13 V and max is 3.47 V.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage	All	1.2		V
V_{DRI}	Data Retention V_{CCAUX} Voltage	All	2.5		V
I_{REF}	V_{REF} current per bank	All	–10	+10	µA
I_L	Input leakage current	All	–10	+10	µA
C_{IN}	Input capacitance	All		10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note 1	250	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6 V (sample tested)	All	Note 1	250	µA
I_{BATT}	Battery supply current	All		100	nA

Notes:
1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typical	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2v40 XC2v80 XC2v250 XC2v500 XC2v1000 XC2v1500 XC2v2000 XC2v3000 XC2v4000 XC2v6000 XC2v8000		75 75 75 100 100 150 200 200 250 250 TBD	TBD TBD TBD TBD 250 TBD TBD TBD TBD 1000 TBD	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1,2)	XC2v40 XC2v80 XC2v250 XC2v500 XC2v1000 XC2v1500 XC2v2000 XC2v3000 XC2v4000 XC2v6000 XC2v8000		1 1 1 1 1 2 2 2 2 2 TBD	TBD TBD TBD TBD 2 TBD TBD TBD TBD 4 TBD	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current(1,2)	XC2v40 XC2v80 XC2v250 XC2v500 XC2v1000 XC2v1500 XC2v2000 XC2v3000 XC2v4000 XC2v6000 XC2v8000		10 10 10 10 10 20 20 20 25 25 TBD	TBD TBD TBD TBD 25 TBD TBD TBD TBD 100 TBD	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER™.
3. Data are retained even if V_{CCO} drops to 0 V.
4. Values specified for quiescent supply current parameters are Commercial Grade only.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT}, V_{CCAUX}, and V_{CCO} power supplies shall ramp on no faster than 1 ms and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages.

V_{CCAUX} and V_{CCO} for bank 4 must be connected together (3.3 V_{DC}) to meet the following specification.

Table 5 shows the minimum current required by Virtex-II devices for proper power on and configuration.

Power supplies can be turned on in any sequence, as long as V_{CCAUX} and V_{CCO} are connected together for bank 4.

If any V_{CCO} bank powers up before V_{CCAUX}, then each bank draws up to 600 mA, worst case, until the V_{CCAUX} powers on(1). This does not harm the device. If the current is limited to the minimum value above, or larger, the device powers on properly after all three supplies have passed through their power on reset threshold voltages.

Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Notes:
1. The 600 mA is transient current (peak); it eventually dissipates even if V_{CCAUX} does not power up.

Table 5: **Power On Current for Virtex-II Devices**

	Device (mA)										
	2v40	**2v80**	**2v250**	**2v500**	**2v1000**	**2v1500**	**2v2000**	**2v3000**	**2v4000**	**2v6000**	**2v8000**
$I_{CCINTMIN}$	250	250	250	250	500	500	500	500	750	1000	TBD
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100	100	100	TBD
I_{CCOMIN}	50	50	50	50	50	100	100	100	100	100	TBD

Notes:
1. Values specified for power on current parameters are Commercial Grade only.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	**V_{IL}**		**V_{IH}**		**V_{OL}**	**V_{OH}**	**I_{OL}**	**I_{OH}**
Standard	**V, min**	**V, max**	**V, min**	**V, max**	**V, Max**	**V, Min**	**mA**	**mA**
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16

Table 6: **DC Input and Output Levels *(Continued)***

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.6	V_{REF} + 0.6	8	– 8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.8	V_{REF} + 0.8	16	– 16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.65	V_{REF} + 0.65	7.6	– 7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.80	V_{REF} + 0.80	15.2	– 15.2
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.

LDT Differential Signal DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.475	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.70	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL.

Table 10: **LVPECL DC Specifications**

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as **Virtex-II Switching Characteristics**, page 8 (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: **Pin-to-Pin Performance**

Description	Pin-to-Pin (w/ I/O delays)	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder	6.3	XC2V1000 –5
32-bit Address Decoder	7.7	XC2V1000 –5
64-bit Address Decoder	9.3	XC2V1000 –5
4:1 MUX	5.7	XC2V1000 –5
8:1 MUX	6.5	XC2V1000 –5
16:1 MUX	6.7	XC2V1000 –5
32:1 MUX	8.7	XC2V1000 –5
Combinatorial (pad to LUT to pad)	5.0	XC2V1000 –5
Memory		
Block RAM		
Pad to setup	1.6	
Clock to Pad	9.5	
Distributed RAM		
Pad to setup	2.7	XC2V1000 –5
Clock to Pad	5.1 (no clk skew)	XC2V1000 –5

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: **Register-to-Register Performance**

Description	Register-to-Register Performance	Device Used & Speed Grade
Basic Functions		
16-bit Address Decoder	398	XC2V1000 –5
32-bit Address Decoder	291	XC2V1000 –5
64-bit Address Decoder	274	XC2V1000 –5
4:1 MUX	563	XC2V1000 –5
8:1 MUX	454	XC2V1000 –5
16:1 MUX	414	XC2V1000 –5
32:1 MUX	323	XC2V1000 –5
Register to LUT to Register	613	XC2V1000 –5
8-bit Adder	292	XC2V1000 –5
16-bit Adder	239	XC2V1000 –5
64-bit Adder	114	XC2V1000 –5
64-bit Counter	114	XC2V1000 –5
64-bit Accumulator	110	XC2V1000 –5

Table 12: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register Performance	Device Used & Speed Grade
Multiplier 18x18 (with Block RAM inputs)	88	XC2V1000 –5
Multiplier 18x18 (with Register inputs)	105	XC2V1000 –5
Memory		
Block RAM		
Single-Port 4096 x 4 bits	278	
Single-Port 2048 x 9 bits	277	
Single-Port 1024 x 18 bits	270	
Single-Port 512 x 36 bits	253	
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits	257	
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits	259	
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits	250	
Distributed RAM		
Single-Port 32 x 8-bit	387	XC2V1000 –5
Single-Port 64 x 8-bit	335	XC2V1000 –5
Single-Port 128 x 8-bit	266	XC2V1000 –5
Dual-Port 16 x 8	409	XC2V1000 –5
Dual-Port 32 x 8	311	XC2V1000 –5
Dual-Port 64 x 8	294	XC2V1000 –5
Shift Registers		
128-bit SRL	N/A	
256-bit SRL	N/A	
FIFOs (Async. in Block RAM)		
1024 x 18-bit Read	279	
1024 x 18-bit Write	172	
FIFOs (Sync. in SRL)		
128 x 8-bit	N/A	
128 x 16-bit	N/A	
CAMs in Block RAM		
32 x 9-bit	N/A	
64 x 9-bit	N/A	
128 x 9-bit	N/A	
256 x 9-bit	N/A	
CAMs in SRL		
32 x 16-bit	N/A	
64 x 32-bit	N/A	
128 x 40-bit	N/A	
256 x 48-bit	N/A	
1024 x 16-bit	N/A	
1024 x 72-bit	N/A	

Virtex-II Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that **Virtex-II Performance Characteristics**, page 6 are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Virtex-II device with a corresponding speed grade designation.

The values reported in this version of the switching characteristics are extracted from speeds file version 1.96.

Table 13: **Virtex-II Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2V40	–6, –5, –4		
XC2V80	–6, –5, –4		
XC2V250	–6, –5, –4		
XC2V500	–6, –5, –4		
XC2V1000	–6		–5, –4
XC2V1500	–6, –5, –4		
XC2V2000	–6, –5, –4		
XC2V3000	–6, –5, –4		
XC2V4000	–6, –5, –4		
XC2V6000	–6		–5, –4
XC2V8000	–5, –4		

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 10.

Table 14: **IOB Input Switching Characteristics**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All	0.69	0.76	0.88	ns, max
Pad to I output, with delay	T_{IOPID}	2v40	3.15	3.46	3.98	ns, max
		2v80	3.15	3.46	3.98	ns, max
		2v250	3.15	3.46	3.98	ns, max
		2v500	3.15	3.46	3.98	ns, max
		2v1000	3.15	3.46	3.98	ns, max
		2v1500	3.15	3.46	3.98	ns, max
		2v2000	3.15	3.46	3.98	ns, max
		2v3000	3.24	3.56	4.10	ns, max
		2v4000	3.24	3.56	4.10	ns, max
		2v6000	3.51	3.86	4.44	ns, max
		2v8000	TBD	TBD	TBD	ns, max

Table 14: **IOB Input Switching Characteristics *(Continued)***

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.99	1.08	1.24	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	2v40	3.44	3.78	4.35	ns, max
		2v80	3.44	3.78	4.35	ns, max
		2v250	3.44	3.78	4.35	ns, max
		2v500	3.44	3.78	4.35	ns, max
		2v1000	3.44	3.78	4.35	ns, max
		2v1500	3.44	3.78	4.35	ns, max
		2v2000	3.44	3.78	4.35	ns, max
		2v3000	3.53	3.88	4.46	ns, max
		2v4000	3.53	3.88	4.46	ns, max
		2v6000	3.80	4.18	4.81	ns, max
		2v8000	TBD	TBD	TBD	ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All	0.63	0.69	0.80	ns, max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.88/–0.36	0.96/–0.39	1.11/–0.45	ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	2v40	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v80	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v250	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v500	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v1000	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v1500	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v2000	3.33/–2.07	3.66/–2.28	4.21/–2.63	ns, min
		2v3000	3.42/–2.14	3.76/–2.35	4.33/–2.71	ns, min
		2v4000	3.42/–2.14	3.76/–2.35	4.33/–2.71	ns, min
		2v6000	3.69/–2.33	4.06/–2.56	4.67/–2.95	ns, min
		2v8000	TBD	TBD	TBD	ns, min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All	0.19/ 0.03	0.21/ 0.04	0.24/ 0.04	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, max
GSR to output IQ	T_{GSRQ}	All	7.27	7.99	9.19	ns, max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

IOB Input Switching Characteristics Standard Adjustments

Table 15: **IOB Input Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.00	0.00	0.00	ns
	$T_{ILVCMOS33}$	LVCMOS33	0.00	0.00	0.00	ns
	$T_{ILVCMOS25}$	LVCMOS25	0.10	0.11	0.12	ns
	$T_{ILVCMOS18}$	LVCMOS18	0.39	0.43	0.49	ns
	$T_{ILVCMOS15}$	LVCMOS15	0.91	1.00	1.15	ns
	T_{ILVDS_25}	LVDS_25	0.55	0.60	0.69	ns
	T_{ILVDS_33}	LVDS_33	0.55	0.60	0.69	ns
	$T_{ILVPECL\_33}$	LVPECL	0.55	0.60	0.69	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	0.00	0.00	0.00	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	0.00	0.00	0.00	ns
	T_{IPCIX}	PCI–X, 133 MHz, 3.3 V	0.00	0.00	0.00	ns
	T_{IGTL}	GTL	0.38	0.42	0.48	ns
	T_{IGTLP}	GTLP	0.38	0.42	0.48	ns
	T_{IHSTL_I}	HSTL I	0.38	0.42	0.48	ns
	T_{IHSTL_II}	HSTL II	0.38	0.42	0.48	ns
	T_{IHSTL_III}	HSTL III	0.38	0.42	0.48	ns
	T_{IHSTL_IV}	HSTL IV	0.38	0.42	0.48	ns
	$T_{IHSTL\_I\_18}$	HSTL I_18	0.38	0.42	0.48	ns
	$T_{IHSTL\_II\_18}$	HSTL II_18	0.38	0.42	0.48	ns
	$T_{IHSTL\_III\_18}$	HSTL III_18	0.38	0.42	0.48	ns
	$T_{IHSTL\_IV\_18}$	HSTL IV_18	0.38	0.42	0.48	ns
	T_{ISSTL2_I}	SSTL2 I	0.38	0.42	0.48	ns
	T_{ISSTL2_II}	SSTL2 II	0.38	0.42	0.48	ns
	T_{ISSTL3_I}	SSTL3 I	0.32	0.35	0.40	ns
	T_{ISSTL3_II}	SSTL3 II	0.32	0.35	0.40	ns
	T_{IAGP}	AGP	0.32	0.35	0.40	ns
	T_{ILVDCI_33}	LVDCI_33	0.00	0.00	0.00	ns
	T_{ILVDCI_25}	LVDCI_25	0.10	0.11	0.12	ns
	T_{ILVDCI_18}	LVDCI_18	0.39	0.43	0.49	ns

Table 15: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{ILVDCI_15}	LVDCI_15	0.91	1.00	1.14	ns
	$T_{ILVDCI\_DV2\_33}$	LVDCI_DV2_33	0.00	0.00	0.00	ns
	$T_{ILVDCI\_DV2\_25}$	LVDCI_DV2_25	0.10	0.11	0.12	ns
	$T_{ILVDCI\_DV2\_18}$	LVDCI_DV2_18	0.39	0.43	0.49	ns
	$T_{ILVDCI\_DV2\_15}$	LVDCI_DV2_15	0.91	1.00	1.14	ns
	T_{IGTL_DCI}	GTL_DCI	0.38	0.42	0.48	ns
	T_{IGTLP_DCI}	GTLP_DCI	0.38	0.42	0.48	ns
	$T_{IHSTL\_I\_DCI}$	HSTL_I_DCI	0.38	0.42	0.48	ns
	$T_{IHSTL\_II\_DCI}$	HSTL_II_DCI	0.38	0.42	0.48	ns
	$T_{IHSTL\_III\_DCI}$	HSTL_III_DCI	0.38	0.42	0.48	ns
	$T_{IHSTL\_IV\_DCI}$	HSTL_IV_DCI	0.38	0.42	0.48	ns
	$T_{IHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18	0.38	0.42	0.48	ns
	$T_{IHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18	0.38	0.42	0.48	ns
	$T_{IHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18	0.38	0.42	0.48	ns
	$T_{IHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18	0.38	0.42	0.48	ns
	$T_{ISSTL2\_I\_DCI}$	SSTL2_I_DCI	0.38	0.42	0.48	ns
	$T_{ISSTL2\_II\_DCI}$	SSTL2_II_DCI	0.38	0.42	0.48	ns
	$T_{ISSTL3\_I\_DCI}$	SSTL3_I_DCI	0.32	0.35	0.40	ns
	$T_{ISSTL3\_II\_DCI}$	SSTL3_II_DCI	0.32	0.35	0.40	ns
	T_{ILDT_25}	LDT_25	0.45	0.49	0.56	ns
	T_{IULVDS_25}	ULVDS_25	0.45	0.49	0.56	ns

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 13.

Table 16: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–6**	**–5**	**–4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	2.39	2.63	3.03	ns, max
O input to Pad via transparent latch	T_{IOOLP}	2.69	2.95	3.40	ns, max
3-State Delays					
T input to Pad high-impedance(1)	T_{IOTHZ}	0.51	0.56	0.64	ns, max
T input to valid data on Pad	T_{IOTON}	2.34	2.57	2.96	ns, max
T input to Pad high-impedance via transparent latch(1)	$T_{IOTLPHZ}$	0.80	0.88	1.01	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	2.63	2.89	3.33	ns, max
GTS to Pad high impedance(1)	T_{GTS}	6.56	7.22	8.30	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	2.72	2.99	3.44	ns, max
Clock CLK to Pad high-impedance (synchronous)(1)	T_{IOCKHZ}	0.95	1.04	1.20	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	2.78	3.06	3.51	ns, max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.31/–0.08	0.34/–0.09	0.39/–0.11	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.28/–0.06	0.31/–0.07	0.35/–0.08	ns, min
3–State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, min
3–State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}	3.37	3.71	4.26	ns, max
SR input to Pad high-impedance (asynchronous)(1)	T_{IOSRHZ}	1.52	1.67	1.92	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	3.35	3.68	4.23	ns, max
GSR to Pad	T_{IOGSRQ}	5.44	5.98	6.88	ns, max

Notes:
1. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	8.53	9.38	10.79	ns
	T_{OLVTTL_S4}	4 mA	5.15	5.67	6.52	ns
	T_{OLVTTL_S6}	6 mA	3.75	4.12	4.74	ns
	T_{OLVTTL_S8}	8 mA	2.57	2.83	3.25	ns
	T_{OLVTTL_S12}	12 mA	2.00	2.19	2.52	ns
	T_{OLVTTL_S16}	16 mA	1.17	1.28	1.48	ns
	T_{OLVTTL_S24}	24 mA	0.85	0.94	1.08	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	5.37	5.90	6.79	ns
	T_{OLVTTL_F4}	4 mA	2.19	2.41	2.77	ns
	T_{OLVTTL_F6}	6 mA	0.94	1.03	1.18	ns
	T_{OLVTTL_F8}	8 mA	0.06	0.07	0.08	ns
	T_{OLVTTL_F12}	12 mA	0.00	0.00	0.00	ns
	T_{OLVTTL_F16}	16 mA	–0.30	–0.33	–0.38	ns
	T_{OLVTTL_F24}	24 mA	–0.44	–0.48	–0.55	ns
	T_{OLVDS_25}	LVDS	–1.02	–1.12	–1.29	ns
	T_{OLVDS_33}	LVDS	–1.07	–1.18	–1.36	ns
	$T_{OLVDSEXT\_25}$	LVDS	–0.94	–1.03	–1.19	ns
	$T_{OLVDSEXT\_33}$	LVDS	–0.95	–1.05	–1.21	ns
	T_{OLDT_25}	LDT	–1.01	–1.11	–1.28	ns
	T_{OBLVDS_25}	BLVDS	0.63	0.69	0.79	ns
	T_{OULVDS_25}	ULVDS	–1.01	–1.11	–1.28	ns
	$T_{OLVPECL\_33}$	LVPECL	0.74	0.81	0.93	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	1.06	1.17	1.34	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	–0.14	–0.15	–0.18	ns
	T_{OPCIX}	PCI–X, 133 MHz, 3.3 V	–0.14	–0.16	–0.18	ns
	T_{OGTL}	GTL	1.13	1.24	1.43	ns
	T_{OGTLP}	GTLP	0.43	0.47	0.54	ns
	T_{OHSTL_I}	HSTL I	0.19	0.21	0.24	ns
	T_{OHSTL_II}	HSTL II	0.01	0.01	0.01	ns
	T_{OHSTL_III}	HSTL III	–0.17	–0.18	–0.21	ns
	T_{OHSTL_IV}	HSTL IV	–0.22	–0.24	–0.28	ns
	$T_{OHSTL\_I\_18}$	HSTL I_18	0.22	0.25	0.28	ns
	$T_{OHSTL\_II\_18}$	HSTL II_18	0.13	0.14	0.16	ns
	$T_{OHSTL\_III\_18}$	HSTL III_18	0.11	0.12	0.14	ns
	$T_{OHSTL\_IV\_18}$	HSTL IV_18	0.15	0.17	0.19	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	T_{OSSTL2_I}	SSTL2 I	0.20	0.22	0.25	ns
	T_{OSSTL2_II}	SSTL2 II	–0.36	–0.39	–0.45	ns
	T_{OSSTL3_I}	SSTL3 I	0.29	0.32	0.36	ns
	T_{OSSTL3_II}	SSTL3 II	–0.14	–0.16	–0.18	ns
	T_{OAGP}	AGP	–0.44	–0.48	–0.56	ns
	$T_{OLVCMOS33\_S2}$	LVCMOS33, Slow, 2 mA	7.03	7.74	8.90	ns
	$T_{OLVCMOS33\_S4}$	4 mA	3.83	4.22	4.85	ns
	$T_{OLVCMOS33\_S6}$	6 mA	2.73	3.00	3.45	ns
	$T_{OLVCMOS33\_S8}$	8 mA	1.97	2.17	2.50	ns
	$T_{OLVCMOS33\_S12}$	12 mA	1.46	1.60	1.84	ns
	$T_{OLVCMOS33\_S16}$	16 mA	0.87	0.96	1.10	ns
	$T_{OLVCMOS33\_S24}$	24 mA	0.82	0.91	1.04	ns
	$T_{OLVCMOS33\_F2}$	LVCMOS33, Fast, 2 mA	5.46	6.01	6.91	ns
	$T_{OLVCMOS33\_F4}$	4 mA	2.12	2.33	2.68	ns
	$T_{OLVCMOS33\_F6}$	6 mA	0.62	0.68	0.79	ns
	$T_{OLVCMOS33\_F8}$	8 mA	–0.08	–0.09	–0.11	ns
	$T_{OLVCMOS33\_F12}$	12 mA	–0.22	–0.24	–0.28	ns
	$T_{OLVCMOS33\_F16}$	16 mA	–0.42	–0.46	–0.53	ns
	$T_{OLVCMOS33\_F24}$	24 mA	–0.51	–0.56	–0.65	ns
	$T_{OLVCMOS25\_S2}$	LVCMOS25, Slow, 2 mA	8.34	9.17	10.55	ns
	$T_{OLVCMOS25\_S4}$	4 mA	4.69	5.16	5.93	ns
	$T_{OLVCMOS25\_S6}$	6 mA	4.14	4.56	5.24	ns
	$T_{OLVCMOS25\_S8}$	8 mA	3.61	3.97	4.57	ns
	$T_{OLVCMOS25\_S12}$	12 mA	2.51	2.76	3.18	ns
	$T_{OLVCMOS25\_S16}$	16 mA	1.98	2.18	2.51	ns
	$T_{OLVCMOS25\_S24}$	24 mA	1.62	1.78	2.05	ns
	$T_{OLVCMOS25\_F2}$	LVCMOS25, Fast, 2 mA	3.90	4.29	4.94	ns
	$T_{OLVCMOS25\_F4}$	4 mA	0.92	1.01	1.17	ns
	$T_{OLVCMOS25\_F6}$	6 mA	0.41	0.45	0.51	ns
	$T_{OLVCMOS25\_F8}$	8 mA	0.23	0.25	0.29	ns
	$T_{OLVCMOS25\_F12}$	12 mA	–0.13	–0.14	–0.17	ns
	$T_{OLVCMOS25\_F16}$	16 mA	–0.22	–0.24	–0.28	ns
	$T_{OLVCMOS25\_F24}$	24 mA	–0.38	–0.42	–0.48	ns
	$T_{OLVCMOS18\_S2}$	LVCMOS18, Slow, 2 mA	15.71	17.28	19.87	ns
	$T_{OLVCMOS18\_S4}$	4 mA	10.38	11.42	13.13	ns
	$T_{OLVCMOS18\_S6}$	6 mA	7.46	8.21	9.44	ns
	$T_{OLVCMOS18\_S8}$	8 mA	6.92	7.61	8.75	ns
	$T_{OLVCMOS18\_S12}$	12 mA	5.31	5.84	6.71	ns
	$T_{OLVCMOS18\_S16}$	16 mA	5.05	5.56	6.39	ns
	$T_{OLVCMOS18\_F2}$	LVCMOS18, Fast, 2 mA	4.64	5.10	5.87	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–6**	**–5**	**–4**	**Units**
	$T_{OLVCMOS18\_F4}$	4 mA	1.48	1.63	1.87	ns
	$T_{OLVCMOS18\_F6}$	6 mA	0.66	0.73	0.83	ns
	$T_{OLVCMOS18\_F8}$	8 mA	0.59	0.65	0.75	ns
	$T_{OLVCMOS18\_F12}$	12 mA	0.12	0.14	0.16	ns
	$T_{OLVCMOS18\_F16}$	16 mA	0.13	0.14	0.16	ns
	$T_{OLVCMOS15\_S2}$	LVCMOS15, Slow, 2 mA	19.67	21.63	24.88	ns
	$T_{OLVCMOS15\_S4}$	4 mA	13.13	14.44	16.61	ns
	$T_{OLVCMOS15\_S6}$	6 mA	12.55	13.80	15.87	ns
	$T_{OLVCMOS15\_S8}$	8 mA	9.54	10.49	12.06	ns
	$T_{OLVCMOS15\_S12}$	12 mA	9.46	10.41	11.97	ns
	$T_{OLVCMOS15\_S16}$	16 mA	8.56	9.41	10.83	ns
	$T_{OLVCMOS15\_F2}$	LVCMOS15, Fast, 2 mA	4.32	4.75	5.46	ns
	$T_{OLVCMOS15\_F4}$	4 mA	1.59	1.75	2.02	ns
	$T_{OLVCMOS15\_F6}$	6 mA	1.21	1.33	1.53	ns
	$T_{OLVCMOS15\_F8}$	8 mA	0.79	0.87	1.00	ns
	$T_{OLVCMOS15\_F12}$	12 mA	0.63	0.69	0.79	ns
	$T_{OLVCMOS15\_F16}$	16 mA	0.59	0.65	0.75	ns
	T_{OLVDCI_33}	LVDCI_33	0.66	0.73	0.83	ns
	T_{OLVDCI_25}	LVDCI_25	0.57	0.62	0.71	ns
	T_{OLVDCI_18}	LVDCI_18	1.40	1.54	1.77	ns
	T_{OLVDCI_15}	LVDCI_15	2.96	3.26	3.75	ns
	$T_{OLVDCI\_DV2\_33}$	LVDCI_DV2_33	0.15	0.17	0.19	ns
	$T_{OLVDCI\_DV2\_25}$	LVDCI_DV2_25	0.31	0.34	0.39	ns
	$T_{OLVDCI\_DV2\_18}$	LVDCI_DV2_18	1.07	1.18	1.35	ns
	$T_{OLVDCI\_DV2\_15}$	LVDCI_DV2_15	2.05	2.25	2.59	ns
	T_{OGTL_DCI}	GTL_DCI	2.82	3.10	3.56	ns
	T_{OGTLP_DCI}	GTLP_DCI	2.03	2.23	2.56	ns
	$T_{OHSTL\_I\_DCI}$	HSTL_I_DCI	0.50	0.55	0.63	ns
	$T_{OHSTL\_II\_DCI}$	HSTL_II_DCI	0.39	0.43	0.50	ns
	$T_{OHSTL\_III\_DCI}$	HSTL_III_DCI	0.15	0.17	0.19	ns
	$T_{OHSTL\_IV\_DCI}$	HSTL_IV_DCI	–0.01	–0.01	–0.02	ns
	$T_{OHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18	0.21	0.23	0.26	ns
	$T_{OHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18	0.94	1.03	1.19	ns
	$T_{OHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18	0.18	0.20	0.23	ns
	$T_{OHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18	–0.14	–0.16	–0.18	ns
	$T_{OSSTL2\_I\_DCI}$	SSTL2_I_DCI	0.25	0.28	0.32	ns
	$T_{OSSTL2\_II\_DCI}$	SSTL2_II_DCI	0.05	0.06	0.07	ns
	$T_{OSSTL3\_I\_DCI}$	SSTL3_I_DCI	0.30	0.33	0.38	ns
	$T_{OSSTL3\_II\_DCI}$	SSTL3_II_DCI	0.16	0.18	0.20	ns

Table 18: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	–
LVCMOS33	0	3.3	1.65	–
LVCMOS25	0	2.5	1.25	–
LVCMOS18	0	1.8	0.9	–
LVCMOS15	0	1.5	0.75	–
PCI33_3	Per PCI Specification			–
PCI66_3	Per PCI Specification			–
PCIX33_3	Per PCI–X Specification			–
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL	1.6 –0.3	1.6 + 0.3	1.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

Table 19: **Standard Capacitive Loads**

Standard	CsI (pF)
LVTTL Fast Slew Rate, 2mA drive	35
LVTTL Fast Slew Rate, 4mA drive	35
LVTTL Fast Slew Rate, 6mA drive	35
LVTTL Fast Slew Rate, 8mA drive	35
LVTTL Fast Slew Rate, 12mA drive	35
LVTTL Fast Slew Rate, 16mA drive	35
LVTTL Fast Slew Rate, 24mA drive	35
LVTTL Slow Slew Rate, 2mA drive	35
LVTTL Slow Slew Rate, 4mA drive	35
LVTTL Slow Slew Rate, 6mA drive	35
LVTTL Slow Slew Rate, 8mA drive	35
LVTTL Slow Slew Rate, 12mA drive	35
LVTTL Slow Slew Rate, 16mA drive	35
LVTTL Slow Slew Rate, 24mA drive	35
LVCMOS33	35
LVCMOS25	35
LVCMOS18	35
LVCMOS15	35
PCI 33MHZ 3.3 V	10
PCI 66 MHz 3.3 V	10
PCI–X 133 MHz 3.3 V	10
GTL	0
GTLP	0
HSTL Class I	20
HSTL Class II	20
HSTL Class III	20
HSTL Class IV	20
SSTL2 Class I	30
SSTL2 Class II	30
SSTL3 Class I	30
SSTL3 Class II	30
AGP	10

Notes:
1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
3. Use of IBIS models results in a more accurate prediction of the propagation delay:
   a. Model the output in an IBIS simulation into the standard capacitive load.
   b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
   c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
   d. Record the results from the new simulation.
   e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 15). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.61	0.67	0.77	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, min

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}	6.49	8.50	10.36	ns, max
Input to Pin34	T_{MULT_P34}	6.36	8.33	10.15	ns, max
Input to Pin33	T_{MULT_P33}	6.23	8.16	9.95	ns, max
Input to Pin32	T_{MULT_P32}	6.10	7.99	9.74	ns, max
Input to Pin31	T_{MULT_P31}	5.97	7.82	9.53	ns, max
Input to Pin30	T_{MULT_P30}	5.84	7.65	9.33	ns, max
Input to Pin29	T_{MULT_P29}	5.71	7.48	9.12	ns, max
Input to Pin28	T_{MULT_P28}	5.58	7.31	8.91	ns, max
Input to Pin27	T_{MULT_P27}	5.45	7.14	8.70	ns, max
Input to Pin26	T_{MULT_P26}	5.32	6.97	8.50	ns, max
Input to Pin25	T_{MULT_P25}	5.19	6.80	8.29	ns, max
Input to Pin24	T_{MULT_P24}	5.06	6.63	8.08	ns, max
Input to Pin23	T_{MULT_P23}	4.93	6.46	7.88	ns, max
Input to Pin22	T_{MULT_P22}	4.80	6.29	7.67	ns, max
Input to Pin21	T_{MULT_P21}	4.67	6.12	7.46	ns, max
Input to Pin20	T_{MULT_P20}	4.54	5.95	7.26	ns, max
Input to Pin19	T_{MULT_P19}	4.41	5.78	7.05	ns, max
Input to Pin18	T_{MULT_P18}	4.28	5.61	6.84	ns, max
Input to Pin17	T_{MULT_P17}	4.15	5.44	6.63	ns, max
Input to Pin16	T_{MULT_P16}	4.02	5.27	6.43	ns, max
Input to Pin15	T_{MULT_P15}	3.89	5.10	6.22	ns, max
Input to Pin14	T_{MULT_P14}	3.76	4.93	6.01	ns, max
Input to Pin13	T_{MULT_P13}	3.63	4.76	5.81	ns, max
Input to Pin12	T_{MULT_P12}	3.50	4.59	5.60	ns, max
Input to Pin11	T_{MULT_P11}	3.37	4.42	5.39	ns, max
Input to Pin10	T_{MULT_P10}	3.24	4.25	5.19	ns, max
Input to Pin9	T_{MULT_P9}	3.11	4.08	4.98	ns, max
Input to Pin8	T_{MULT_P8}	2.98	3.91	4.77	ns, max
Input to Pin7	T_{MULT_P7}	2.85	3.74	4.56	ns, max
Input to Pin6	T_{MULT_P6}	2.72	3.57	4.36	ns, max
Input to Pin5	T_{MULT_P5}	2.59	3.40	4.15	ns, max
Input to Pin4	T_{MULT_P4}	2.46	3.23	3.94	ns, max
Input to Pin3	T_{MULT_P3}	2.33	3.06	3.74	ns, max
Input to Pin2	T_{MULT_P2}	2.20	2.89	3.53	ns, max
Input to Pin1	T_{MULT_P1}	2.07	2.72	3.32	ns, max
Input to Pin0	T_{MULT_P0}	1.94	2.55	3.12	ns, max

Table 25: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, max
Clock to Output Pin					
Clock to Pin35	T_{MULTCK_P35}	4.11	6.91	8.11	ns, max
Clock to Pin34	T_{MULTCK_P34}	3.98	6.75	7.92	ns, max
Clock to Pin33	T_{MULTCK_P33}	3.86	6.59	7.74	ns, max
Clock to Pin32	T_{MULTCK_P32}	3.73	6.43	7.55	ns, max
Clock to Pin31	T_{MULTCK_P31}	3.60	6.27	7.37	ns, max
Clock to Pin30	T_{MULTCK_P30}	3.47	6.11	7.18	ns, max
Clock to Pin29	T_{MULTCK_P29}	3.34	5.95	6.99	ns, max
Clock to Pin28	T_{MULTCK_P28}	3.22	5.79	6.81	ns, max
Clock to Pin27	T_{MULTCK_P27}	3.09	5.63	6.62	ns, max
Clock to Pin26	T_{MULTCK_P26}	2.96	5.47	6.44	ns, max
Clock to Pin25	T_{MULTCK_P25}	2.83	5.31	6.25	ns, max
Clock to Pin24	T_{MULTCK_P24}	2.70	5.15	6.06	ns, max
Clock to Pin23	T_{MULTCK_P23}	2.58	4.99	5.88	ns, max
Clock to Pin22	T_{MULTCK_P22}	2.45	4.83	5.69	ns, max
Clock to Pin21	T_{MULTCK_P21}	2.32	4.67	5.51	ns, max
Clock to Pin20	T_{MULTCK_P20}	2.19	4.51	5.32	ns, max
Clock to Pin19	T_{MULTCK_P19}	2.06	4.35	5.13	ns, max
Clock to Pin18	T_{MULTCK_P18}	1.94	4.19	4.95	ns, max
Clock to Pin17	T_{MULTCK_P17}	1.81	4.03	4.76	ns, max
Clock to Pin16	T_{MULTCK_P16}	1.68	3.87	4.58	ns, max
Clock to Pin15	T_{MULTCK_P15}	1.68	3.71	4.39	ns, max
Clock to Pin14	T_{MULTCK_P14}	1.68	3.55	4.20	ns, max
Clock to Pin13	T_{MULTCK_P13}	1.68	3.39	4.02	ns, max
Clock to Pin12	T_{MULTCK_P12}	1.68	3.23	3.83	ns, max
Clock to Pin11	T_{MULTCK_P11}	1.68	3.07	3.65	ns, max
Clock to Pin10	T_{MULTCK_P10}	1.68	2.91	3.46	ns, max
Clock to Pin9	T_{MULTCK_P9}	1.68	2.75	3.27	ns, max
Clock to Pin8	T_{MULTCK_P8}	1.68	2.59	3.09	ns, max
Clock to Pin7	T_{MULTCK_P7}	1.68	2.43	2.90	ns, max
Clock to Pin6	T_{MULTCK_P6}	1.68	2.27	2.72	ns, max
Clock to Pin5	T_{MULTCK_P5}	1.68	2.11	2.53	ns, max
Clock to Pin4	T_{MULTCK_P4}	1.68	1.95	2.34	ns, max
Clock to Pin3	T_{MULTCK_P3}	1.68	1.79	2.16	ns, max
Clock to Pin2	T_{MULTCK_P2}	1.68	1.70	1.97	ns, max
Clock to Pin1	T_{MULTCK_P1}	1.68	1.70	1.97	ns, max
Clock to Pin0	T_{MULTCK_P0}	1.68	1.70	1.97	ns, max

Block SelectRAM Switching Characteristics

Table 26: **Block SelectRAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	2.10	2.31	2.65	ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, min
EN input	T_{BECK}/T_{BCKE}	0.95/–0.46	1.04/–0.50	1.20/–0.58	ns, min
RST input	T_{BRCK}/T_{BCKR}	1.31/–0.71	1.44/–0.78	1.65/–0.90	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.57/–0.19	0.63/–0.21	0.72/–0.25	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}	1.17	1.29	1.48	ns, min
Minimum Pulse Width, Low	T_{BPWL}	1.17	1.29	1.48	ns, min

TBUF Switching Characteristics

Table 27: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–6	–5	–4	
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.45	0.50	0.58	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.44	0.48	0.55	ns, max
TRI input to valid data on OUT output	T_{ON}	0.44	0.48	0.55	ns, max

JTAG Test Access Port Switching Characteristics

Table 28: **JTAG Test Access Port Switching Characteristics**

Description	Symbol		Units
TMS and TDI Setup times before TCK	T_{TAPTK}	5.5	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	0.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	10.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Virtex-II Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM

Table 29: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 13.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	2v40	2.19	2.40	2.76	ns
		2v80	2.19	2.40	2.76	ns
		2v250	2.19	2.40	2.76	ns
		2v500	2.19	2.40	2.76	ns
		2v1000	2.19	2.40	2.76	ns
		2v1500	2.19	2.40	2.76	ns
		2v2000	2.19	2.40	2.76	ns
		2v3000	2.28	2.50	2.88	ns
		2v4000	2.28	2.50	2.88	ns
		2v6000	2.73	3.00	3.45	ns
		2v8000	TBD	TBD	TBD	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 18.
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 30: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 13.						
Global Clock and OFF without DCM	T_{ICKOF}	2v40	4.28	4.70	4.98	ns
		2v80	4.28	4.70	4.98	ns
		2v250	4.50	5.00	5.75	ns
		2v500	4.50	5.00	5.75	ns
		2v1000	5.10	5.40	5.90	ns
		2v1500	5.10	5.40	5.90	ns
		2v2000	5.20	5.55	6.10	ns
		2v3000	5.20	5.70	6.55	ns
		2v4000	5.50	6.00	6.90	ns
		2v6000	6.00	6.50	7.22	ns
		2v8000	TBD	TBD	TBD	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 18.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 31: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 10.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	2v40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		2v80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		2v250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		2v500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		2v1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		2v1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		2v2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		2v3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		2v4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		2v6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		2v8000	TBD	TBD	TBD	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is already included in the timing calculation.

Global Clock Setup and Hold for LVTTL Standard, *Without* DCM

Table 32: **Global Clock Setup and Hold for LVTTL Standard, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			–6	–5	–4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 10.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	2v40	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v80	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v250	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v1000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v1500	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v2000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v3000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v4000	1.92/ 0.00	1.92/ 0.00	2.21/ 0.00	ns
		2v6000	1.92/ 0.46	1.92/ 0.50	2.21/ 0.50	ns
		2v8000	TBD	TBD	TBD	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

DCM Timing Parameters

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605; all devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 33: **Operating Frequency Ranges**

Description	Symbol	Constraints	Speed Grade			Units
			–6	–5	–4	
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_1X_LF_Max		230.00	210.00	180.00	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_2X_LF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_LF_Min		1.50	1.50	1.50	MHz
	CLKOUT_FREQ_DV_LF_Max		150.00	140.00	120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_Min		24.00	24.00	24.00	MHz
	CLKOUT_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs)(1)	CLKIN_FREQ_DLL_LF_Min		24.00	24.00	24.00	MHz
	CLKIN_FREQ_DLL_LF_Max		230.00	210.00	180.00	MHz
CLKIN (using CLKFX outputs)(2)	CLKIN_FREQ_FX_LF_Min		1.00	1.00	1.00	MHz
	CLKIN_FREQ_FX_LF_Max		260.00	240.00	210.00	MHz
PSCLK	PSCLK_FREQ_LF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_LF_Max		450.00	420.00	360.00	MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180	CLKOUT_FREQ_1X_HF_Min		48.00	48.00	48.00	MHz
	CLKOUT_FREQ_1X_HF_Max		450.00	420.00	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_Min		3.00	3.00	3.00	MHz
	CLKOUT_FREQ_DV_HF_Max		300.00	280.00	240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_Min		210.00	210.00	210.00	MHz
	CLKOUT_FREQ_FX_HF_Max		350.00	320.00	270.00	MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs)(1)	CLKIN_FREQ_DLL_HF_Min		48.00	48.00	48.00	MHz
	CLKIN_FREQ_DLL_HF_Max		450.00	420.00	360.00	MHz
CLKIN (using CLKFX outputs)(2)	CLKIN_FRQ_FX_HF_Min		50.00	50.00	50.00	MHz
	CLKIN_FRQ_FX_HF_Max		350.00	320.00	270.00	MHz
PSCLK	PSCLK_FREQ_HF_Min		0.01	0.01	0.01	MHz
	PSCLK_FREQ_HF_Max		450.00	420.00	360.00	MHz

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.

Input Clock Tolerances

Table 34: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			–6		–5		–4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/high Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
CLKIN(2)	CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. Specification also applies to PSCLK.

Output Clock Jitter

Table 35: **Output Clock Jitter**

Description	Symbol	Constraints	Speed Grade			Units
			–6	–5	–4	
Clock Synthesis Period Jitter						
CLK0	CLKOUT_PER_JITT_0		±100	±100	±100	ps
CLK90	CLKOUT_PER_JITT_90		±150	±150	±150	ps
CLK180	CLKOUT_PER_JITT_180		±150	±150	±150	ps
CLK270	CLKOUT_PER_JITT_270		±150	±150	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X		±200	±200	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1		±150	±150	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2		±300	±300	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX		Note 1	Note 1	Note 1	ps

Notes:
1. Values for this parameter are available on www.xilinx.com.

Output Clock Phase Alignment

Table 36: **Output Clock Phase Alignment**

Description	Symbol	Constraints	Speed Grade			Units
			–6	–5	–4	
Phase Offset Between CLKIN and CLKFB						
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		±50	±50	±50	ps
Phase Offset Between Any DCM Outputs						
All CLK* outputs	CLKOUT_PHASE		±140	±140	±140	ps
Duty Cycle Precision						
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL		±150	±150	±150	ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		±100	±100	±100	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Miscellaneous Timing Parameters

Table 37: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade			Units
			–6	–5	–4	
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL					
	LOCK_DLL_60	> 60MHz	20.0	20.0	20.0	µs
	LOCK_DLL_50_60	50 - 60 MHz	25.0	25.0	25.0	µs
	LOCK_DLL_40_50	40 - 50 MHz	50.0	50.0	50.0	µs
	LOCK_DLL_30_40	30 - 40 MHz	90.0	90.0	90.0	µs
	LOCK_DLL_24_30	24 - 30 MHz	120.0	120.0	120.0	µs
Using CLKFX outputs	LOCK_FX_MIN		10.0	10.0	10.0	ms
	LOCK_FX_MAX		10.0	10.0	10.0	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT		50.0	50.0	50.0	µs
Fine-Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.0	10.0	10.0	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.0	30.0	30.0	ps
	DCM_TAP_MAX		60.0	60.0	60.0	ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Frequency Synthesis

Table 38: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross Reference

Table 39: **Parameter Cross Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Table 18, “Delay Measurement Methodology,” on page 16
04/23/01	1.5	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.
07/30/01	1.6	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Added values to the **Virtex-II Pin-to-Pin Output Parameter Guidelines** and **Virtex-II Pin-to-Pin Input Parameter Guidelines** tables. • Added **Frequency Synthesis** table.
10/02/01	1.7	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables. • Updated the speed grade designations used in data sheets, and added Table 13, which shows the current speed grade designation for each device.
10/05/01	1.8	• Corrected the speed grade designation for the XC2V1000 device in Table 13.
10/12/01	1.9	• Updated values in the **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables.
11/28/01	2.0	• Updated values in Table 3, Table 4, Table 5, **Virtex-II Performance Characteristics**, and **Virtex-II Switching Characteristics** tables.
01/03/02	2.1	• Updated values in **Virtex-II Performance Characteristics** and **Virtex-II Switching Characteristics** tables, based on values extracted from speeds file version 1.96. • Changed the speed grade designation for the XC2V6000 device in Table 13.

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- DS031-1, Virtex-II 1.5V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS031-2, Virtex-II 1.5V FPGAs: **Functional Description (Module 2)**
- DS031-3, Virtex-II 1.5V FPGAs: DC and Switching Characteristics (Module 3)
- DS031-4, Virtex-II 1.5V FPGAs: **Pinout Tables (Module 4)**