

## Features

- 36 macrocells with 800 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (36 user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 3.3V-core XC9536XL device in the 44-pin PLCC, 44-pin VQFP, and 48-pin CSP packages

## Description

The XC9536XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of two 54V18 Function Blocks, providing 800 usable gates with propagation delays of 3.5 ns. See [Figure 2](#) for architecture overview.

## Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of  $I_{CC}$ , the following equation may be used:

$$I_{CC} \text{ (mA)} = MC_{HP}(0.36) + MC_{LP}(0.23) + MC(0.005 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance (default) mode

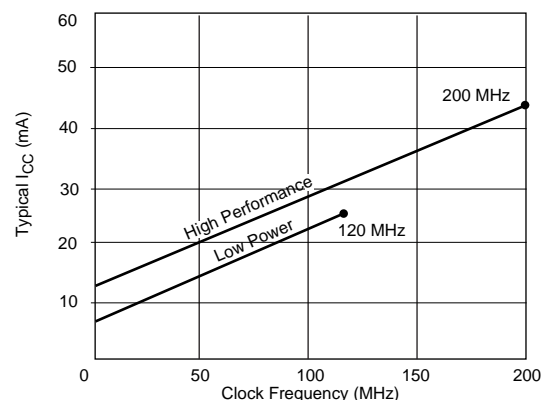
$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

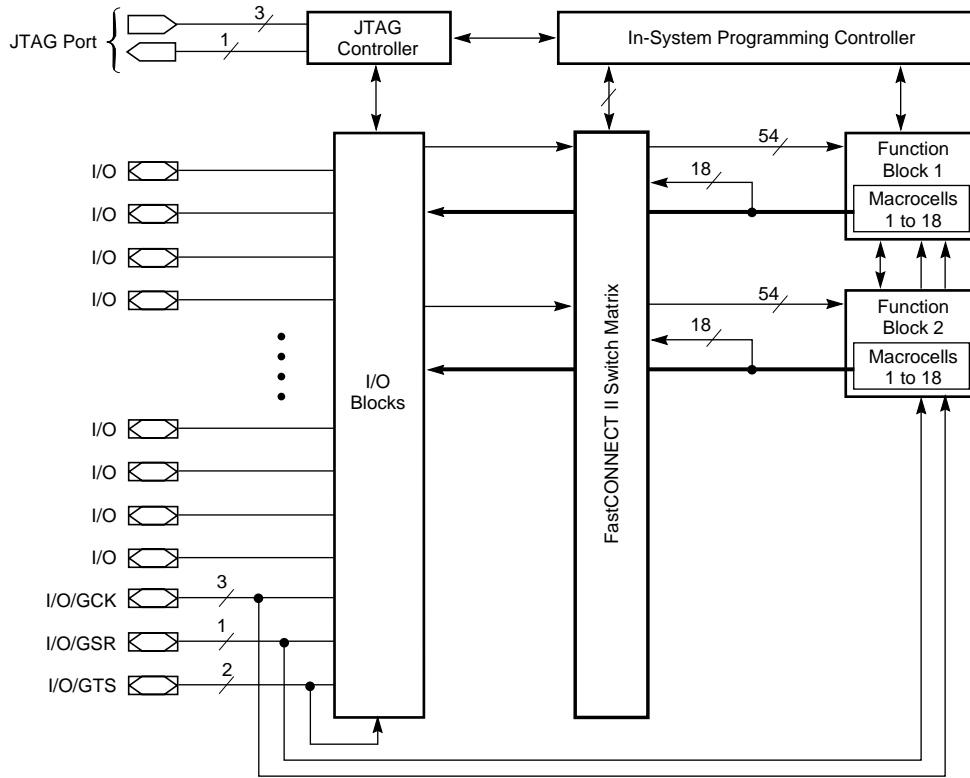
This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual  $I_{CC}$  value varies with the design application and should be verified during normal system operation.

[Figure 1](#) shows the above estimation in a graphical form.



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Figure 1: Typical  $I_{CC}$  vs. Frequency for XC9536XV



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**Figure 2: XC9536XV Architecture**

Function block outputs (indicated by the bold line) drive the I/O Blocks directly.

## Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 2.7	V
$V_{CCIO}$	Supply voltage for output drivers	-0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND <sup>(1)</sup>	-0.5 to 3.6	V
$V_{TS}$	Voltage applied to 3-state output <sup>(1)</sup>	-0.5 to 3.6	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	+150	°C

### Notes:

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	2.37	2.62	V
		Industrial $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	2.37	2.62	
$V_{CCIO}$	Supply voltage for output drivers for 3.3V operation		3.13	3.46	V
	Supply voltage for output drivers for 2.5V operation		2.37	2.62	V
	Supply voltage for output drivers for 1.8V operation		1.71	1.89	V
$V_{IL}$	Low-level input voltage		0	0.8	V
$V_{IH}$	High-level input voltage		1.7	3.6	V
$V_O$	Output voltage		0	$V_{CCIO}$	V

## Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
$T_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles (Endurance)	10,000	-	Cycles
$V_{ESD}$	Electrostatic Discharge (ESD)	2,000	-	Volts

## DC Characteristics (Over Recommended Operating Conditions)

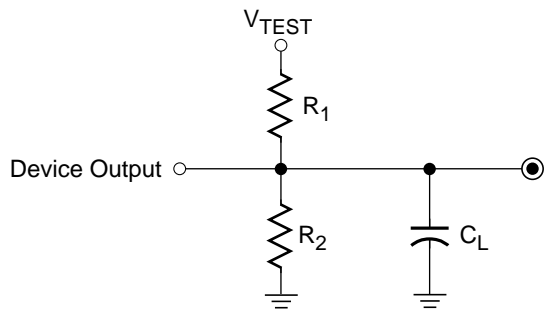
Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 3.3V outputs	$I_{OH} = -4.0 \text{ mA}$	2.4	-	V
	Output high voltage for 2.5V outputs	$I_{OH} = -1.0 \text{ mA}$	2.0	-	V
	Output high voltage for 1.8V outputs	$I_{OH} = -100 \mu\text{A}$	$90\% V_{CCIO}$	-	V
$V_{OL}$	Output low voltage for 3.3V outputs	$I_{OL} = 8.0 \text{ mA}$	-	0.4	V
	Output low voltage for 2.5V outputs	$I_{OL} = 1.0 \text{ mA}$	-	0.4	V
	Output low voltage for 1.8V outputs	$I_{OL} = 100 \mu\text{A}$	-	0.4	V
$I_{IL}$	Input leakage low current	$V_{CC} = 2.62\text{V}$ $V_{CCIO} = 3.6\text{V}$ $V_{IN} = \text{GND or } 3.6\text{V}$	-	10	$\mu\text{A}$
$I_{IH}$	Input leakage high current	$V_{CC} = 2.62\text{V}$ $V_{CCIO} = 3.6\text{V}$ $V_{IN} = \text{GND or } 3.6\text{V}$	-	10	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$	-	10	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	7		mA

## AC Characteristics

Symbol	Parameter	XC9536XV-3		XC9536XV-4		XC9536XV-5		XC9536XV-7		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$T_{PD}$	I/O to output valid	-	3.5	-	4.0	-	5.0	-	7.5	ns
$T_{SU}$	I/O setup time before GCK	2.5	-	2.8	-	3.5	-	4.8	-	ns
$T_H$	I/O hold time after GCK	0	-	0	-	0	-	0	-	ns
$T_{CO}$	GCK to output valid	-	2.5	-	2.8	-	3.5	-	4.5	ns
$f_{SYSTEM}$	Multiple FB internal operating frequency	-	277.8	-	250.0	-	222.2	-	125.0	MHz
$T_{PSU}$	I/O setup time before p-term clock input	0.7	-	0.8	-	1.0	-	1.6	-	ns
$T_{PH}$	I/O hold time after p-term clock input	1.8	-	2.0	-	2.5	-	3.2	-	ns
$T_{PCO}$	P-term clock output valid	-	4.3	-	4.8	-	6.0	-	7.7	ns
$T_{OE}$	GTS to output valid	-	2.8	-	3.2	-	4.0	-	5.0	ns
$T_{OD}$	GTS to output disable	-	2.8	-	3.2	-	4.0	-	5.0	ns
$T_{POE}$	Product term OE to output enabled	-	4.9	-	5.6	-	7.0	-	9.5	ns
$T_{POD}$	Product term OE to output disabled	-	4.9	-	5.6	-	7.0	-	9.5	ns
$T_{AO}$	GSR to output valid	-	7.0	-	7.9	-	10.0	-	12.0	ns
$T_{PAO}$	P-term S/R to output valid	-	7.5	-	8.5	-	10.7	-	12.6	ns
$T_{WLH}$	GCK pulse width (High or Low)	1.8	-	2.0	-	2.2	-	4.0	-	ns
$T_{PLH}$	P-term clock pulse width (High or Low)	4.5	-	5.0	-	5.0	-	6.5	-	ns
<b>Advance Information</b>						<b>Preliminary Information</b>				

### Notes:

1. Please contact Xilinx for up-to-date information on advance specifications.



Output Type	V <sub>CCIO</sub>	V <sub>TEST</sub>	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>
	3.3V	3.3V	320Ω	360Ω	35 pF
	2.5V	2.5V	250Ω	660Ω	35 pF
	1.8V	1.8V	10KΩ	14KΩ	35 pF

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Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC9536XV-3		XC9536XV-4		XC9536XV-5		XC9536XV-7		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>										
T <sub>IN</sub>	Input buffer delay	-	1.4	-	1.6	-	2.0	-	2.3	ns
T <sub>GCK</sub>	GCK buffer delay	-	0.8	-	1.0	-	1.2	-	1.5	ns
T <sub>GSR</sub>	GSR buffer delay	-	1.4	-	1.6	-	2.0	-	3.1	ns
T <sub>GTS</sub>	GTS buffer delay	-	2.8	-	3.2	-	4.0	-	5.0	ns
T <sub>OUT</sub>	Output buffer delay	-	1.5	-	1.6	-	2.1	-	2.5	ns
T <sub>EN</sub>	Output buffer enable/disable delay	-	0	-	0	-	0	-	0	ns
<b>Product Term Control Delays</b>										
T <sub>PTCK</sub>	Product term clock delay	-	1.2	-	1.4	-	1.7	-	2.4	ns
T <sub>PTSR</sub>	Product term set/reset delay	-	0.5	-	0.6	-	0.7	-	1.4	ns
T <sub>PTTS</sub>	Product term 3-state delay	-	3.5	-	4.0	-	5.0	-	7.2	ns
<b>Internal Register and Combinatorial Delays</b>										
T <sub>PDI</sub>	Combinatorial logic propagation delay	-	0.1	-	0.2	-	0.2	-	1.3	ns
T <sub>SUI</sub>	Register setup time	1.4	-	1.6	-	2.0	-	2.6	-	ns
T <sub>HI</sub>	Register hold time	1.1	-	1.2	-	1.5	-	2.2	-	ns
T <sub>ECSU</sub>	Register clock enable setup time	1.4	-	1.6	-	2.0	-	2.6	-	ns
T <sub>ECHO</sub>	Register clock enable hold time	1.1	-	1.2	-	1.5	-	2.2	-	ns
T <sub>COI</sub>	Register clock to output valid time	-	0.2	-	0.2	-	0.2	-	0.5	ns
T <sub>AOI</sub>	Register async. S/R to output delay	-	4.1	-	4.7	-	5.9	-	6.4	ns
T <sub>RAI</sub>	Register async. S/R recover before clock	3.5		4.0		5.0		7.5		ns
T <sub>LOGI</sub>	Internal logic delay	-	0.5	-	0.6	-	0.7	-	1.4	ns
T <sub>LOGILP</sub>	Internal low power logic delay	-	5.5	-	5.6	-	5.7	-	6.4	ns
<b>Feedback Delays</b>										
T <sub>F</sub>	FastCONNECT II™ feedback delay	-	1.5	-	1.6	-	1.6	-	3.5	ns
<b>Time Adders</b>										
T <sub>PTA</sub>	Incremental product term allocator delay	-	0.5	-	0.6	-	0.7	-	0.8	ns
T <sub>PTA2</sub>	Adjacent macrocell p-term allocator delay	-	0.2	-	0.2	-	0.3	-	0.3	ns
T <sub>SLEW</sub>	Slew-rate limited delay	-	3.0	-	3.0	-	3.0	-	4.0	ns
<b>Advance Information</b>						<b>Preliminary Information</b>				

**Notes:**

1. Please contact Xilinx for up-to-date information on advance specifications.

## XC9536XV I/O Pins

Function Block	Macrocell	PC44	VQ44	CS48	BScan Order	Function Block	Macrocell	PC44	VQ44	CS48	BScan Order
1	1	2	40	D6	105	2	1	1	39	D7	51
1	2	3	41	C7	102	2	2	44	38	E5	48
1	3	5 <sup>(1)</sup>	43 <sup>(1)</sup>	B7 <sup>(1)</sup>	99	2	3	42 <sup>(1)</sup>	36 <sup>(1)</sup>	E6 <sup>(1)</sup>	45
1	4	4	42	C6	96	2	4	43	37	E7	42
1	5	6 <sup>(1)</sup>	44 <sup>(1)</sup>	B6 <sup>(1)</sup>	93	2	5	40 <sup>(1)</sup>	34 <sup>(1)</sup>	F6 <sup>(1)</sup>	39
1	6	8	2	A6	90	2	6	39 <sup>(1)</sup>	33 <sup>(1)</sup>	G7 <sup>(1)</sup>	36
1	7	7 <sup>(1)</sup>	1 <sup>(1)</sup>	A7 <sup>(1)</sup>	87	2	7	38	32	G6	33
1	8	9	3	C5	84	2	8	37	31	F5	30
1	9	11	5	B5	81	2	9	36	30	G5	27
1	10	12	6	A4	78	2	10	35	29	F4	24
1	11	13	7	B4	75	2	11	34	28	G4	21
1	12	14	8	A3	72	2	12	33	27	E3	18
1	13	18	12	B2	69	2	13	29	23	F2	15
1	14	19	13	B1	66	2	14	28	22	G1	12
1	15	20	14	C2	63	2	15	27	21	F1	9
1	16	22	16	C3	60	2	16	26	20	E2	6
1	17	24	18	D2	57	2	17	25	19	E1	3
1	18	-	-	D3	54	2	18	-	-	E4	0

### Notes:

1. Global control pin.

## XC9536XV Global, JTAG and Power Pins

Pin Type	PC44	VQ44	CS48
I/O/GCK1	5	43	B7
I/O/GCK2	6	44	B6
I/O/GCK3	7	1	A7
I/O/GTS1	42	36	E6
I/O/GTS2	40	34	F6
I/O/GSR	39	33	G7
TCK	17	11	A1
TDI	15	9	B3
TDO	30	24	G2
TMS	16	10	A2
V <sub>CCINT</sub> 2.5V	21, 41	15, 35	C1, F7
V <sub>CCIO</sub> 1.8V/2.5V/3.3V	32	26	G3
GND	10, 23, 31	4, 17, 25	A5, D1, F3
No Connects	-	-	-



## Revision History

Date	Revision No.	Description
02/01/00	1.1	Initial Xilinx release. Advance information specification.
01/29/01	2.0	Added -3 performance specification and VQ44 package. Deleted VQ64 package. Updated $I_{CC}$ vs. Frequency <a href="#">Figure 1</a> .
05/15/01	2.1	Updated $I_{CC}$ formula, Recommended Operation Conditions, -3, -4, and -5 AC Characteristics and Internal Timing Parameters
08/27/01	2.2	Changed $V_{CCIO}$ 3.3V from 3.13 to 3.0 (min), 3.46 to 3.60 (max); DC characteristics: $I_{IL}$ - added "low" current, $I_{IH}$ - changed to "Input leakage high current"; Internal Timing: -3 $T_{CGK}$ from 0.3 to 0.8; -5 $T_{AOI}$ from 6.5 to 5.9.