Virtex-II Pro Electrical Characteristics

Virtex-II Pro devices are provided in -8, -7, and -6 speed grades, with -8 having the highest performance.

Virtex-II Pro DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -6 speed grade industrial device are the same as for a -6 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications. Contact Xilinx for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex-II Pro DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.45	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.45	V
V_{BATT}	Key memory battery backup supply	–0.5 to 3.45	V
V_{REF}	Input reference voltage	–0.5 to 3.45	V
V_{IN}	Input voltage relative to GND (user and dedicated I/Os)	–0.5(2) to 3.45(4)	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	–0.5(3) to 3.45(5)	V
$V_{CCAUXRX}$	Auxilliary supply voltage relative to analog ground, GNDA (Rocket I/O pins)	–0.5 to 3.45	V
$V_{CCAUXTX}$	Auxilliary supply voltage relative to analog ground, GNDA (Rocket I/O pins)	–0.5 to 3.45	V
V_{TTX}	Terminal transmit supply voltage relative to GND (Rocket I/O pins)	–0.5 to 3.45	V
V_{TRX}	Terminal receive supply voltage relative to GND (Rocket I/O pins)	–0.5 to 3.45	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature	+220	°C
T_J	Operating junction temperature	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For 3.3V I/O standards only, I/O input pin voltage, including negative undershoot, must not fall below 0.0V, either on a continuous or transient basis (i.e., no negative undershoot is allowed). See Table 6, page 56.
3. For 3.3V I/O standards only, I/O output pin voltage while in 3-state mode must not fall below 0.0V, either on a continuous or transient basis. See Table 6, page 56.
4. I/O input pin voltage, including overshoot, must not exceed 3.45V, either on a continuous or transient basis.
5. I/O output pin voltage while in 3-state mode must not exceed 3.45V, either on a continuous or transient basis.

Table 2: **Recommended Operating Conditions**

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.425	1.575	V
	Internal supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.425	1.575	V
V_{CCAUX}(1)	Auxiliary supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.375	2.625	V
	Auxiliary supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	2.375	2.625	V
V_{CCO}(2)	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.45(4)	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.45(4)	V
V_{BATT}(3)	Battery voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.0	2.63	V
	Battery voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.0	2.63	V
$V_{CCAUXRX}$, $V_{CCAUXTX}$	Auxilliary supply voltage relative to GNDA	Commercial	2.375	2.625	V
	Auxilliary supply voltage relative to GNDA	Industrial	2.375	2.625	V
V_{TTX}, V_{TRX}	Terminal supply voltage relative to GND	Commercial	1.8	2.625	V
	Terminal supply voltage relative to GND	Industrial	1.8	2.625	V

Notes:
1. For LVDS operation, V_{CCAUX} min is 2.37V and max is 2.63V.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. If battery is not used, do not connect V_{BATT}.
4. For 3.3V operation, see Table 4 in Module 4 for banking information.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Device	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	All	1.2			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	All				V
I_{REF}	V_{REF} current per bank	All				µA
I_L	Input or output leakage current per pin	All				µA
C_{IN}	Input capacitance (sample tested)	All				pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V, V_{CCO} = 3.3V (sample tested)	All	Note (1)			mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6V (sample tested)	All	Note (1)			mA
$I_{CCAUXTX}$	Operating $V_{CCAUXTX}$ supply current			60		mA
$I_{CCAUXRX}$	Operating $V_{CCAUXRX}$ supply current			35		mA
I_{TTX}	Operating I_{TTX} supply current when transmitter is AC coupled			30		mA
	Operating I_{TTX} supply current when transmitter is DC coupled			15		mA
I_{TRX}	Operating I_{TRX} supply current when receiver is AC coupled			TBD		mA
	Operating I_{TRX} supply current when receiver is DC coupled			15		mA

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Continued)***

Symbol	Description	Device	Min	Typ	Max	Units
P_{CPU}	Power dissipation of PowerPC® 405 processor block					mW / MHz
P_{RXTX}	Power dissipation of Rocket I/O @ 3.125 Gb/s per channel			350		mW
	Power dissipation of Rocket I/O @ 2.5 Gb/s per channel			310		mW
	Power dissipation of Rocket I/O @ 1.25 Gb/s per channel			230		mW

Notes:
1. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Min	Typ	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC2VP2				mA
		XC2VP4				mA
		XC2VP7				mA
		XC2VP20				mA
		XC2VP50				mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC2VP2				mA
		XC2VP4				mA
		XC2VP7				mA
		XC2VP20				mA
		XC2VP50				mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC2VP2				mA
		XC2VP4				mA
		XC2VP7				mA
		XC2VP20				mA
		XC2VP50				mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
2. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER™.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply.

The V_{CCINT}, V_{CCAUX}, and V_{CCO} power supplies must ramp on no faster than 100 µs and no slower than 50 ms. Ramp on is defined as: 0 V_{DC} to minimum supply voltages (see Table 2, page 54).

V_{CCAUX} and V_{CCO} for bank 4 must be connected together (2.5 V_{DC}) to meet the following specification.

Table 5, page 56, shows the minimum current required by Virtex-II Pro devices for proper power on and configuration.

Power supplies can be turned on in any sequence, as long as V_{CCAUX} and V_{CCO} are connected together for bank 4.

If any V_{CCO} bank powers up before V_{CCAUX}, then each bank draws up to 600 mA, worst case, until the V_{CCAUX} powers on. This does not harm the device. (Note that the 600 mA is *peak transient current*, which eventually dissipates even if V_{CCAUX} does not power on.)

If the currents minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages. Once initialized and configured, use the power calculator to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-II Pro Devices**

Symbol	Device					Units
	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP50	
$I_{CCINTMIN}$	250	250	250	250	500	mA
$I_{CCAUXMIN}$	250	250	250	250	250	mA
I_{CCOMIN}	10	10	10	10	10	mA

SelectI/O DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	0.0	0.8	2.0	V_{CCO}	0.4	2.4	24	–24
LVCMOS33	0.0	0.8	2.0	V_{CCO}	0.4	V_{CCO} – 0.4	24	–24
LVCMOS25	–0.5	0.7	1.7	V_{CCO} + 0.4	0.4	V_{CCO} – 0.4	24	–24
LVCMOS18	–0.5	20% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
LVCMOS15	–0.5	20% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.4	0.4	V_{CCO} – 0.45	16	–16
PCI33_3(2)	0.0	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}		
PCI66_3(2)	0.0	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}		
GTLP	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.6	n/a	36	n/a
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.4	0.4	n/a	40	n/a
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(3)	V_{CCO} – 0.4	8(3)	–8(3)
HSTL II	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(3)	V_{CCO} – 0.4	16(3)	–16(3)
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(3)	V_{CCO} – 0.4	24(3)	–8(3)
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.4	0.4(3)	V_{CCO} – 0.4	48(3)	–8(3)
SSTL3 I	0.0	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO}	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	0.0	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO}	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.4	V_{REF} – 0.61	V_{REF} + 0.65	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.4	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always CMOS 2.5 12 mA.
2. For optimum performance, it is recommended that PCI be used in conjunction with LVDCI_33. Contact Xilinx for more details.
3. This applies to 1.5V and 1.8V HSTL.

LDT DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Differential Output Voltage	V_{OD}	R_T = 100 ohm across Q and $\overline{Q}$ signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 ohm across Q and $\overline{Q}$ signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.475	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100	350	600	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 9: **Extended LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.38	2.5	2.63	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.70	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.705			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	440		820	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.200	1.275	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25V	100		1000	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Rocket I/O DC Input and Output Levels

Table 10: **Rocket I/O DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-Peak Differential Input Voltage	DV_{IN}			175		mV
Peak-to-Peak Differential Output Voltage(1,2)	DV_{OUT}			800		mV
				1000		mV
				1200		mV
				1400		mV
				1600		mV

Notes:

1. Output swing levels are selectable using TX_DIFF_CTRL attribute. Refer to the *Rocket I/O User Guide* or Chapter 2 in the Virtex-II Pro *Platform FPGA Handbook* for details.
2. Output preemphasis levels are selectable at 10% (default), 20%, 25%, and 33% using the TX_PREEMPHASIS attribute. Refer to the *Rocket I/O User Guide* or Chapter 2 in the Virtex-II Pro *Platform FPGA Handbook* for details.

Virtex-II Pro Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II Pro devices. The numbers reported here are fully characterized worst-case values. Note that these values are subject to the same guidelines as **Virtex-II Pro Switching Characteristics**, page 61 (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: **Pin-to-Pin Performance**

Description	Pin-to-Pin (w/ I/O delays)	Device Used & Speed Grade
Basic Functions:		
16-bit Address Decoder		
32-bit Address Decoder		
64-bit Address Decoder		
4:1 MUX		
8:1 MUX		
16:1 MUX		
32:1 MUX		
Combinatorial (pad to LUT to pad)		
Memory:		
Block RAM		
Pad to setup		
Clock to Pad		
Distributed RAM		
Pad to setup		
Clock to Pad		

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: **Register-to-Register Performance**

Description	Register-to-Register Performance	Device Used & Speed Grade
Basic Functions:		
16-bit Address Decoder		
32-bit Address Decoder		
64-bit Address Decoder		
4:1 MUX		
8:1 MUX		
16:1 MUX		
32:1 MUX		
Register to LUT to Register		
8-bit Adder		
16-bit Adder		

Table 12: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register Performance	Device Used & Speed Grade
64-bit Adder		
64-bit Counter		
64-bit Accumulator		
Multiplier 18x18 (with Block RAM inputs)		
Multiplier 18x18 (with Register inputs)		
Memory:		
Block RAM		
Single-Port 4096 x 4 bits		
Single-Port 2048 x 9 bits		
Single-Port 1024 x 18 bits		
Single-Port 512 x 36 bits		
Dual-Port A:4096 x 4 bits & B:1024 x 18 bits		
Dual-Port A:1024 x 18 bits & B:1024 x 18 bits		
Dual-Port A:2048 x 9 bits & B: 512 x 36 bits		
Distributed RAM		
Single-Port 32 x 8-bit		
Single-Port 64 x 8-bit		
Single-Port 128 x 8-bit		
Dual-Port 16 x 8		
Dual-Port 32 x 8		
Dual-Port 64 x 8		
Dual-Port 128 x 8		
Shift Registers		
128-bit SRL		
256-bit SRL		
FIFOs (Async. in Block RAM)		
1024 x 18-bit		
1024 x 18-bit		
FIFOs (Sync. in SRL)		
128 x 8-bit		
128 x 16-bit		
CAMs in Block RAM		
32 x 9-bit		
64 x 9-bit		
128 x 9-bit		
256 x 9-bit		

Table 12: **Register-to-Register Performance *(Continued)***

Description	Register-to-Register Performance	Device Used & Speed Grade
CAMs in SRL		
32 x 16-bit		
64 x 32-bit		
128 x 40-bit		
256 x 48-bit		
1024 x 16-bit		
1024 x 72-bit		

Virtex-II Pro Switching Characteristics

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that **Virtex-II Pro Performance Characteristics**, page 59 are subject to these guidelines, as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Virtex-II Pro device with a corresponding speed file designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Table 13: **Virtex-II Pro Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2VP2	-8, -7, -6		
XC2VP4	-8, -7, -6		
XC2VP7	-8, -7, -6		
XC2VP20	-8, -7, -6		
XC2VP50	-8, -7, -6		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II Pro devices.

PowerPC Switching Characteristics

Table 14: **Processor Clocks Absolute AC Characteristics**

	Speed Grade						
	-8		-7		-6		
Description	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
CPMC405CLOCK frequency							MHz
JTAGC405TCK frequency(1)							MHz

Notes:
1. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is dependent on the system, and will be much less

Table 15: **Processor Block Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (CPMC405CLOCK)					
Device Control Register Bus control inputs	$T_{PCCK\_}DCR/T_{PCKC\_}DCR$				ns, min
Device Control Register Bus data inputs	$T_{PDCK\_}DCR/T_{PCKD\_}DCR$				ns, min
Clock and Power Management control inputs	$T_{PCCK\_}CPM/T_{PCKC\_}CPM$				ns, min
Reset control inputs	$T_{PCCK\_}RST/T_{PCKC\_}RST$				ns, min
Debug control inputs	$T_{PCCK\_}DBG/T_{PCKC\_}DBG$				ns, min
Trace control inputs	$T_{PCCK\_}TRC/T_{PCKC\_}TRC$				ns, min
External Interrupt Controller control inputs	$T_{PCCK\_}EIC/T_{PCKC\_}EIC$				ns, min
Clock to Out					
Device Control Register Bus control outputs	$T_{PCKCO\_}DCR$				ns, max
Device Control Register Bus address outputs	$T_{PCKAO\_}DCR$				ns, max
Device Control Register Bus data outputs	$T_{PCKDO\_}DCR$				ns, max
Clock and Power Management control outputs	$T_{PCKCO\_}CPM$				ns, max
Reset control outputs	$T_{PCKCO\_}RST$				ns, max
Debug control outputs	$T_{PCKCO\_}DBG$				ns, max
Trace control outputs	$T_{PCKCO\_}TRC$				ns, max

Table 15: **Processor Block Switching Characteristics *(Continued)***

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Clock					
CPMC405CLOCK minimum pulse width, high	T_{CPWH}				ns, min
CPMC405CLOCK minimum pulse width, low	T_{CPWL}				ns, min

Table 16: **Processor Block PLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (PLBCLK)					
Processor Local Bus(ICU/DCU) control inputs	$T_{PCCK\_}PLB/T_{PCKC\_}PLB$				ns, min
Processor Local Bus (ICU/DCU) data inputs	$T_{PDCK\_}PLB/T_{PCKD\_}PLB$				ns, min
Clock to Out					
Processor Local Bus(ICU/DCU) control outputs	$T_{PCKCO\_}PLB$				ns, max
Processor Local Bus(ICU/DCU) address bus outputs	$T_{PCKAO\_}PLB$				ns, max
Processor Local Bus(ICU/DCU) data bus outputs	$T_{PCKDO\_}PLB$				ns, max
Clock					
PLBCLK minimum pulse width, high	T_{PPWH}				ns, min
PLBCLK minimum pulse width, low	T_{PPWL}				ns, min

Table 17: **Processor Block JTAG Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (JTAGC405TCK)					
JTAG control inputs	$T_{PCCK\_}JTAG/T_{PCKC\_}JTAG$				ns, min
JTAG reset input	$T_{PCCK\_}JTAGRST/$ $T_{PCKC\_}JTAGRST$				ns, min
Clock to Out					
JTAG control outputs	$T_{PCKCO\_}JTAG$				ns, max

Table 17: **Processor Block JTAG Switching Characteristics *(Continued)***

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Clock					
JTAGC405TCK minimum pulse width, high	T_{JPWH}				ns, min
JTAGC405TCK minimum pulse width, low	T_{JPWL}				ns, min

Table 18: **PowerPC 405 Data-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (BRAMDSOCMCLK)					
Data-Side On-Chip Memory data bus inputs	$T_{PDCK_}$DSOCM/$T_{PCKD_}$DSOCM				ns, min
Clock to Out					
Data-Side On-Chip Memory control outputs	$T_{PCKCO_}$DSOCM				ns, max
Data-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$DSOCM				ns, max
Data-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$DSOCM				ns, max
Clock					
BRAMDSOCMCLK minimum pulse width, high	T_{DPWH}				ns, min
BRAMDSOCMCLK minimum pulse width, low	T_{DPWL}				ns, min

Table 19: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (BRAMISOCMCLK)					
Instruction-Side On-Chip Memory data bus inputs	$T_{PDCK_}$ISOCM/$T_{PCKD_}$ISOCM				ns, min
Clock to Out					
Instruction-Side On-Chip Memory control outputs	$T_{PCKCO_}$ISOCM				ns, max
Instruction-Side On-Chip Memory address bus outputs	$T_{PCKAO_}$ISOCM				ns, max
Instruction-Side On-Chip Memory data bus outputs	$T_{PCKDO_}$ISOCM				ns, max

Table 19: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics *(Continued)***

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Clock					
BRAMISOCMCLK minimum pulse width, high	T_{IPWH}				ns, min
BRAMISOCMCLK minimum pulse width, low	T_{IPWL}				ns, min

Rocket I/O Switching Characteristics

Table 20: **Rocket I/O Reference Clock Switching Characteristics**

			All Speed Grades			
Description	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
REFCLK frequency range(1)	F_{GCLK}		40	Note(1)	156.25	MHz
REFCLK frequency tolerance	F_{GTOL}				±100	ppm
REFCLK rise time	T_{RCLK}	20% – 80%				ns
REFCLK fall time	T_{FCLK}	20% – 80%				ns
REFCLK duty cycle	T_{DCREF}		45	50	55	%
REFCLK total jitter	T_{GJTT}	peak-to-peak			40	ps
Clock recovery frequency acquisition time	T_{LOCK}			10		µs
Clock recovery phase acquisition time	T_{PHASE}			960		bits
Bit error rate	BER				10^{-12}	

Notes:
1. REFCLK frequency is typically 1/20 of serial data rate.

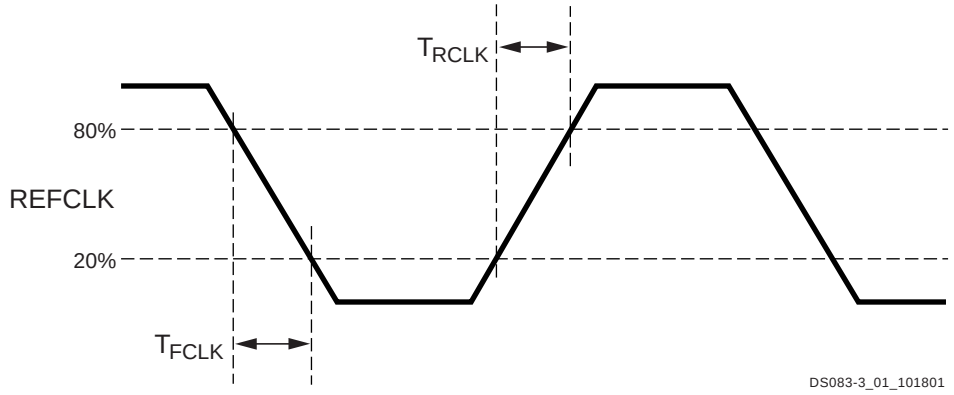

Figure 1: **Reference Clock (REFCLK) Timing Parameters**

Table 21: **Rocket I/O Receiver Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Receive total jitter tolerance	T_{JTOL}				0.65	UI(1)
Receive deterministic jitter tolerance	T_{DJTOL}				0.41	UI
Receive latency(2)	T_{RXLAT}			25	42	RXUSRCLK cycles
RXUSRCLK duty cycle	T_{RXDC}		45	50	55	%
RXUSRCLK2 duty cycle	T_{RX2DC}		45	50	55	%
Bit error rate	BER				10^{-12}	

Notes:
1. UI = Unit Interval
2. Receive latency delay from RXP/RXN to RXDATA

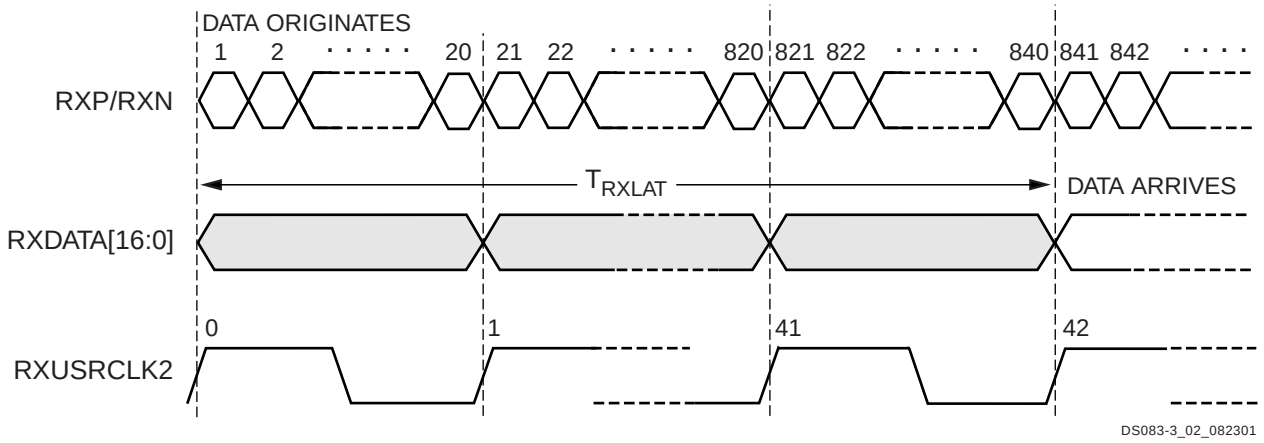

Figure 2: **Receive Latency (Maximum)**

Table 22: **Rocket I/O Transmitter Switching Characteristics**

Description	Symbol	Conditions	Min	Typ	Max	Units
Serial data rate, full-speed clock	F_{GTX}	Flipchip packages	0.800		3.125	Gb/s
		Wirebond packages	0.800		2.5	Gb/s
Serial data rate, half-speed clock		Flipchip packages	0.600		1.0	Gb/s
		Wirebond packages	0.600		1.0	Gb/s
Serial data output deterministic jitter	T_{DJ}				0.18	UI(1)
Serial data output random jitter	T_{RJ}				0.17	UI
TX rise time	T_{RTX}	20% – 80%		120		ps
TX fall time	T_{FTX}			120		ps
Transmit latency(2)	T_{TXLAT}	Including CRC		14	17	TXUSRCLK cycles
		Excluding CRC		8	11	
TXUSRCLK duty cycle	T_{TXDC}		45	50	55	%
TXUSRCLK2 duty cycle	T_{TX2DC}		45	50	55	%

Notes:
1. UI = Unit Interval
2. Transmit latency delay from TXDATA to TXP/TXN

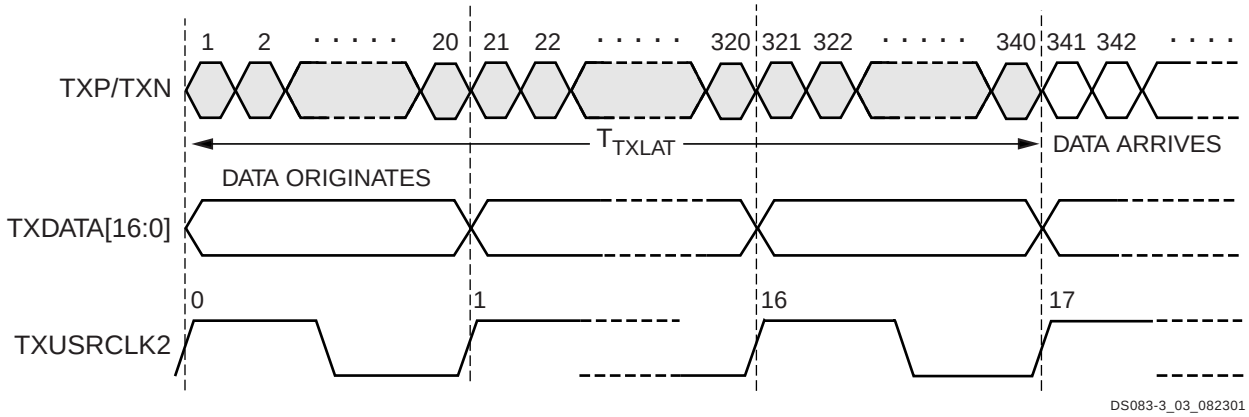

Figure 3: **Transmit Latency (Maximum, Including CRC)**

Table 23: **Rocket I/O RXUSRCLK Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (RXUSRCLK)					
CHBONDI control inputs	$T_{GCCK\_}CHBI/T_{GCKC\_}CHBI$				ns, min
Clock to Out					
CHBONDO control outputs	$T_{GCKCO\_}CHBO$				ns, max
Clock					
RXUSRCLK minimum pulse width, High	$T_{GPWH\_}RX$				ns, min
RXUSRCLK minimum pulse width, Low	$T_{GPWL\_}RX$				ns, min

Table 24: **Rocket I/O RXUSRCLK2 Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (RXUSRCLK2)					
RXRESET control input	$T_{GCCK\_}RRST/T_{GCKC\_}RRST$				ns, min
RXPOLARITY control input	$T_{GCCK\_}RPOL/T_{GCKC\_}RPOL$				ns, min
ENCHANSYNC control input	$T_{GCCK\_}ECSY/T_{GCKC\_}ECSY$				ns, min
Clock to Out					
RXNOTINTABLE status outputs	$T_{GCKST\_}RNIT$				ns, max
RXDISPERR status outputs	$T_{GCKST\_}RDERR$				ns, max
RXCHARISCOMMA status outputs	$T_{GCKST\_}RCMCH$				ns, max
RXREALIGN status output	$T_{GCKST\_}ALIGN$				ns, max
RXCOMMADET status output	$T_{GCKST\_}CMDT$				ns, max
RXLOSSOFSYNC status outputs	$T_{GCKST\_}RLOS$				ns, max
RXCLKCORCNT status outputs	$T_{GCKST\_}RCCCNT$				ns, max
RXBUFSTATUS status outputs	$T_{GCKST\_}RBSTA$				ns, max
RXCHECKINGCRC status output	$T_{GCKST\_}RCCRC$				ns, max
RXCRCERR status output	$T_{GCKST\_}RCRCE$				ns, max
CHBONDDONE status output	$T_{GCKST\_}CHBD$				ns, max
RXCHARISK status outputs	$T_{GCKST\_}RKCH$				ns, max
RXRUNDISP status outputs	$T_{GCKST\_}RRDIS$				ns, max
RXDATA data outputs	$T_{GCKDO\_}RDAT$				ns, max
Clock					
RXUSRCLK2 minimum pulse width, High	$T_{GPWH\_}RX2$				ns, min
RXUSRCLK2 minimum pulse width, Low	$T_{GPWL\_}RX2$				ns, min

Table 25: **Rocket I/O TXUSRCLK Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Setup and Hold Relative to Clock (TXUSRCLK2)					
CONFIGENABLE control input	$T_{GCCK\_}CFGEN/T_{GCKC\_}CFGEN$				ns, min
TXBYPASS8B10B control inputs	$T_{GCCK\_}TBYP/T_{GCKC\_}TBYP$				ns, min
TXFORCECRCERR control input	$T_{GCCK\_}TCRCE/T_{GCKC\_}TCRCE$				ns, min
TXPOLARITY control input	$T_{GCCK\_}TPOL/T_{GCKC\_}TPOL$				ns, min
TXINHIBIT control inputs	$T_{GCCK\_}TINH/T_{GCKC\_}TINH$				ns, min
LOOPBACK control inputs	$T_{GCCK\_}LBK/T_{GCKC\_}LBK$				ns, min
TXRESET control input	$T_{GCCK\_}TRST/T_{GCKC\_}TRST$				ns, min
TXCHARISK control inputs	$T_{GCCK\_}TKCH/T_{GCKC\_}TKCH$				ns, min
TXCHARDISPMODE control inputs	$T_{GCCK\_}TCDM/T_{GCKC\_}TCDM$				ns, min
TXCHARDISPVAL control inputs	$T_{GCCK\_}TCDV/T_{GCKC\_}TCDV$				ns, min
CONFIGIN data input	$T_{GDCK\_}CFGIN/T_{GCKD\_}CFGIN$				ns, min
TXDATA data inputs	$T_{GDCK\_}TDAT/T_{GCKD\_}TDAT$				ns, min
Clock to Out					
TXBUFERR status output	$T_{GCKST\_}TBERR$				ns, max
TXKERR status outputs	$T_{GCKST\_}TKERR$				ns, max
TXRUNDISP status outputs	$T_{GCKST\_}TRDIS$				ns, max
CONFIGOUT data output	$T_{GCKDO\_}CFGOUT$				ns, max
Clock					
TXUSRCLK minimum pulse width, High	$T_{GPWH\_}TX$				ns, min
TXUSRCLK minimum pulse width, Low	$T_{GPWL\_}TX$				ns, min
TXUSRCLK2 minimum pulse width, High	$T_{GPWH\_}TX2$				ns, min
TXUSRCLK2 minimum pulse width, Low	$T_{GPWL\_}TX2$				ns, min

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVCMOS 2.5V levels. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 71.

Table 26: **IOB Input Switching Characteristics**

			Speed Grade			
Description	**Symbol**	**Device**	**–8**	**–7**	**–6**	**Units**
Propagation Delays						
Pad to I output, no delay	T_{IOPI}	All				ns, max
Pad to I output, with delay	T_{IOPID}	XC2VP2				ns, max
		XC2VP4				ns, max
		XC2VP7				ns, max
		XC2VP20				ns, max
		XC2VP50				ns, max
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All				ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2VP2				ns, max
		XC2VP4				ns, max
		XC2VP7				ns, max
		XC2VP20				ns, max
		XC2VP50				ns, max
Clock CLK to output IQ	T_{IOCKIQ}	All				ns, max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All				ns, min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2VP2				ns, max
		XC2VP4				ns, max
		XC2VP7				ns, max
		XC2VP20				ns, max
		XC2VP50				ns, max
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All				ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All				ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All				ns, max
GSR to output IQ	T_{GSRQ}	All				ns, max

Notes:
1. Input timing for LVCMOS25 is measured at 1.25V. For other I/O standards, see Table 30.

IOB Input Switching Characteristics Standard Adjustments

Table 27: **IOB Input Switching Characteristics Standard Adjustments**

			Speed Grade			
Description	**Symbol**	**Standard**	**–8**	**–7**	**–6**	**Units**
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL				ns
	$T_{ILVCMOS33}$	LVCMOS33				ns
	$T_{ILVCMOS25}$	LVCMOS25				ns
	$T_{ILVCMOS18}$	LVCMOS18				ns
	$T_{ILVCMOS15}$	LVCMOS15				ns
	T_{ILVDS_25}	LVDS_25				ns
	$T_{ILVDS\_25\_EXT}$	LVDS_25_EXT				ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3V				ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3V				ns
	T_{IGTL}	GTL				ns
	$T_{IGTLPLUS}$	GTLP				ns
	T_{IHSTL_I}	HSTL I				ns
	T_{IHSTL_II}	HSTL II				ns
	T_{IHSTL_III}	HSTL III				ns
	T_{IHSTL_IV}	HSTL IV				ns
	$T_{IHSTL\_I\_18}$	HSTL_I_18				ns
	$T_{IHSTL\_II\_18}$	HSTL_II_18				ns
	$T_{IHSTL\_III\_18}$	HSTL_III_18				ns
	$T_{IHSTL\_IV\_18}$	HSTL_IV_18				ns
	T_{ISSTL2_I}	SSTL2 I				ns
	T_{ISSTL2_II}	SSTL2 II				ns
	T_{ISSTL3_I}	SSTL3 I				ns
	T_{ISSTL3_II}	SSTL3 II				ns
	$T_{ILVDCI33}$	LVDCI_33				ns
	$T_{ILVDCI25}$	LVDCI_25				ns
	$T_{ILVDCI18}$	LVDCI_18				ns
	$T_{ILVDCI15}$	LVDCI_15				ns
	$T_{ILVDCI\_DV2\_25}$	LVDCI_DV2_25				ns
	$T_{ILVDCI\_DV2\_18}$	LVDCI_DV2_18				ns
	$T_{ILVDCI\_DV2\_15}$	LVDCI_DV2_15				ns
	T_{IGTL_DCI}	GTL_DCI				ns
	T_{IGTLP_DCI}	GTLP_DCI				ns
	$T_{IHSTL\_I\_DCI}$	HSTL_I_DCI				ns

Table 27: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–8**	**–7**	**–6**	**Units**
Standard-specific data input delay adjustments *(continued)*	$T_{IHSTL\_II\_DCI}$	HSTL_II_DCI				ns
	$T_{IHSTL\_III\_DCI}$	HSTL_III_DCI				ns
	$T_{IHSTL\_IV\_DCI}$	HSTL_IV_DCI				ns
	$T_{IHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18				ns
	$T_{IHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18				ns
	$T_{IHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18				ns
	$T_{IHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18				ns
	$T_{ISSTL2\_I\_DCI}$	SSTL2_I_DCI				ns
	$T_{ISSTL2\_II\_DCI}$	SSTL2_II_DCI				ns
	$T_{ISSTL3\_I\_DCI}$	SSTL3_I_DCI				ns
	$T_{ISSTL3\_II\_DCI}$	SSTL3_II_DCI				ns
	T_{ILDT_25}	LDT_25				ns
	T_{IULVDS_25}	ULVDS_25				ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see Table 30.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 73.

Table 28: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–8**	**–7**	**–6**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}				ns, max
O input to Pad via transparent latch	T_{IOOLP}				ns, max
3-State Delays					
T input to Pad high-impedance(2)	T_{IOTHZ}				ns, max
T input to valid data on Pad	T_{IOTON}				ns, max
T input to Pad high-impedance via transparent latch(2)	$T_{IOTLPHZ}$				ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$				ns, max
GTS to Pad high-impedance(2)	T_{GTS}				ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}				ns, max
Clock CLK to Pad high-impedance (synchronous)(2)	T_{IOCKHZ}				ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}				ns, max

Table 28: **IOB Output Switching Characteristics *(Continued)***

Description	Symbol	Speed Grade			Units
		–8	–7	–6	
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}				ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$				ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$				ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}				ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$				ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$				ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}				ns, max
SR input to Pad high-impedance (asynchronous)(2)	T_{IOSRHZ}				ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}				ns, max
GSR to Pad	T_{IOGSRQ}				ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. The 3-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVCMOS25 with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 29: **IOB Output Switching Characteristics Standard Adjustments**

Description	Symbol	Standard	Speed Grade			Units
			–8	–7	–6	
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA				ns
	T_{OLVTTL_S4}	4 mA				ns
	T_{OLVTTL_S6}	6 mA				ns
	T_{OLVTTL_S8}	8 mA				ns
	T_{OLVTTL_S12}	12 mA				ns
	T_{OLVTTL_S16}	16 mA				ns
	T_{OLVTTL_S24}	24 mA				ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA				ns
	T_{OLVTTL_F4}	4 mA				ns
	T_{OLVTTL_F6}	6 mA				ns
	T_{OLVTTL_F8}	8 mA				ns
	T_{OLVTTL_F12}	12 mA				ns

Table 29: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–8**	**–7**	**–6**	**Units**
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) *(continued)*	T_{OLVTTL_F16}	16 mA				ns
	T_{OLVTTL_F24}	24 mA				ns
	T_{OLVDS_25}	LVDS				ns
	$T_{OLVDSEXT\_25}$	LVDS				ns
	T_{OLDT_25}	LDT				ns
	T_{OBLVDS_25}	BLVDS				ns
	T_{OULVDS_25}	ULVDS				ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3V				ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3V				ns
	T_{OGTL}	GTL				ns
	T_{OGTLP}	GTLP				ns
	T_{OHSTL_I}	HSTL I				ns
	T_{OHSTL_II}	HSTL II				ns
	T_{OHSTL_IIII}	HSTL III				ns
	T_{OHSTL_IV}	HSTL IV				ns
	$T_{OHSTL\_I\_18}$	HSTL_I_18				ns
	$T_{OHSTL\_II\_18}$	HSTL_II_18				ns
	$T_{OHSTL\_IIII\_18}$	HSTL_III_18				ns
	$T_{OHSTL\_IV\_18}$	HSTL_IV_18				ns
	T_{OSSTL2_I}	SSTL2 I				ns
	T_{OSSTL2_II}	SSTL2 II				ns
	T_{OSSTL3_I}	SSTL3 I				ns
	T_{OSSTL3_II}	SSTL3 II				ns
	$T_{OLVCMOS33\_S2}$	LVCMOS33, Slow, 2 mA				ns
	$T_{OLVCMOS33\_S4}$	4 mA				ns
	$T_{OLVCMOS33\_S6}$	6 mA				ns
	$T_{OLVCMOS33\_S8}$	8 mA				ns
	$T_{OLVCMOS33\_S12}$	12 mA				ns
	$T_{OLVCMOS33\_S16}$	16 mA				ns
	$T_{OLVCMOS33\_S24}$	24 mA				ns
	$T_{OLVCMOS33\_F2}$	LVCMOS33, Fast, 2 mA				ns
	$T_{OLVCMOS33\_F4}$	4 mA				ns
	$T_{OLVCMOS33\_F6}$	6 mA				ns
	$T_{OLVCMOS33\_F8}$	8 mA				ns
	$T_{OLVCMOS33\_F12}$	12 mA				ns

Table 29: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–8**	**–7**	**–6**	**Units**
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) *(continued)*	$T_{OLVCMOS33\_F16}$	16 mA				ns
	$T_{OLVCMOS33\_F24}$	24 mA				ns
	$T_{OLVCMOS25\_S2}$	LVCMOS25, Slow, 2 mA				ns
	$T_{OLVCMOS25\_S4}$	4 mA				ns
	$T_{OLVCMOS25\_S6}$	6 mA				ns
	$T_{OLVCMOS25\_S8}$	8 mA				ns
	$T_{OLVCMOS25\_S12}$	12 mA				ns
	$T_{OLVCMOS25\_S16}$	16 mA				ns
	$T_{OLVCMOS25\_S24}$	24 mA				ns
	$T_{OLVCMOS25\_F2}$	LVCMOS25, Fast, 2 mA				ns
	$T_{OLVCMOS25\_F4}$	4 mA				ns
	$T_{OLVCMOS25\_F6}$	6 mA				ns
	$T_{OLVCMOS25\_F8}$	8 mA				ns
	$T_{OLVCMOS25\_F12}$	12 mA				ns
	$T_{OLVCMOS25\_F16}$	16 mA				ns
	$T_{OLVCMOS25\_F24}$	24 mA				ns
	$T_{OLVCMOS18\_S2}$	LVCMOS18, Slow, 2 mA				ns
	$T_{OLVCMOS18\_S4}$	4 mA				ns
	$T_{OLVCMOS18\_S6}$	6 mA				ns
	$T_{OLVCMOS18\_S8}$	8 mA				ns
	$T_{OLVCMOS18\_S12}$	12 mA				ns
	$T_{OLVCMOS18\_S16}$	16 mA				ns
	$T_{OLVCMOS18\_F2}$	LVCMOS18, Fast, 2 mA				ns
	$T_{OLVCMOS18\_F4}$	4 mA				ns
	$T_{OLVCMOS18\_F6}$	6 mA				ns
	$T_{OLVCMOS18\_F8}$	8 mA				ns
	$T_{OLVCMOS18\_F12}$	12 mA				ns
	$T_{OLVCMOS18\_F16}$	16 mA				ns
	$T_{OLVCMOS15\_S2}$	LVCMOS15, Slow, 2 mA				ns
	$T_{OLVCMOS15\_S4}$	4 mA				ns
	$T_{OLVCMOS15\_S6}$	6 mA				ns
	$T_{OLVCMOS15\_S8}$	8 mA				ns
	$T_{OLVCMOS15\_S12}$	12 mA				ns
	$T_{OLVCMOS15\_S16}$	16 mA				ns

Table 29: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

			Speed Grade			
Description	**Symbol**	**Standard**	**–8**	**–7**	**–6**	**Units**
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) *(continued)*	$T_{OLVCMOS15\_F2}$	LVCMOS15, Fast, 2 mA				ns
	$T_{OLVCMOS15\_F4}$	4 mA				ns
	$T_{OLVCMOS15\_F6}$	6 mA				ns
	$T_{OLVCMOS15\_F8}$	8 mA				ns
	$T_{OLVCMOS15\_F12}$	12 mA				ns
	$T_{OLVCMOS15\_F16}$	16 mA				ns
	$T_{OLVDCI33}$	LVDCI_33				ns
	$T_{OLVDCI25}$	LVDCI_25				ns
	$T_{OLVDCI18}$	LVDCI_18				ns
	$T_{OLVDCI15}$	LVDCI_15				ns
	$T_{OLVDCI\_DV2\_25}$	LVDCI_DV2_25				ns
	$T_{OLVDCI\_DV2\_18}$	LVDCI_DV2_18				ns
	$T_{OLVDCI\_DV2\_15}$	LVDCI_DV2_15				ns
	T_{OGTL_DCI}	GTL_DCI				ns
	T_{OGTLP_DCI}	GTLP_DCI				ns
	$T_{OHSTL\_I\_DCI}$	HSTL_I_DCI				ns
	$T_{OHSTL\_II\_DCI}$	HSTL_II_DCI				ns
	$T_{OHSTL\_III\_DCI}$	HSTL_III_DCI				ns
	$T_{OHSTL\_IV\_DCI}$	HSTL_IV_DCI				ns
	$T_{OHSTL\_I\_DCI\_18}$	HSTL_I_DCI_18				ns
	$T_{OHSTL\_II\_DCI\_18}$	HSTL_II_DCI_18				ns
	$T_{OHSTL\_III\_DCI\_18}$	HSTL_III_DCI_18				ns
	$T_{OHSTL\_IV\_DCI\_18}$	HSTL_IV_DCI_18				ns
	$T_{OSSTL2\_I\_DCI}$	SSTL2_I_DCI				ns
	$T_{OSSTL2\_II\_DCI}$	SSTL2_II_DCI				ns
	$T_{OSSTL3\_I\_DCI}$	SSTL3_I_DCI				ns
	$T_{OSSTL3\_II\_DCI}$	SSTL3_II_DCI				ns

Table 30: **Delay Measurement Methodology**

Standard	V_L (1)	V_H (1)	Meas. Point	V_{REF} (Typ) (2)
LVTTL	0	3	1.4	–
LVCMOS33	0	3.3	1.65	–
LVCMOS25	0	2.5	1.25	–
LVCMOS18	0	1.8	0.9	–
LVCMOS15	0	1.5	0.75	–
PCI33_3	Per PCI Specification			–
PCI66_3	Per PCI Specification			–
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class I (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
HSTL Class II (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
HSTL Class III (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
HSTL Class IV (1.8V)	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL3 I & II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

Table 31: **Standard Capacitive Loads**

Standard	Csl (pF)
LVTTL Fast Slew Rate, 2mA drive	35
LVTTL Fast Slew Rate, 4mA drive	35
LVTTL Fast Slew Rate, 6mA drive	35
LVTTL Fast Slew Rate, 8mA drive	35
LVTTL Fast Slew Rate, 12mA drive	35
LVTTL Fast Slew Rate, 16mA drive	35
LVTTL Fast Slew Rate, 24mA drive	35
LVTTL Slow Slew Rate, 2mA drive	35
LVTTL Slow Slew Rate, 4mA drive	35
LVTTL Slow Slew Rate, 6mA drive	35
LVTTL Slow Slew Rate, 8mA drive	35
LVTTL Slow Slew Rate, 12mA drive	35
LVTTL Slow Slew Rate, 16mA drive	35
LVTTL Slow Slew Rate, 24mA drive	35
LVCMOS33	35
LVCMOS25	35
LVCMOS18	35
LVCMOS15	35
PCI 33MHZ 3.3V	10
PCI 66 MHz 3.3V	10
GTL	0
GTLP	0
HSTL Class I (1.5V and 1.8V)	20
HSTL Class II (1.5Vand 1.8V	20
HSTL Class III (1.5Vand 1.8V	20
HSTL Class IV1.5Vand 1.8V	20
SSTL2 Class I	30
SSTL2 Class II	30
SSTL3 Class I	30
SSTL3 Class II	30

Notes:
1. I/O parameter measurements are made with the capacitance values shown above.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.
3. Use of IBIS models results in a more accurate prediction of the propagation delay:
   a. Model the output in an IBIS simulation into the standard capacitive load.
   b. Record the relative time to the V_{OH} or V_{OL} transition of interest.
   c. Remove the capacitance, and model the actual PCB traces (transmission lines) and actual loads from the appropriate IBIS models for driven devices.
   d. Record the results from the new simulation.
   e. Compare with the capacitance simulation. The increase or decrease in delay from the capacitive load delay simulation should be added or subtracted from the value above to predict the actual delay.

Clock Distribution Switching Characteristics

Table 32: **Clock Distribution Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–8**	**–7**	**–6**	**Units**
Global Clock Buffer I input to O output	T_{GIO}				ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 22 in Data Sheet Module 1). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 33: **CLB Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–8**	**–7**	**–6**	**Units**
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}				ns, max
5-input function: F/G inputs to F5 output	T_{IF5}				ns, max
5-input function: F/G inputs to X output	T_{IF5X}				ns, max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}				ns, max
FXINA input to FX output via MUXFX	T_{INAFX}				ns, max
FXINB input to FX output via MUXFX	T_{INBFX}				ns, max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}				ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}				ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}				ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}				ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}				ns, min
DY inputs	T_{DYCK}/T_{CKDY}				ns, min
DX inputs	T_{DXCK}/T_{CKDX}				ns, min
CE input	T_{CECK}/T_{CKCE}				ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}				ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}				ns, min
Minimum Pulse Width, Low	T_{CL}				ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}				ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}				ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}				MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Table 34: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–8	–7	–6	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$				ns, max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$				ns, max
Clock CLK to F5 output	$T_{SHCKOF5}$				ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}				ns, min
F/G address inputs	T_{AS}/T_{AH}				ns, min
CE input (WE)	T_{WES}/T_{WEH}				ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}				ns, min
Minimum Pulse Width, Low	T_{WPL}				ns, min
Minimum clock period to meet address write cycle time	T_{WC}				ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Shift Register Switching Characteristics

Table 35: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–8	–7	–6	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}				ns, max
Clock CLK to X/Y outputs	T_{REG32}				ns, max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}				ns, max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}				ns, max
Clock CLK to Shiftout	T_{CKSH}				ns, max
Clock CLK to F5 output	T_{REGF5}				ns, max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}				ns, min
CE input (WS)	T_{WSS}/T_{WSH}				ns, min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}				ns, min
Minimum Pulse Width, Low	T_{SRPL}				ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Multiplier Switching Characteristics

Table 36: **Multiplier Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**–8**	**–7**	**–6**	**Units**
Propagation Delay to Output Pin					
Input to Pin35	T_{MULT_P35}				ns, max
Input to Pin34	T_{MULT_P34}				ns, max
Input to Pin33	T_{MULT_P33}				ns, max
Input to Pin32	T_{MULT_P32}				ns, max
Input to Pin31	T_{MULT_P31}				ns, max
Input to Pin30	T_{MULT_P30}				ns, max
Input to Pin29	T_{MULT_P29}				ns, max
Input to Pin28	T_{MULT_P28}				ns, max
Input to Pin27	T_{MULT_P27}				ns, max
Input to Pin26	T_{MULT_P26}				ns, max
Input to Pin25	T_{MULT_P25}				ns, max
Input to Pin24	T_{MULT_P24}				ns, max
Input to Pin23	T_{MULT_P23}				ns, max
Input to Pin22	T_{MULT_P22}				ns, max
Input to Pin21	T_{MULT_P21}				ns, max
Input to Pin20	T_{MULT_P20}				ns, max
Input to Pin19	T_{MULT_P19}				ns, max
Input to Pin18	T_{MULT_P18}				ns, max
Input to Pin17	T_{MULT_P17}				ns, max
Input to Pin16	T_{MULT_P16}				ns, max
Input to Pin15	T_{MULT_P15}				ns, max
Input to Pin14	T_{MULT_P14}				ns, max
Input to Pin13	T_{MULT_P13}				ns, max
Input to Pin12	T_{MULT_P12}				ns, max
Input to Pin11	T_{MULT_P11}				ns, max
Input to Pin10	T_{MULT_P10}				ns, max
Input to Pin9	T_{MULT_P9}				ns, max
Input to Pin8	T_{MULT_P8}				ns, max
Input to Pin7	T_{MULT_P7}				ns, max
Input to Pin6	T_{MULT_P6}				ns, max
Input to Pin5	T_{MULT_P5}				ns, max
Input to Pin4	T_{MULT_P4}				ns, max
Input to Pin3	T_{MULT_P3}				ns, max
Input to Pin2	T_{MULT_P2}				ns, max
Input to Pin1	T_{MULT_P1}				ns, max
Input to Pin0	T_{MULT_P0}				ns, max

Block SelectRAM Switching Characteristics

Table 37: **Block SelectRAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–8	–7	–6	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}				ns, max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}				ns, min
DIN inputs	T_{BDCK}/T_{BCKD}				ns, min
EN input	T_{BECK}/T_{BCKE}				ns, min
RST input	T_{BRCK}/T_{BCKR}				ns, min
WEN input	T_{BWCK}/T_{BCKW}				ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}				ns, min
Minimum Pulse Width, Low	T_{BPWL}				ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Table 38: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–8	–7	–6	
Combinatorial Delays					
IN input to OUT output	T_{IO}				ns, max
TRI input to OUT output high-impedance	T_{OFF}				ns, max
TRI input to valid data on OUT output	T_{ON}				ns, max

JTAG Test Access Port Switching Characteristics

Table 39: **JTAG Test Access Port Switching Characteristics**

Description	Symbol	Speed Grade			Units
		–8	–7	–6	
TMS and TDI Setup times before TCK	T_{TAPTK}				ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}				ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}				ns, max
Maximum TCK clock frequency	F_{TCK}				MHz, max

Virtex-II Pro Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM

Table 40: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**–8**	**–7**	**–6**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 73.						
Global Clock and OFF with DCM	$T_{ICKOFDCM}$	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP50				ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 30.
3. DCM output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM

Table 41: **Global Clock Input to Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**–8**	**–7**	**–6**	**Units**
LVCMOS25 Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 73.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP50				ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 30.
3. DCM output jitter is already included in the timing calculation.

Virtex-II Pro Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM

Table 42: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *With* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**–8**	**–7**	**–6**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 71.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP50				ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DCM output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM

Table 43: **Global Clock Set-Up and Hold for LVCMOS25 Standard, *Without* DCM**

			Speed Grade			
Description	**Symbol**	**Device**	**–8**	**–7**	**–6**	**Units**
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 71.						
Full Delay Global Clock and IFF without DCM	T_{PSFD}/T_{PHFD}	XC2VP2				ns
		XC2VP4				ns
		XC2VP7				ns
		XC2VP20				ns
		XC2VP50				ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DCM Timing Parameters

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605; all devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins.

Operating Frequency Ranges

Table 44: **Operating Frequency Ranges**

			Speed Grade			
Description	**Symbol**	**Constraints**	**-8**	**-7**	**-6**	**Units**
Output Clocks (Low Frequency Mode)						
CLK0, CLK90, CLK180, CLK270	CLKOUT_FREQ_1X_LF_MIN					MHz
	CLKOUT_FREQ_1X_LF_MAX					MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_LF_MIN					MHz
	CLKOUT_FREQ_2X_LF_MAX					MHz
CLKDV	CLKOUT_FREQ_DV_LF_MIN					MHz
	CLKOUT_FREQ_DV_LF_MAX					MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_LF_MIN					MHz
	CLKOUT_FREQ_FX_LF_MAX					MHz

Table 44: **Operating Frequency Ranges *(Continued)***

			Speed Grade			
Description	**Symbol**	**Constraints**	**-8**	**-7**	**-6**	**Units**
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs)(1)	CLKIN_FREQ_DLL_LF_MIN					MHz
	CLKIN_FREQ_DLL_LF_MAX					MHz
CLKIN (using CLKFX outputs)(2)	CLKIN_FREQ_FX_LF_MIN					MHz
	CLKIN_FREQ_FX_LF_MAX					MHz
PSCLK	PSCLK_FREQ_LF_MIN					MHz
	PSCLK_FREQ_LF_MAX					MHz
Output Clocks (High Frequency Mode)						
CLK0, CLK180	CLKOUT_FREQ_1X_HF_MIN					MHz
	CLKOUT_FREQ_1X_HF_MAX					MHz
CLKDV	CLKOUT_FREQ_DV_HF_MIN					MHz
	CLKOUT_FREQ_DV_HF_MAX					MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_MIN					MHz
	CLKOUT_FREQ_FX_HF_MAX					MHz
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs)(1)	CLKIN_FREQ_DLL_HF_MIN					MHz
	CLKIN_FREQ_DLL_HF_MAX					MHz
CLKIN (using CLKFX outputs)(2)	CLKIN_FREQ_FX_HF_MIN					MHz
	CLKIN_FREQ_FX_HF_MAX					MHz
PSCLK	PSCLK_FREQ_HF_MIN					MHz
	PSCLK_FREQ_HF_MAX					MHz

Notes:
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.

Input Clock Tolerances

Table 45: **Input Clock Tolerances**

			Speed Grade						
			–8		–7		–6		
Description	**Symbol**	**Constraints**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Low/high Pulse Width									
PSCLK CLKIN(3)	PSCLK_PULSE CLKIN_PULSE	< 1MHz							ns
		1 - 10 MHz							ns
		10 - 25 MHz							ns
		25 - 50 MHz							ns
		50 - 100 MHz							ns
		100 - 150 MHz							ns
		150 - 200 MHz							ns
		200 - 250 MHz							ns
		250 - 300 MHz							ns
		300 - 350 MHz							ns
		350 - 400 MHz							ns
		> 400 MHz							ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF								ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF								ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF								ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF								ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF								ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF								ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF								ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF								ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT								ns

Notes:
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. Specification also applies to PSCLK.

Output Clock Jitter

Table 46: **Output Clock Jitter**

			Speed Grade						
			–8		–7		–6		
Description	**Symbol**	**Constraints**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Synthesis Period Jitter									
CLK0	CLKOUT_PER_JITT_0								ps
CLK90	CLKOUT_PER_JITT_90								ps
CLK180	CLKOUT_PER_JITT_180								ps
CLK270	CLKOUT_PER_JITT_270								ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X								ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1								ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2								ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX								ps

Output Clock Phase Alignment

Table 47: **Output Clock Phase Alignment**

			Speed Grade						
			–8		–7		–6		
Description	**Symbol**	**Constraints**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Phase Offset Between CLKIN and CLKFB									
CLKIN/CLKFB	CLKIN_CLKFB_PHASE								ps
Phase Offset Between Any DCM Outputs									
All CLK outputs	CLKOUT_PHASE								ps
Duty Cycle Precision									
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL								ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX								ps

Notes:
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Miscellaneous Timing Parameters

Table 48: **Miscellaneous Timing Parameters**

			Speed Grade			
Description	**Symbol**	**Constraints F_{CLKIN}**	**–8**	**–7**	**–6**	**Units**
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL:					
	LOCK_DLL_60	> 60MHz				us
	LOCK_DLL_50_60	50 - 60 MHz				us
	LOCK_DLL_40_50	40 - 50 MHz				us
	LOCK_DLL_30_40	30 - 40 MHz				us
	LOCK_DLL_24_30	24 - 30 MHz				us
Using CLKFX outputs	LOCK_FX_MIN					ms
	LOCK_FX_MAX					ms
Additional lock time with fine phase shifting	LOCK_DLL_FINE_SHIFT					us
Fine Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE					ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN					ps
	DCM_TAP_MAX					ps

Notes:
1. “”DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

Frequency Synthesis

Table 49: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross-Reference

Table 50: **Parameter Cross-Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
01/31/02	1.0	Initial Xilinx release.

Virtex-II Pro Data Sheet Modules

The Virtex-II Pro Data Sheet contains the following modules:

- **Virtex-II Pro™ Platform FPGAs: Introduction and Overview (Module 1)**
- **Virtex-II Pro™ Platform FPGAs: Functional Description (Module 2)**
- **Virtex-II Pro Platform FPGAs: DC and Switching Characteristics (Module 3)**
- **Virtex-II Pro™ Platform FPGAs: Pinout Information (Module 4)**