Virtex-II Pro™ Platform FPGAs: Pinout Information

Advance Product Specification

This document provides **Virtex-II Pro Device/Package Combinations and Maximum I/Os** and **Virtex-II Pro Pin Definitions**, followed by pinout tables for the following packages:

- **FG256 Fine-Pitch BGA Package**
- **FG456 Fine-Pitch BGA Package**

- **FF672 Flip-Chip Fine-Pitch BGA Package**
- **FF896 Flip-Chip Fine-Pitch BGA Package**
- **FF1152 Flip-Chip Fine-Pitch BGA Package**
- **FF1517 Flip-Chip Fine-Pitch BGA Package**
- **BF957 Flip-Chip BGA Package**

Virtex-II Pro Device/Package Combinations and Maximum I/Os

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

Table 1: **Wire-Bond Packages Information**

Package	FG256	FG456
Pitch (mm)	1.00	1.00
Size (mm)	17 x 17	23 x 23
I/Os	140	248

Table 2: **Flip-Chip Packages Information**

Package	FF672	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.00	1.27
Size (mm)	27 x 27	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	396	556	692	852	584

Table 3 shows the number of available I/Os and the number of Rocket I/O™ multi-gigabit transceiver (MGT) pins for each Virtex-II Pro device/package combination. The number of I/Os per package includes all user I/Os *except* the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD) and the nine (per transceiver) Rocket I/O MGT pins (TXP, TXN, RXP, RXN, AVCCAUXTX, AVCCAUXRX, VTTX, VTRX, and GNDA). The number of transceivers in the device is the number of Rocket I/O MGT pins in Table 3 divided by nine.

Table 3: **Virtex-II Pro Available I/Os and Rocket I/O MGT Pins per Device/Package Combination**

Device⇒ Package⇓	XC2VP2		XC2VP4		XC2VP7		XC2VP20		XC2VP50	
	Available User I/Os	Rocket I/O MGT Pins	Available User I/Os	Rocket I/O MGT Pins	Available User I/Os	Rocket I/O MGT Pins	Available User I/Os	Rocket I/O MGT Pins	Available User I/Os	Rocket I/O MGT Pins
FG256	140	36	140	36						
FG456	156	72	248	72	248	72				
FF672	204	72	348	72	396	72				
FF896					396	72	556	72		
FF1152							564	144	692	144
FF1517									852	144
BF957							564	108	584	108

Table 4 shows the number of 3.3V SelectI/Os in each bank and the total for each device/package combination.

Table 4: **3.3V SelectI/O Banks**

Virtex-II Pro Device	Package	Bank0	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7	Total 3.3V I/Os
2VP2	FG256		17	18	18					53
	FG456		21	18	18					57
	FF672		27	24	24					75
2VP4	FG256		17	17	17					51
	FG456		21	40	42					103
	FF672		27	60	60					147
2VP7	FG456		21	40	42					103
	FF672		39	60	60					159
	FF896		39	60	60					159
2VP20	BF957	57	57							114
	FF896		55	84						139
	FF1152	57	57							114
2VP50	BF957	59	59							118
	FF1152	69	69							138
	FF1517	81	81							162

Virtex-II Pro Pin Definitions

This section describes the pinouts for Virtex-II Pro devices in the following packages:

- FG256 and FG456: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF672, FF896, FF1152, and FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the Virtex-II Pro *Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 5 provides definitions for all pin types.

All Virtex-II Pro pinout tables are available on the distribution CD-ROM, or on the web (at **http://www.xilinx.com**).

Pin Definitions

Table 5 provides a description of each pin type listed in Virtex-II Pro pinout tables.

Table 5: **Virtex-II Pro Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		

IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where:
		    IO indicates a user I/O pin.
		    LXXY indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair.
		    # indicates the bank number (0 through 7)

Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, DIN/D0 – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
DIN / D0, D1, D2, D3, D4, D5, D6, D7	Input/Output	In SelectMAP mode, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. In bit-serial modes, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins[1]		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 5: **Virtex-II Pro Pin Definitions** *(Continued)*

Pin Name	Direction	Description
PROG_B	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
DONE	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
M2, M1, M0	Input	Configuration mode selection.
HSWAP_EN	Input	Enable I/O pullups during configuration.
TCK	Input	Boundary Scan Clock.
TDI	Input	Boundary Scan Data Input.
TDO	Output	Boundary Scan Data Output.
TMS	Input	Boundary Scan Mode Select.
PWRDWN_B	Input	Power down pin.
Other Pins		
DXN, DXP	N/A	Temperature-sensing diode pins (Anode: DXP, Cathode: DXN).
V_{BATT}	Input	Decryptor key memory backup supply. (Do not connect if battery is not used.)
RSVD	N/A	Reserved pin - do not connect.
V_{CCO}	Input	Power-supply pins for the output drivers (per bank).
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits.
V_{CCINT}	Input	Power-supply pins for the internal core logic.
GND	Input	Ground.
AVCCAUXRX#	Input	Analog power supply for receive circuitry of the Rocket I/O multi-gigabit transceiver (2.5V).
AVCCAUXTX#	Input	Analog power supply for transmit circuitry of the Rocket I/O multi-gigabit transceiver (2.5V).
VTRXPAD#	Input	Receive termination supply for the Rocket I/O multi-gigabit transceiver (1.8V - 2.8V).
VTTXPAD#	Input	Transmit termination supply for the Rocket I/O multi-gigabit transceiver (1.8V - 2.8V).
GNDA# [2]	Input	Ground for the analog circuitry of the Rocket I/O multi-gigabit transceiver.
RXPPAD#	Output	Positive differential receive port of the Rocket I/O multi-gigabit transceiver.
RXNPAD#	Output	Negitive differential receive port of the Rocket I/O multi-gigabit transceiver.
TXPPAD#	Input	Positive differential transmit port of the Rocket I/O multi-gigabit transceiver.
TXNPAD#	Input	Negitive differential transmit port of the Rocket I/O multi-gigabit transceiver.

Notes:
1. All dedicated pins (JTAG and configuration) are powered by V_{CCAUX} (independent of the bank V_{CCO} voltage).
2. Two pads on the die are tied to the same package pin (GNDA) in order to lower the resistance on these connections. Thus, duplicate entries exist for GNDA pins.

FG256 Fine-Pitch BGA Package

As shown in Table 6, XC2VP2 and XC2VP4 Virtex-II Pro devices are available in the FG256 fine-pitch BGA package. The pins in each of these devices are identical. Following this table are the **FG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	C2
0	IO_L01P_0/VRN_0	C3
0	IO_L02N_0	B3
0	IO_L02P_0	C4
0	IO_L03N_0	A2
0	IO_L03P_0/VREF_0	A3
0	IO_L06N_0	D5
0	IO_L06P_0	C5
0	IO_L07P_0	D6
0	IO_L09N_0	E6
0	IO_L09P_0/VREF_0	E7
0	IO_L69N_0	D7
0	IO_L69P_0/VREF_0	C7
0	IO_L74N_0/GCLK7P	D8
0	IO_L74P_0/GCLK6S	C8
0	IO_L75N_0/GCLK5P	B8
0	IO_L75P_0/GCLK4S	A8
1	IO_L75N_1/GCLK3P	A9
1	IO_L75P_1/GCLK2S	B9
1	IO_L74N_1/GCLK1P	C9
1	IO_L74P_1/GCLK0S	D9
1	IO_L69N_1/VREF_1	C10
1	IO_L69P_1	D10
1	IO_L09N_1/VREF_1	E10
1	IO_L09P_1	E11
1	IO_L07N_1	D11
1	IO_L06N_1	C12
1	IO_L06P_1	D12
1	IO_L03N_1/VREF_1	A14
1	IO_L03P_1	A15

Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
1	IO_L02N_1	C13
1	IO_L02P_1	B14
1	IO_L01N_1/VRP_1	C14
1	IO_L01P_1/VRN_1	C15
2	IO_L01N_2/VRP_2	E14
2	IO_L01P_2/VRN_2	E15
2	IO_L02N_2	E13
2	IO_L02P_2	F12
2	IO_L03N_2	F13
2	IO_L03P_2	F14
2	IO_L04N_2/VREF_2	F15
2	IO_L04P_2	F16
2	IO_L06N_2	G13
2	IO_L06P_2	G14
2	IO_L85N_2	G15
2	IO_L85P_2	G16
2	IO_L86N_2	G12
2	IO_L86P_2	H13
2	IO_L88N_2/VREF_2	H14
2	IO_L88P_2	H15
2	IO_L90N_2	H16
2	IO_L90P_2	J16
3	IO_L90N_3	J15
3	IO_L90P_3	J14
3	IO_L89N_3	J13
3	IO_L89P_3	K12
3	IO_L87N_3/VREF_3	K16
3	IO_L87P_3	K15
3	IO_L85N_3	K14
3	IO_L85P_3	K13
3	IO_L06N_3	L16
3	IO_L06P_3	L15
3	IO_L05N_3	L14

Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
3	IO_L05P_3	L13
3	IO_L03N_3/VREF_3	L12
3	IO_L03P_3	M13
3	IO_L02N_3	M16
3	IO_L02P_3	N16
3	IO_L01N_3/VRP_3	M15
3	IO_L01P_3/VRN_3	M14
4	IO_L01N_4/DOUT	P15
4	IO_L01P_4/INIT_B	P14
4	IO_L02N_4/D0	R14
4	IO_L02P_4/D1	P13
4	IO_L03N_4/D2	T15
4	IO_L03P_4/D3	T14
4	IO_L06N_4/VRP_4	N12
4	IO_L06P_4/VRN_4	P12
4	IO_L07P_4/VREF_4	N11
4	IO_L09N_4	M11
4	IO_L09P_4/VREF_4	M10
4	IO_L69N_4	N10
4	IO_L69P_4/VREF_4	P10
4	IO_L74N_4/GCLK3S	N9
4	IO_L74P_4/GCLK2P	P9
4	IO_L75N_4/GCLK1S	R9
4	IO_L75P_4/GCLK0P	T9
5	IO_L75N_5/GCLK7S	T8
5	IO_L75P_5/GCLK6P	R8
5	IO_L74N_5/GCLK5S	P8
5	IO_L74P_5/GCLK4P	N8
5	IO_L69N_5/VREF_5	P7
5	IO_L69P_5	N7
5	IO_L09N_5/VREF_5	M7
5	IO_L09P_5	M6
5	IO_L07N_5/VREF_5	N6

Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
5	IO_L06N_5/VRP_5	P5
5	IO_L06P_5/VRN_5	N5
5	IO_L03N_5/D4	T3
5	IO_L03P_5/D5	T2
5	IO_L02N_5/D6	P4
5	IO_L02P_5/D7	R3
5	IO_L01N_5/RDWR_B	P3
5	IO_L01P_5/CS_B	P2
6	IO_L01P_6/VRN_6	M3
6	IO_L01N_6/VRP_6	M2
6	IO_L02P_6	N1
6	IO_L02N_6	M1
6	IO_L03P_6	M4
6	IO_L03N_6/VREF_6	L5
6	IO_L05P_6	L4
6	IO_L05N_6	L3
6	IO_L06P_6	L2
6	IO_L06N_6	L1
6	IO_L85P_6	K4
6	IO_L85N_6	K3
6	IO_L87P_6	K2
6	IO_L87N_6/VREF_6	K1
6	IO_L89P_6	K5
6	IO_L89N_6	J4
6	IO_L90P_6	J3
6	IO_L90N_6	J2
7	IO_L90P_7	J1
7	IO_L90N_7	H1
7	IO_L88P_7	H2
7	IO_L88N_7/VREF_7	H3
7	IO_L86P_7	H4
7	IO_L86N_7	G5
7	IO_L85P_7	G1

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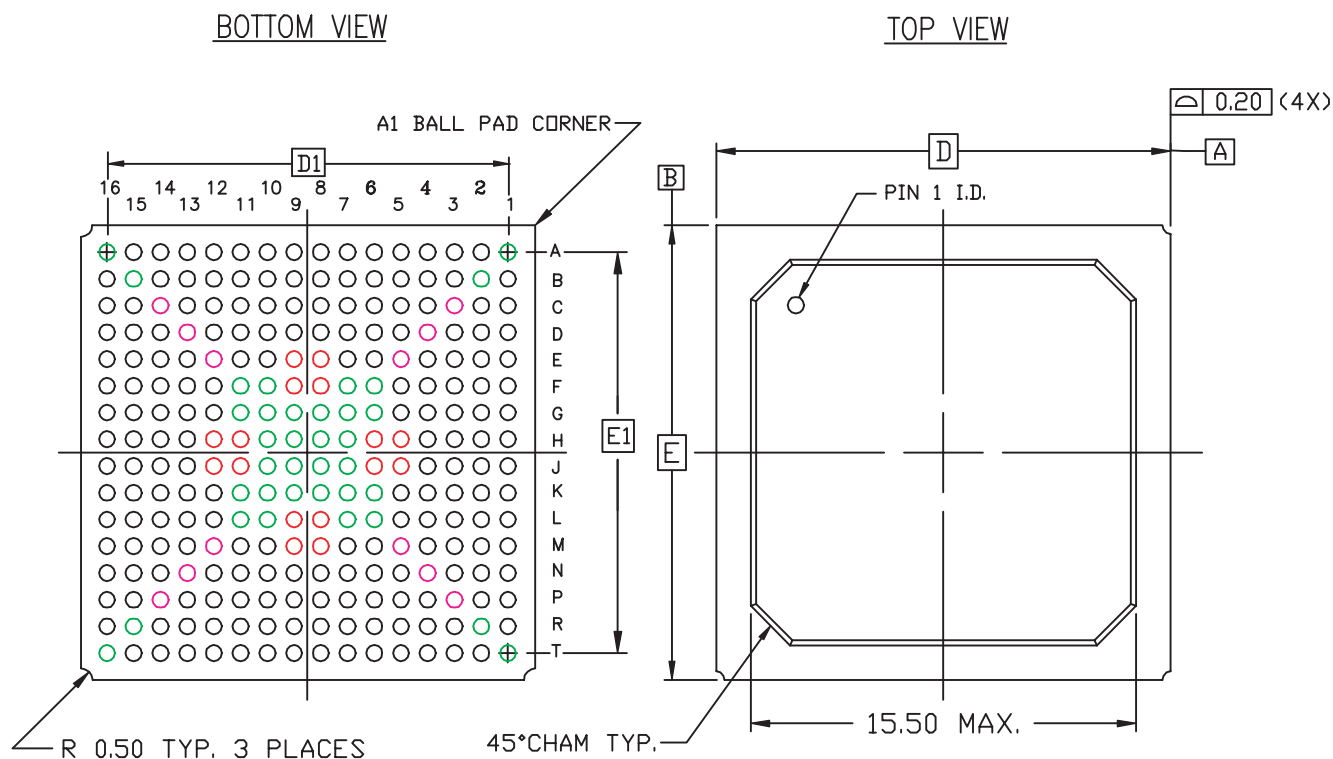DS083-4 (v1.0) January 31, 2002
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Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
7	IO_L85N_7	G2
7	IO_L06P_7	G3
7	IO_L06N_7	G4
7	IO_L04P_7	F1
7	IO_L04N_7/VREF_7	F2
7	IO_L03P_7	F3
7	IO_L03N_7	F4
7	IO_L02P_7	F5
7	IO_L02N_7	E4
7	IO_L01P_7/VRN_7	E2
7	IO_L01N_7/VRP_7	E3
0	VCCO_0	F8
0	VCCO_0	F7
0	VCCO_0	E8
1	VCCO_1	F9
1	VCCO_1	F10
1	VCCO_1	E9
2	VCCO_2	H12
2	VCCO_2	H11
2	VCCO_2	G11
3	VCCO_3	K11
3	VCCO_3	J12
3	VCCO_3	J11
4	VCCO_4	M9
4	VCCO_4	L9
4	VCCO_4	L10
5	VCCO_5	M8
5	VCCO_5	L8
5	VCCO_5	L7
6	VCCO_6	K6
6	VCCO_6	J6
6	VCCO_6	J5
7	VCCO_7	H6
7	VCCO_7	H5

Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
7	VCCO_7	G6
N/A	CCLK	N15
N/A	PROG_B	D1
N/A	DONE	P16
N/A	M0	N3
N/A	M1	N2
N/A	M2	P1
N/A	TCK	D16
N/A	TDI	E1
N/A	TDO	E16
N/A	TMS	C16
N/A	PWRDWN_B	N14
N/A	HSWAP_EN	C1
N/A	RSVD	D14
N/A	VBATT	D15
N/A	DXP	D2
N/A	DXN	D3
N/A	AVCCAUXTX6	B5
N/A	VTTXPAD6	B4
N/A	TXNPAD6	A4
N/A	TXPPAD6	A5
N/A	GNDA6	C6
N/A	GNDA6	C6
N/A	RXPPAD6	A6
N/A	RXNPAD6	A7
N/A	VTRXPAD6	B6
N/A	AVCCAUXRX6	B7
N/A	AVCCAUXTX7	B11
N/A	VTTXPAD7	B10
N/A	TXNPAD7	A10
N/A	TXPPAD7	A11
N/A	GNDA7	C11
N/A	GNDA7	C11
N/A	RXPPAD7	A12

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Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
N/A	RXNPAD7	A13
N/A	VTRXPAD7	B12
N/A	AVCCAUXRX7	B13
N/A	AVCCAUXRX18	R13
N/A	VTRXPAD18	R12
N/A	RXNPAD18	T13
N/A	RXPPAD18	T12
N/A	GNDA18	P11
N/A	GNDA18	P11
N/A	TXPPAD18	T11
N/A	TXNPAD18	T10
N/A	VTTXPAD18	R10
N/A	AVCCAUXTX18	R11
N/A	AVCCAUXRX19	R7
N/A	VTRXPAD19	R6
N/A	RXNPAD19	T7
N/A	RXPPAD19	T6
N/A	GNDA19	P6
N/A	GNDA19	P6
N/A	TXPPAD19	T5
N/A	TXNPAD19	T4
N/A	VTTXPAD19	R4
N/A	AVCCAUXTX19	R5
N/A	VCCINT	N4
N/A	VCCINT	N13
N/A	VCCINT	M5
N/A	VCCINT	M12
N/A	VCCINT	E5
N/A	VCCINT	E12
N/A	VCCINT	D4
N/A	VCCINT	D13
N/A	VCCAUX	R16
N/A	VCCAUX	R1
N/A	VCCAUX	B16

Table 6: **FG256 — XC2VP2 and XC2VP4**

Bank	Pin Description	Pin Number
N/A	VCCAUX	B1
N/A	GND	T16
N/A	GND	T1
N/A	GND	R2
N/A	GND	R15
N/A	GND	L6
N/A	GND	L11
N/A	GND	K9
N/A	GND	K8
N/A	GND	K7
N/A	GND	K10
N/A	GND	J9
N/A	GND	J8
N/A	GND	J7
N/A	GND	J10
N/A	GND	H9
N/A	GND	H8
N/A	GND	H7
N/A	GND	H10
N/A	GND	G9
N/A	GND	G8
N/A	GND	G7
N/A	GND	G10
N/A	GND	F6
N/A	GND	F11
N/A	GND	B2
N/A	GND	B15
N/A	GND	A16
N/A	GND	A1

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FG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)

BOTTOM VIEW

TOP VIEW

A1 BALL PAD CORNER

D1

16 14 12 10   8   6   4   2
  15 13 11   9   7   5   3   1

A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T

E1

PIN 1 I.D.

0.20 (4X)

D

B

E

A

15.50 MAX.

R 0.50 TYP. 3 PLACES

45°CHAM TYP.

30°

SEATING PLANE

// ccc C

A

aaa

C

A1

e

Øb

Ødddd M C A B
Øeee M C

SOLDER BALLS
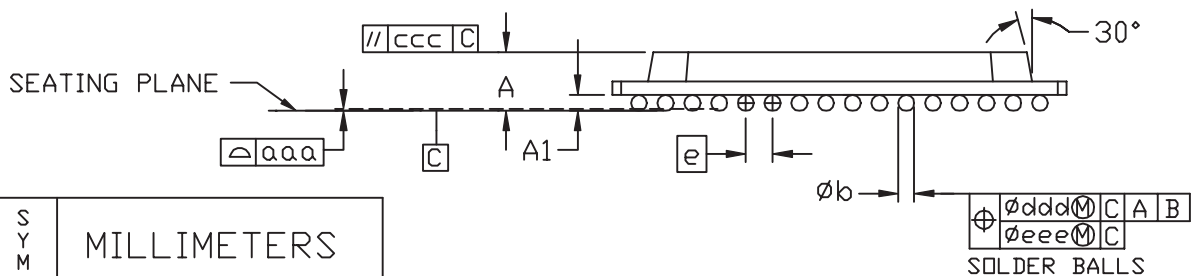
SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.73	2.00
A₁	0.40	0.50	0.60
D/E	17.00 BSC		
D₁/E₁	15.00 REF		
e	1.00 BSC		
Øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	16		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994

2. SYMBOL 'M' IS THE BALL MATRIX SIZE.

3. CONFORMS TO JEDEC MO-151 AAF-1.

Figure 1: **FG256 Fine-Pitch BGA Package Specifications**

FG456 Fine-Pitch BGA Package

As shown in Table 7, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FG456 fine-pitch BGA package. The pins in these devices are same, except for the differences shown in the "No Connects" column. Following this table are the **FG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects XC2V P2	XC2V P4	XC2V P7
0	IO_L01N_0/VRP_0	D5			
0	IO_L01P_0/VRN_0	D6			
0	IO_L02N_0	E6			
0	IO_L02P_0	E7			
0	IO_L03N_0	D7			
0	IO_L03P_0/VREF_0	C7			
0	IO_L05_0/No_Pair	E8			
0	IO_L06N_0	D8			
0	IO_L06P_0	C8			
0	IO_L07N_0	F9			
0	IO_L07P_0	E9			
0	IO_L09N_0	D9			
0	IO_L09P_0/VREF_0	D10			
0	IO_L67N_0	F10			
0	IO_L67P_0	E10			
0	IO_L69N_0	C10			
0	IO_L69P_0/VREF_0	B11			
0	IO_L74N_0/GCLK7P	F11			
0	IO_L74P_0/GCLK6S	E11			
0	IO_L75N_0/GCLK5P	D11			
0	IO_L75P_0/GCLK4S	C11			
1	IO_L75N_1/GCLK3P	C12			
1	IO_L75P_1/GCLK2S	D12			
1	IO_L74N_1/GCLK1P	E12			
1	IO_L74P_1/GCLK0S	F12			
1	IO_L69N_1/VREF_1	B12			
1	IO_L69P_1	C13			
1	IO_L67N_1	E13			
1	IO_L67P_1	F13			
1	IO_L09N_1/VREF_1	D13			

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
1	IO_L09P_1	D14			
1	IO_L07N_1	E14			
1	IO_L07P_1	F14			
1	IO_L06N_1	C15			
1	IO_L06P_1	D15			
1	IO_L05_1/No_Pair	E15			
1	IO_L03N_1/VREF_1	C16			
1	IO_L03P_1	D16			
1	IO_L02N_1	E16			
1	IO_L02P_1	E17			
1	IO_L01N_1/VRP_1	D17			
1	IO_L01P_1/VRN_1	D18			
2	IO_L01N_2/VRP_2	C21			
2	IO_L01P_2/VRN_2	C22			
2	IO_L02N_2	D21			
2	IO_L02P_2	D22			
2	IO_L03N_2	E19			
2	IO_L03P_2	E20			
2	IO_L04N_2/VREF_2	E21			
2	IO_L04P_2	E22			
2	IO_L06N_2	F19			
2	IO_L06P_2	F20			
2	IO_L43N_2	F21	NC		
2	IO_L43P_2	F22	NC		
2	IO_L46N_2/VREF_2	F18	NC		
2	IO_L46P_2	G18	NC		
2	IO_L48N_2	G19	NC		
2	IO_L48P_2	G20	NC		
2	IO_L49N_2	G21	NC		
2	IO_L49P_2	G22	NC		
2	IO_L50N_2	H19	NC		
2	IO_L50P_2	H20	NC		
2	IO_L52N_2/VREF_2	H21	NC		
2	IO_L52P_2	H22	NC		

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
2	IO_L54N_2	H18	NC		
2	IO_L54P_2	J17	NC		
2	IO_L55N_2	J19	NC		
2	IO_L55P_2	J20	NC		
2	IO_L56N_2	J21	NC		
2	IO_L56P_2	J22	NC		
2	IO_L58N_2/VREF_2	J18	NC		
2	IO_L58P_2	K18	NC		
2	IO_L60N_2	K19	NC		
2	IO_L60P_2	K20	NC		
2	IO_L85N_2	K21			
2	IO_L85P_2	K22			
2	IO_L86N_2	K17			
2	IO_L86P_2	L17			
2	IO_L88N_2/VREF_2	L18			
2	IO_L88P_2	L19			
2	IO_L90N_2	L20			
2	IO_L90P_2	L21			
3	IO_L90N_3	M21			
3	IO_L90P_3	M20			
3	IO_L89N_3	M19			
3	IO_L89P_3	M18			
3	IO_L87N_3/VREF_3	M17			
3	IO_L87P_3	N17			
3	IO_L85N_3	N22			
3	IO_L85P_3	N21			
3	IO_L60N_3	N20	NC		
3	IO_L60P_3	N19	NC		
3	IO_L59N_3	N18	NC		
3	IO_L59P_3	P18	NC		
3	IO_L57N_3/VREF_3	P22	NC		
3	IO_L57P_3	P21	NC		
3	IO_L55N_3	P20	NC		
3	IO_L55P_3	P19	NC		

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
3	IO_L54N_3	P17	NC		
3	IO_L54P_3	R18	NC		
3	IO_L53N_3	R22	NC		
3	IO_L53P_3	R21	NC		
3	IO_L51N_3/VREF_3	R20	NC		
3	IO_L51P_3	R19	NC		
3	IO_L49N_3	T22	NC		
3	IO_L49P_3	T21	NC		
3	IO_L48N_3	T20	NC		
3	IO_L48P_3	T19	NC		
3	IO_L47N_3	T18	NC		
3	IO_L47P_3	U18	NC		
3	IO_L45N_3/VREF_3	U22	NC		
3	IO_L45P_3	U21	NC		
3	IO_L43N_3	U20	NC		
3	IO_L43P_3	U19	NC		
3	IO_L06N_3	V22			
3	IO_L06P_3	V21			
3	IO_L05N_3	V20			
3	IO_L05P_3	V19			
3	IO_L03N_3/VREF_3	W22			
3	IO_L03P_3	W21			
3	IO_L02N_3	Y22			
3	IO_L02P_3	Y21			
3	IO_L01N_3/VRP_3	AA22			
3	IO_L01P_3/VRN_3	AB21			
4	IO_L01N_4/DOUT	W18			
4	IO_L01P_4/INIT_B	W17			
4	IO_L02N_4/D0	V17			
4	IO_L02P_4/D1	V16			
4	IO_L03N_4/D2	W16			
4	IO_L03P_4/D3	Y16			
4	IO_L05_4/No_Pair	V15			
4	IO_L06N_4/VRP_4	W15			

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
4	IO_L06P_4/VRN_4	Y15			
4	IO_L07N_4	U14			
4	IO_L07P_4/VREF_4	V14			
4	IO_L09N_4	W14			
4	IO_L09P_4/VREF_4	W13			
4	IO_L67N_4	U13			
4	IO_L67P_4	V13			
4	IO_L69N_4	Y13			
4	IO_L69P_4/VREF_4	AA12			
4	IO_L74N_4/GCLK3S	U12			
4	IO_L74P_4/GCLK2P	V12			
4	IO_L75N_4/GCLK1S	W12			
4	IO_L75P_4/GCLK0P	Y12			
5	IO_L75N_5/GCLK7S	Y11			
5	IO_L75P_5/GCLK6P	W11			
5	IO_L74N_5/GCLK5S	V11			
5	IO_L74P_5/GCLK4P	U11			
5	IO_L69N_5/VREF_5	AA11			
5	IO_L69P_5	Y10			
5	IO_L67N_5	V10			
5	IO_L67P_5	U10			
5	IO_L09N_5/VREF_5	W10			
5	IO_L09P_5	W9			
5	IO_L07N_5/VREF_5	V9			
5	IO_L07P_5	U9			
5	IO_L06N_5/VRP_5	Y8			
5	IO_L06P_5/VRN_5	W8			
5	IO_L05_5/No_Pair	V8			
5	IO_L03N_5/D4	Y7			
5	IO_L03P_5/D5	W7			
5	IO_L02N_5/D6	V7			
5	IO_L02P_5/D7	V6			
5	IO_L01N_5/RDWR_B	W6			
5	IO_L01P_5/CS_B	W5			

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
6	IO_L01P_6/VRN_6	AB2			
6	IO_L01N_6/VRP_6	AA1			
6	IO_L02P_6	Y2			
6	IO_L02N_6	Y1			
6	IO_L03P_6	W2			
6	IO_L03N_6/VREF_6	W1			
6	IO_L05P_6	V4			
6	IO_L05N_6	V3			
6	IO_L06P_6	V2			
6	IO_L06N_6	V1			
6	IO_L43P_6	U4	NC		
6	IO_L43N_6	U3	NC		
6	IO_L45P_6	U2	NC		
6	IO_L45N_6/VREF_6	U1	NC		
6	IO_L47P_6	U5	NC		
6	IO_L47N_6	T5	NC		
6	IO_L48P_6	T4	NC		
6	IO_L48N_6	T3	NC		
6	IO_L49P_6	T2	NC		
6	IO_L49N_6	T1	NC		
6	IO_L51P_6	R4	NC		
6	IO_L51N_6/VREF_6	R3	NC		
6	IO_L53P_6	R2	NC		
6	IO_L53N_6	R1	NC		
6	IO_L54P_6	R5	NC		
6	IO_L54N_6	P6	NC		
6	IO_L55P_6	P4	NC		
6	IO_L55N_6	P3	NC		
6	IO_L57P_6	P2	NC		
6	IO_L57N_6/VREF_6	P1	NC		
6	IO_L59P_6	P5	NC		
6	IO_L59N_6	N5	NC		
6	IO_L60P_6	N4	NC		
6	IO_L60N_6	N3	NC		

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
6	IO_L85P_6	N2			
6	IO_L85N_6	N1			
6	IO_L87P_6	N6			
6	IO_L87N_6/VREF_6	M6			
6	IO_L89P_6	M5			
6	IO_L89N_6	M4			
6	IO_L90P_6	M3			
6	IO_L90N_6	M2			
7	IO_L90P_7	L2			
7	IO_L90N_7	L3			
7	IO_L88P_7	L4			
7	IO_L88N_7/VREF_7	L5			
7	IO_L86P_7	L6			
7	IO_L86N_7	K6			
7	IO_L85P_7	K1			
7	IO_L85N_7	K2			
7	IO_L60P_7	K3	NC		
7	IO_L60N_7	K4	NC		
7	IO_L58P_7	K5	NC		
7	IO_L58N_7/VREF_7	J5	NC		
7	IO_L56P_7	J1	NC		
7	IO_L56N_7	J2	NC		
7	IO_L55P_7	J3	NC		
7	IO_L55N_7	J4	NC		
7	IO_L54P_7	J6	NC		
7	IO_L54N_7	H5	NC		
7	IO_L52P_7	H1	NC		
7	IO_L52N_7/VREF_7	H2	NC		
7	IO_L50P_7	H3	NC		
7	IO_L50N_7	H4	NC		
7	IO_L49P_7	G1	NC		
7	IO_L49N_7	G2	NC		
7	IO_L48P_7	G3	NC		
7	IO_L48N_7	G4	NC		

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects XC2V P2	No Connects XC2V P4	No Connects XC2V P7
7	IO_L46P_7	G5	NC		
7	IO_L46N_7/VREF_7	F5	NC		
7	IO_L43P_7	F1	NC		
7	IO_L43N_7	F2	NC		
7	IO_L06P_7	F3			
7	IO_L06N_7	F4			
7	IO_L04P_7	E1			
7	IO_L04N_7/VREF_7	E2			
7	IO_L03P_7	E3			
7	IO_L03N_7	E4			
7	IO_L02P_7	D1			
7	IO_L02N_7	D2			
7	IO_L01P_7/VRN_7	C1			
7	IO_L01N_7/VRP_7	C2			
0	VCCO_0	G9			
0	VCCO_0	G11			
0	VCCO_0	G10			
0	VCCO_0	F8			
0	VCCO_0	F7			
1	VCCO_1	G14			
1	VCCO_1	G13			
1	VCCO_1	G12			
1	VCCO_1	F16			
1	VCCO_1	F15			
2	VCCO_2	L16			
2	VCCO_2	K16			
2	VCCO_2	J16			
2	VCCO_2	H17			
2	VCCO_2	G17			
3	VCCO_3	T17			
3	VCCO_3	R17			
3	VCCO_3	P16			
3	VCCO_3	N16			
3	VCCO_3	M16			

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
4	VCCO_4	U16			
4	VCCO_4	U15			
4	VCCO_4	T14			
4	VCCO_4	T13			
4	VCCO_4	T12			
5	VCCO_5	U8			
5	VCCO_5	U7			
5	VCCO_5	T9			
5	VCCO_5	T11			
5	VCCO_5	T10			
6	VCCO_6	T6			
6	VCCO_6	R6			
6	VCCO_6	P7			
6	VCCO_6	N7			
6	VCCO_6	M7			
7	VCCO_7	L7			
7	VCCO_7	K7			
7	VCCO_7	J7			
7	VCCO_7	H6			
7	VCCO_7	G6			
N/A	CCLK	W20			
N/A	PROG_B	B1			
N/A	DONE	Y18			
N/A	M0	Y4			
N/A	M1	W3			
N/A	M2	Y5			
N/A	TCK	B22			
N/A	TDI	D3			
N/A	TDO	D20			
N/A	TMS	A21			
N/A	PWRDWN_B	Y19			
N/A	HSWAP_EN	A2			
N/A	RSVD	C18			
N/A	VBATT	C19			

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	DXP	C4			
N/A	DXN	C5			
N/A	AVCCAUXTX4	B4	NC	NC	
N/A	VTTXPAD4	B3	NC	NC	
N/A	TXNPAD4	A3	NC	NC	
N/A	TXPPAD4	A4	NC	NC	
N/A	GNDA4	C6	NC	NC	
N/A	GNDA4	C6	NC	NC	
N/A	RXPPAD4	A5	NC	NC	
N/A	RXNPAD4	A6	NC	NC	
N/A	VTRXPAD4	B5	NC	NC	
N/A	AVCCAUXRX4	B6	NC	NC	
N/A	AVCCAUXTX6	B8			
N/A	VTTXPAD6	B7			
N/A	TXNPAD6	A7			
N/A	TXPPAD6	A8			
N/A	GNDA6	C9			
N/A	GNDA6	C9			
N/A	RXPPAD6	A9			
N/A	RXNPAD6	A10			
N/A	VTRXPAD6	B9			
N/A	AVCCAUXRX6	B10			
N/A	AVCCAUXTX7	B14			
N/A	VTTXPAD7	B13			
N/A	TXNPAD7	A13			
N/A	TXPPAD7	A14			
N/A	GNDA7	C14			
N/A	GNDA7	C14			
N/A	RXPPAD7	A15			
N/A	RXNPAD7	A16			
N/A	VTRXPAD7	B15			
N/A	AVCCAUXRX7	B16			
N/A	AVCCAUXTX9	B18	NC	NC	
N/A	VTTXPAD9	B17	NC	NC	
N/A	TXNPAD9	A17	NC	NC	

Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	**XC2V P4**	**XC2V P7**
N/A	TXPPAD9	A18	NC	NC	
N/A	GNDA9	C17	NC	NC	
N/A	GNDA9	C17	NC	NC	
N/A	RXPPAD9	A19	NC	NC	
N/A	RXNPAD9	A20	NC	NC	
N/A	VTRXPAD9	B19	NC	NC	
N/A	AVCCAUXRX9	B20	NC	NC	
N/A	AVCCAUXRX16	AA20	NC	NC	
N/A	VTRXPAD16	AA19	NC	NC	
N/A	RXNPAD16	AB20	NC	NC	
N/A	RXPPAD16	AB19	NC	NC	
N/A	GNDA16	Y17	NC	NC	
N/A	GNDA16	Y17	NC	NC	
N/A	TXPPAD16	AB18	NC	NC	
N/A	TXNPAD16	AB17	NC	NC	
N/A	VTTXPAD16	AA17	NC	NC	
N/A	AVCCAUXTX16	AA18	NC	NC	
N/A	AVCCAUXRX18	AA16			
N/A	VTRXPAD18	AA15			
N/A	RXNPAD18	AB16			
N/A	RXPPAD18	AB15			
N/A	GNDA18	Y14			
N/A	GNDA18	Y14			
N/A	TXPPAD18	AB14			
N/A	TXNPAD18	AB13			
N/A	VTTXPAD18	AA13			
N/A	AVCCAUXTX18	AA14			
N/A	AVCCAUXRX19	AA10			
N/A	VTRXPAD19	AA9			
N/A	RXNPAD19	AB10			
N/A	RXPPAD19	AB9			
N/A	GNDA19	Y9			
N/A	GNDA19	Y9			
N/A	TXPPAD19	AB8			
N/A	TXNPAD19	AB7			

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

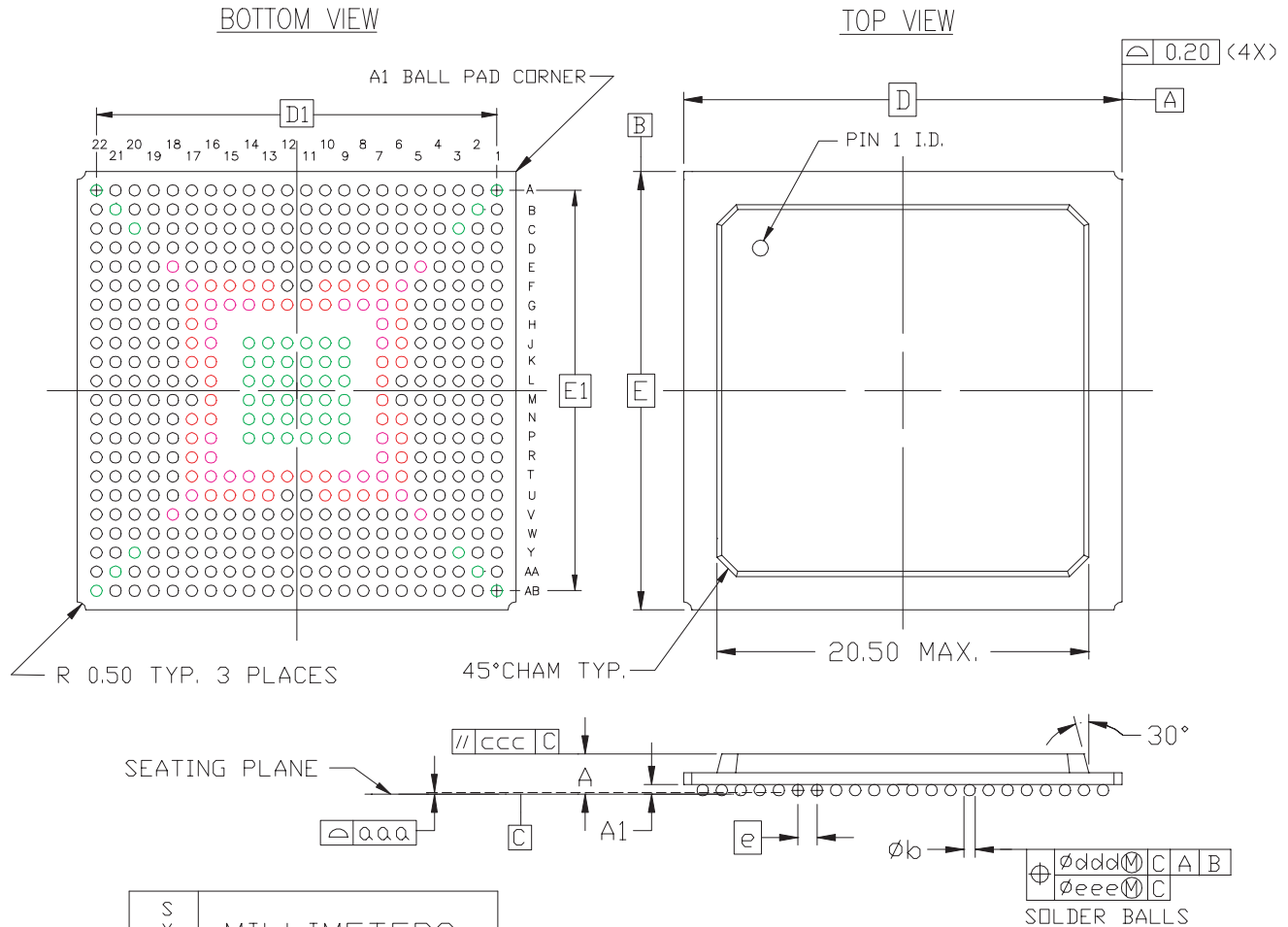| Bank	Pin Description	Pin Number	No Connects		
			XC2VP2	XC2VP4	XC2VP7
N/A	VTTXPAD19	AA7			
N/A	AVCCAUXTX19	AA8			
N/A	AVCCAUXRX21	AA6	NC	NC	
N/A	VTRXPAD21	AA5	NC	NC	
N/A	RXNPAD21	AB6	NC	NC	
N/A	RXPPAD21	AB5	NC	NC	
N/A	GNDA21	Y6	NC	NC	
N/A	GNDA21	Y6	NC	NC	
N/A	TXPPAD21	AB4	NC	NC	
N/A	TXNPAD21	AB3	NC	NC	
N/A	VTTXPAD21	AA3	NC	NC	
N/A	AVCCAUXTX21	AA4	NC	NC	
N/A	VCCINT	U6			
N/A	VCCINT	U17			
N/A	VCCINT	T8			
N/A	VCCINT	T7			
N/A	VCCINT	T16			
N/A	VCCINT	T15			
N/A	VCCINT	R7			
N/A	VCCINT	R16			
N/A	VCCINT	H7			
N/A	VCCINT	H16			
N/A	VCCINT	G8			
N/A	VCCINT	G7			
N/A	VCCINT	G16			
N/A	VCCINT	G15			
N/A	VCCINT	F6			
N/A	VCCINT	F17			
N/A	VCCAUX	M22			
N/A	VCCAUX	L1			
N/A	VCCAUX	B21			
N/A	VCCAUX	B2			
N/A	VCCAUX	AB11			
N/A	VCCAUX	AA21			

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	VCCAUX	AA2			
N/A	VCCAUX	A12			
N/A	GND	Y3			
N/A	GND	Y20			
N/A	GND	W4			
N/A	GND	W19			
N/A	GND	V5			
N/A	GND	V18			
N/A	GND	P9			
N/A	GND	P14			
N/A	GND	P13			
N/A	GND	P12			
N/A	GND	P11			
N/A	GND	P10			
N/A	GND	N9			
N/A	GND	N14			
N/A	GND	N13			
N/A	GND	N12			
N/A	GND	N11			
N/A	GND	N10			
N/A	GND	M9			
N/A	GND	M14			
N/A	GND	M13			
N/A	GND	M12			
N/A	GND	M11			
N/A	GND	M10			
N/A	GND	M1			
N/A	GND	L9			
N/A	GND	L22			
N/A	GND	L14			
N/A	GND	L13			
N/A	GND	L12			
N/A	GND	L11			
N/A	GND	L10			
N/A	GND	K9			

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Table 7: **FG456 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	GND	K14			
N/A	GND	K13			
N/A	GND	K12			
N/A	GND	K11			
N/A	GND	K10			
N/A	GND	J9			
N/A	GND	J14			
N/A	GND	J13			
N/A	GND	J12			
N/A	GND	J11			
N/A	GND	J10			
N/A	GND	E5			
N/A	GND	E18			
N/A	GND	D4			
N/A	GND	D19			
N/A	GND	C3			
N/A	GND	C20			
N/A	GND	AB22			
N/A	GND	AB12			
N/A	GND	AB1			
N/A	GND	A22			
N/A	GND	A11			
N/A	GND	A1			

FG456 Fine-Pitch BGA Package Specifications (1.00mm pitch)

BOTTOM VIEW

TOP VIEW

A1 BALL PAD CORNER

PIN 1 I.D.

R 0.50 TYP. 3 PLACES

45°CHAM TYP.

20.50 MAX.

30°

SEATING PLANE

SOLDER BALLS

SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	2.20	2.60
A_1	0.40	0.50	0.60
D/E	23.00 BSC		
D_1/E_1	21.00 REF		
e	1.00 BSC		
Øb	0.50	0.60	0.70
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.10
M	22		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994

2. SYMBOL 'M' IS THE BALL MATRIX SIZE.

3. CONFORMS TO JEDEC MO-151 AAJ-1 (DEPOPULATED)

456-BALL FINE PITCH BGA (FG456)

Figure 2: **FG456 Fine-Pitch BGA Package Specifications**

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FF672 Flip-Chip Fine-Pitch BGA Package

As shown in Table 8, XC2VP2, XC2VP4, and XC2VP7 Virtex-II Pro devices are available in the FF672 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the **FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
0	IO_L01N_0/VRP_0	B24			
0	IO_L01P_0/VRN_0	A24			
0	IO_L02N_0	D21			
0	IO_L02P_0	C21			
0	IO_L03N_0	E20			
0	IO_L03P_0/VREF_0	D20			
0	IO_L05_0/No_Pair	F19			
0	IO_L06N_0	E19			
0	IO_L06P_0	E18			
0	IO_L07N_0	D19			
0	IO_L07P_0	C19			
0	IO_L08N_0	B19			
0	IO_L08P_0	A19			
0	IO_L09N_0	G18			
0	IO_L09P_0/VREF_0	F18			
0	IO_L37N_0	D18	NC	NC	
0	IO_L37P_0	C18	NC	NC	
0	IO_L38N_0	G17	NC	NC	
0	IO_L38P_0	H16	NC	NC	
0	IO_L39N_0	F17	NC	NC	
0	IO_L39P_0	F16	NC	NC	
0	IO_L43N_0	E17	NC	NC	
0	IO_L43P_0	D17	NC	NC	
0	IO_L44N_0	G16	NC	NC	
0	IO_L44P_0	G15	NC	NC	
0	IO_L45N_0	E16	NC	NC	
0	IO_L45P_0/VREF_0	D16	NC	NC	
0	IO_L67N_0	F15			
0	IO_L67P_0	E15			
0	IO_L68N_0	D15			
0	IO_L68P_0	C15			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
0	IO_L69N_0	H15			
0	IO_L69P_0/VREF_0	H14			
0	IO_L73N_0	G14			
0	IO_L73P_0	F14			
0	IO_L74N_0/GCLK7P	E14			
0	IO_L74P_0/GCLK6S	D14			
0	IO_L75N_0/GCLK5P	C14			
0	IO_L75P_0/GCLK4S	B14			
1	IO_L75N_1/GCLK3P	B13			
1	IO_L75P_1/GCLK2S	C13			
1	IO_L74N_1/GCLK1P	D13			
1	IO_L74P_1/GCLK0S	E13			
1	IO_L73N_1	F13			
1	IO_L73P_1	G13			
1	IO_L69N_1/VREF_1	H13			
1	IO_L69P_1	H12			
1	IO_L68N_1	C12			
1	IO_L68P_1	D12			
1	IO_L67N_1	E12			
1	IO_L67P_1	F12			
1	IO_L45N_1/VREF_1	D11	NC	NC	
1	IO_L45P_1	E11	NC	NC	
1	IO_L44N_1	G12	NC	NC	
1	IO_L44P_1	G11	NC	NC	
1	IO_L43N_1	D10	NC	NC	
1	IO_L43P_1	E10	NC	NC	
1	IO_L39N_1	F11	NC	NC	
1	IO_L39P_1	F10	NC	NC	
1	IO_L38N_1	H11	NC	NC	
1	IO_L38P_1	G10	NC	NC	
1	IO_L37N_1	C9	NC	NC	
1	IO_L37P_1	D9	NC	NC	
1	IO_L09N_1/VREF_1	F9			
1	IO_L09P_1	G9			

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
1	IO_L08N_1	A8			
1	IO_L08P_1	B8			
1	IO_L07N_1	C8			
1	IO_L07P_1	D8			
1	IO_L06N_1	E9			
1	IO_L06P_1	E8			
1	IO_L05_1/No_Pair	F8			
1	IO_L03N_1/VREF_1	D7			
1	IO_L03P_1	E7			
1	IO_L02N_1	C6			
1	IO_L02P_1	D6			
1	IO_L01N_1/VRP_1	A3			
1	IO_L01P_1/VRN_1	B3			
2	IO_L01N_2/VRP_2	C4			
2	IO_L01P_2/VRN_2	D3			
2	IO_L02N_2	A2			
2	IO_L02P_2	B1			
2	IO_L03N_2	C2			
2	IO_L03P_2	C1			
2	IO_L04N_2/VREF_2	D2			
2	IO_L04P_2	D1			
2	IO_L05N_2	E4			
2	IO_L05P_2	E3			
2	IO_L06N_2	E2			
2	IO_L06P_2	E1			
2	IO_L40N_2/VREF_2	F5	NC	NC	NC
2	IO_L40P_2	F4	NC	NC	NC
2	IO_L42N_2	F3	NC	NC	NC
2	IO_L42P_2	F2	NC	NC	NC
2	IO_L43N_2	G6	NC		
2	IO_L43P_2	G5	NC		
2	IO_L44N_2	G4	NC		
2	IO_L44P_2	G3	NC		
2	IO_L45N_2	F1	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects XC2V P2	No Connects XC2V P4	No Connects XC2V P7
2	IO_L45P_2	G1	NC		
2	IO_L46N_2/VREF_2	H6	NC		
2	IO_L46P_2	H5	NC		
2	IO_L47N_2	H4	NC		
2	IO_L47P_2	H3	NC		
2	IO_L48N_2	H2	NC		
2	IO_L48P_2	H1	NC		
2	IO_L49N_2	J7	NC		
2	IO_L49P_2	J6	NC		
2	IO_L50N_2	J5	NC		
2	IO_L50P_2	J4	NC		
2	IO_L51N_2	J3	NC		
2	IO_L51P_2	J2	NC		
2	IO_L52N_2/VREF_2	K6	NC		
2	IO_L52P_2	K5	NC		
2	IO_L53N_2	K4	NC		
2	IO_L53P_2	K3	NC		
2	IO_L54N_2	J1	NC		
2	IO_L54P_2	K1	NC		
2	IO_L55N_2	K7	NC		
2	IO_L55P_2	L8	NC		
2	IO_L56N_2	L7	NC		
2	IO_L56P_2	M7	NC		
2	IO_L57N_2	L6	NC		
2	IO_L57P_2	L5	NC		
2	IO_L58N_2/VREF_2	L4	NC		
2	IO_L58P_2	L3	NC		
2	IO_L59N_2	L2	NC		
2	IO_L59P_2	L1	NC		
2	IO_L60N_2	M8	NC		
2	IO_L60P_2	N8	NC		
2	IO_L85N_2	M6			
2	IO_L85P_2	M5			
2	IO_L86N_2	M4			
2	IO_L86P_2	M3			

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
2	IO_L87N_2	M2			
2	IO_L87P_2	M1			
2	IO_L88N_2/VREF_2	N7			
2	IO_L88P_2	N6			
2	IO_L89N_2	N5			
2	IO_L89P_2	N4			
2	IO_L90N_2	N3			
2	IO_L90P_2	N2			
3	IO_L90N_3	P2			
3	IO_L90P_3	P3			
3	IO_L89N_3	P4			
3	IO_L89P_3	P5			
3	IO_L88N_3	P6			
3	IO_L88P_3	P7			
3	IO_L87N_3/VREF_3	R1			
3	IO_L87P_3	R2			
3	IO_L86N_3	R3			
3	IO_L86P_3	R4			
3	IO_L85N_3	R5			
3	IO_L85P_3	R6			
3	IO_L60N_3	P8	NC		
3	IO_L60P_3	R8	NC		
3	IO_L59N_3	T1	NC		
3	IO_L59P_3	T2	NC		
3	IO_L58N_3	T3	NC		
3	IO_L58P_3	T4	NC		
3	IO_L57N_3/VREF_3	T5	NC		
3	IO_L57P_3	T6	NC		
3	IO_L56N_3	R7	NC		
3	IO_L56P_3	T7	NC		
3	IO_L55N_3	T8	NC		
3	IO_L55P_3	U7	NC		
3	IO_L54N_3	U1	NC		
3	IO_L54P_3	V1	NC		

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
3	IO_L53N_3	U3	NC		
3	IO_L53P_3	U4	NC		
3	IO_L52N_3	U5	NC		
3	IO_L52P_3	U6	NC		
3	IO_L51N_3/VREF_3	V2	NC		
3	IO_L51P_3	V3	NC		
3	IO_L50N_3	V4	NC		
3	IO_L50P_3	V5	NC		
3	IO_L49N_3	V6	NC		
3	IO_L49P_3	V7	NC		
3	IO_L48N_3	W1	NC		
3	IO_L48P_3	W2	NC		
3	IO_L47N_3	W3	NC		
3	IO_L47P_3	W4	NC		
3	IO_L46N_3	W5	NC		
3	IO_L46P_3	W6	NC		
3	IO_L45N_3/VREF_3	Y1	NC		
3	IO_L45P_3	AA1	NC		
3	IO_L44N_3	Y3	NC		
3	IO_L44P_3	Y4	NC		
3	IO_L43N_3	Y5	NC		
3	IO_L43P_3	Y6	NC		
3	IO_L42N_3	AA2	NC	NC	NC
3	IO_L42P_3	AA3	NC	NC	NC
3	IO_L41N_3	AA4	NC	NC	NC
3	IO_L41P_3	AA5	NC	NC	NC
3	IO_L39N_3/VREF_3	AB1	NC	NC	NC
3	IO_L39P_3	AB2	NC	NC	NC
3	IO_L06N_3	AB3			
3	IO_L06P_3	AB4			
3	IO_L05N_3	AC1			
3	IO_L05P_3	AC2			
3	IO_L04N_3	AD1			
3	IO_L04P_3	AD2			
3	IO_L03N_3/VREF_3	AE1			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
3	IO_L03P_3	AF2			
3	IO_L02N_3	AC3			
3	IO_L02P_3	AD4			
3	IO_L01N_3/VRP_3	AE3			
3	IO_L01P_3/VRN_3	AF3			
4	IO_L01N_4/DOUT	AC6			
4	IO_L01P_4/INIT_B	AD6			
4	IO_L02N_4/D0	AB7			
4	IO_L02P_4/D1	AC7			
4	IO_L03N_4/D2	AA7			
4	IO_L03P_4/D3	AA8			
4	IO_L05_4/No_Pair	Y8			
4	IO_L06N_4/VRP_4	AB8			
4	IO_L06P_4/VRN_4	AB9			
4	IO_L07N_4	AC8			
4	IO_L07P_4/VREF_4	AD8			
4	IO_L08N_4	AE8			
4	IO_L08P_4	AF8			
4	IO_L09N_4	Y9			
4	IO_L09P_4/VREF_4	AA9			
4	IO_L37N_4	AC9	NC	NC	
4	IO_L37P_4	AD9	NC	NC	
4	IO_L38N_4	Y10	NC	NC	
4	IO_L38P_4	W11	NC	NC	
4	IO_L39N_4	AA10	NC	NC	
4	IO_L39P_4	AA11	NC	NC	
4	IO_L43N_4	AB10	NC	NC	
4	IO_L43P_4	AC10	NC	NC	
4	IO_L44N_4	Y11	NC	NC	
4	IO_L44P_4	Y12	NC	NC	
4	IO_L45N_4	AB11	NC	NC	
4	IO_L45P_4/VREF_4	AC11	NC	NC	
4	IO_L67N_4	AA12			
4	IO_L67P_4	AB12			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
4	IO_L68N_4	AC12			
4	IO_L68P_4	AD12			
4	IO_L69N_4	W12			
4	IO_L69P_4/VREF_4	W13			
4	IO_L73N_4	Y13			
4	IO_L73P_4	AA13			
4	IO_L74N_4/GCLK3S	AB13			
4	IO_L74P_4/GCLK2P	AC13			
4	IO_L75N_4/GCLK1S	AD13			
4	IO_L75P_4/GCLK0P	AE13			
5	IO_L75N_5/GCLK7S	AE14			
5	IO_L75P_5/GCLK6P	AD14			
5	IO_L74N_5/GCLK5S	AC14			
5	IO_L74P_5/GCLK4P	AB14			
5	IO_L73N_5	AA14			
5	IO_L73P_5	Y14			
5	IO_L69N_5/VREF_5	W14			
5	IO_L69P_5	W15			
5	IO_L68N_5	AD15			
5	IO_L68P_5	AC15			
5	IO_L67N_5	AB15			
5	IO_L67P_5	AA15			
5	IO_L45N_5/VREF_5	AC16	NC	NC	
5	IO_L45P_5	AB16	NC	NC	
5	IO_L44N_5	Y15	NC	NC	
5	IO_L44P_5	Y16	NC	NC	
5	IO_L43N_5	AC17	NC	NC	
5	IO_L43P_5	AB17	NC	NC	
5	IO_L39N_5	AA16	NC	NC	
5	IO_L39P_5	AA17	NC	NC	
5	IO_L38N_5	W16	NC	NC	
5	IO_L38P_5	Y17	NC	NC	
5	IO_L37N_5	AD18	NC	NC	
5	IO_L37P_5	AC18	NC	NC	

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	**XC2V P4**	**XC2V P7**
5	IO_L09N_5/VREF_5	AA18			
5	IO_L09P_5	Y18			
5	IO_L08N_5	AF19			
5	IO_L08P_5	AE19			
5	IO_L07N_5/VREF_5	AD19			
5	IO_L07P_5	AC19			
5	IO_L06N_5/VRP_5	AB18			
5	IO_L06P_5/VRN_5	AB19			
5	IO_L05_5/No_Pair	Y19			
5	IO_L03N_5/D4	AA19			
5	IO_L03P_5/D5	AA20			
5	IO_L02N_5/D6	AC20			
5	IO_L02P_5/D7	AB20			
5	IO_L01N_5/RDWR_B	AD21			
5	IO_L01P_5/CS_B	AC21			
6	IO_L01P_6/VRN_6	AF24			
6	IO_L01N_6/VRP_6	AE24			
6	IO_L02P_6	AD23			
6	IO_L02N_6	AC24			
6	IO_L03P_6	AE26			
6	IO_L03N_6/VREF_6	AF25			
6	IO_L04P_6	AD25			
6	IO_L04N_6	AD26			
6	IO_L05P_6	AC25			
6	IO_L05N_6	AC26			
6	IO_L06P_6	AB23			
6	IO_L06N_6	AB24			
6	IO_L39P_6	AB25	NC	NC	NC
6	IO_L39N_6/VREF_6	AB26	NC	NC	NC
6	IO_L41P_6	AA22	NC	NC	NC
6	IO_L41N_6	AA23	NC	NC	NC
6	IO_L42P_6	AA24	NC	NC	NC
6	IO_L42N_6	AA25	NC	NC	NC
6	IO_L43P_6	Y21	NC		

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	**XC2V P4**	**XC2V P7**
6	IO_L43N_6	Y22	NC		
6	IO_L44P_6	Y23	NC		
6	IO_L44N_6	Y24	NC		
6	IO_L45P_6	AA26	NC		
6	IO_L45N_6/VREF_6	Y26	NC		
6	IO_L46P_6	W21	NC		
6	IO_L46N_6	W22	NC		
6	IO_L47P_6	W23	NC		
6	IO_L47N_6	W24	NC		
6	IO_L48P_6	W25	NC		
6	IO_L48N_6	W26	NC		
6	IO_L49P_6	V20	NC		
6	IO_L49N_6	V21	NC		
6	IO_L50P_6	V22	NC		
6	IO_L50N_6	V23	NC		
6	IO_L51P_6	V24	NC		
6	IO_L51N_6/VREF_6	V25	NC		
6	IO_L52P_6	U21	NC		
6	IO_L52N_6	U22	NC		
6	IO_L53P_6	U23	NC		
6	IO_L53N_6	U24	NC		
6	IO_L54P_6	V26	NC		
6	IO_L54N_6	U26	NC		
6	IO_L55P_6	U20	NC		
6	IO_L55N_6	T19	NC		
6	IO_L56P_6	T20	NC		
6	IO_L56N_6	R20	NC		
6	IO_L57P_6	T21	NC		
6	IO_L57N_6/VREF_6	T22	NC		
6	IO_L58P_6	T23	NC		
6	IO_L58N_6	T24	NC		
6	IO_L59P_6	T25	NC		
6	IO_L59N_6	T26	NC		
6	IO_L60P_6	R19	NC		
6	IO_L60N_6	P19	NC		

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
6	IO_L85P_6	R21			
6	IO_L85N_6	R22			
6	IO_L86P_6	R23			
6	IO_L86N_6	R24			
6	IO_L87P_6	R25			
6	IO_L87N_6/VREF_6	R26			
6	IO_L88P_6	P20			
6	IO_L88N_6	P21			
6	IO_L89P_6	P22			
6	IO_L89N_6	P23			
6	IO_L90P_6	P24			
6	IO_L90N_6	P25			
7	IO_L90P_7	N25			
7	IO_L90N_7	N24			
7	IO_L89P_7	N23			
7	IO_L89N_7	N22			
7	IO_L88P_7	N21			
7	IO_L88N_7/VREF_7	N20			
7	IO_L87P_7	M26			
7	IO_L87N_7	M25			
7	IO_L86P_7	M24			
7	IO_L86N_7	M23			
7	IO_L85P_7	M22			
7	IO_L85N_7	M21			
7	IO_L60P_7	N19	NC		
7	IO_L60N_7	M19	NC		
7	IO_L59P_7	L26	NC		
7	IO_L59N_7	L25	NC		
7	IO_L58P_7	L24	NC		
7	IO_L58N_7/VREF_7	L23	NC		
7	IO_L57P_7	L22	NC		
7	IO_L57N_7	L21	NC		
7	IO_L56P_7	M20	NC		
7	IO_L56N_7	L20	NC		

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
7	IO_L55P_7	L19	NC		
7	IO_L55N_7	K20	NC		
7	IO_L54P_7	K26	NC		
7	IO_L54N_7	J26	NC		
7	IO_L53P_7	K24	NC		
7	IO_L53N_7	K23	NC		
7	IO_L52P_7	K22	NC		
7	IO_L52N_7/VREF_7	K21	NC		
7	IO_L51P_7	J25	NC		
7	IO_L51N_7	J24	NC		
7	IO_L50P_7	J23	NC		
7	IO_L50N_7	J22	NC		
7	IO_L49P_7	J21	NC		
7	IO_L49N_7	J20	NC		
7	IO_L48P_7	H26	NC		
7	IO_L48N_7	H25	NC		
7	IO_L47P_7	H24	NC		
7	IO_L47N_7	H23	NC		
7	IO_L46P_7	H22	NC		
7	IO_L46N_7/VREF_7	H21	NC		
7	IO_L45P_7	G26	NC		
7	IO_L45N_7	F26	NC		
7	IO_L44P_7	G24	NC		
7	IO_L44N_7	G23	NC		
7	IO_L43P_7	G22	NC		
7	IO_L43N_7	G21	NC		
7	IO_L42P_7	F25	NC	NC	NC
7	IO_L42N_7	F24	NC	NC	NC
7	IO_L40P_7	F23	NC	NC	NC
7	IO_L40N_7/VREF_7	F22	NC	NC	NC
7	IO_L06P_7	E26			
7	IO_L06N_7	E25			
7	IO_L05P_7	E24			
7	IO_L05N_7	E23			
7	IO_L04P_7	D26			

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
7	IO_L04N_7/VREF_7	D25			
7	IO_L03P_7	C26			
7	IO_L03N_7	C25			
7	IO_L02P_7	B26			
7	IO_L02N_7	A25			
7	IO_L01P_7/VRN_7	D24			
7	IO_L01N_7/VRP_7	C23			
0	VCCO_0	C17			
0	VCCO_0	C20			
0	VCCO_0	H17			
0	VCCO_0	H18			
0	VCCO_0	J14			
0	VCCO_0	J15			
0	VCCO_0	J16			
1	VCCO_1	C7			
1	VCCO_1	H9			
1	VCCO_1	C10			
1	VCCO_1	H10			
1	VCCO_1	J11			
1	VCCO_1	J12			
1	VCCO_1	J13			
2	VCCO_2	G2			
2	VCCO_2	J8			
2	VCCO_2	K2			
2	VCCO_2	K8			
2	VCCO_2	L9			
2	VCCO_2	M9			
2	VCCO_2	N9			
3	VCCO_3	P9			
3	VCCO_3	R9			
3	VCCO_3	T9			
3	VCCO_3	U2			
3	VCCO_3	U8			
3	VCCO_3	V8			

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
3	VCCO_3	Y2			
4	VCCO_4	W9			
4	VCCO_4	AD7			
4	VCCO_4	V11			
4	VCCO_4	V12			
4	VCCO_4	V13			
4	VCCO_4	W10			
4	VCCO_4	AD10			
5	VCCO_5	V14			
5	VCCO_5	V15			
5	VCCO_5	V16			
5	VCCO_5	W17			
5	VCCO_5	W18			
5	VCCO_5	AD17			
5	VCCO_5	AD20			
6	VCCO_6	P18			
6	VCCO_6	R18			
6	VCCO_6	T18			
6	VCCO_6	U19			
6	VCCO_6	U25			
6	VCCO_6	V19			
6	VCCO_6	Y25			
7	VCCO_7	G25			
7	VCCO_7	J19			
7	VCCO_7	K19			
7	VCCO_7	K25			
7	VCCO_7	L18			
7	VCCO_7	M18			
7	VCCO_7	N18			
N/A	CCLK	W7			
N/A	PROG_B	D22			
N/A	DONE	AB6			
N/A	M0	AC22			
N/A	M1	W20			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	M2	AB21			
N/A	TCK	G8			
N/A	TDI	H20			
N/A	TDO	H7			
N/A	TMS	F7			
N/A	PWRDWN_B	AC5			
N/A	HSWAP_EN	E21			
N/A	RSVD	D5			
N/A	VBATT	E6			
N/A	DXP	F20			
N/A	DXN	G19			
N/A	AVCCAUXTX7	B11			
N/A	VTTXPAD7	B12			
N/A	TXNPAD7	A12			
N/A	TXPPAD7	A11			
N/A	GNDA7	C11			
N/A	GNDA7	C11			
N/A	RXPPAD7	A10			
N/A	RXNPAD7	A9			
N/A	VTRXPAD7	B10			
N/A	AVCCAUXRX7	B9			
N/A	AVCCAUXTX9	B6	NC	NC	
N/A	VTTXPAD9	B7	NC	NC	
N/A	TXNPAD9	A7	NC	NC	
N/A	TXPPAD9	A6	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	GNDA9	C5	NC	NC	
N/A	RXPPAD9	A5	NC	NC	
N/A	RXNPAD9	A4	NC	NC	
N/A	VTRXPAD9	B5	NC	NC	
N/A	AVCCAUXRX9	B4	NC	NC	
N/A	AVCCAUXRX16	AE4	NC	NC	
N/A	VTRXPAD16	AE5	NC	NC	
N/A	RXNPAD16	AF4	NC	NC	
N/A	RXPPAD16	AF5	NC	NC	

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	GNDA16	AD5	NC	NC	
N/A	GNDA16	AD5	NC	NC	
N/A	TXPPAD16	AF6	NC	NC	
N/A	TXNPAD16	AF7	NC	NC	
N/A	VTTXPAD16	AE7	NC	NC	
N/A	AVCCAUXTX16	AE6	NC	NC	
N/A	AVCCAUXRX18	AE9			
N/A	VTRXPAD18	AE10			
N/A	RXNPAD18	AF9			
N/A	RXPPAD18	AF10			
N/A	GNDA18	AD11			
N/A	GNDA18	AD11			
N/A	TXPPAD18	AF11			
N/A	TXNPAD18	AF12			
N/A	VTTXPAD18	AE12			
N/A	AVCCAUXTX18	AE11			
N/A	AVCCAUXTX4	B22	NC	NC	
N/A	VTTXPAD4	B23	NC	NC	
N/A	TXNPAD4	A23	NC	NC	
N/A	TXPPAD4	A22	NC	NC	
N/A	GNDA4	C22	NC	NC	
N/A	GNDA4	C22	NC	NC	
N/A	RXPPAD4	A21	NC	NC	
N/A	RXNPAD4	A20	NC	NC	
N/A	VTRXPAD4	B21	NC	NC	
N/A	AVCCAUXRX4	B20	NC	NC	
N/A	AVCCAUXTX6	B17			
N/A	VTTXPAD6	B18			
N/A	TXNPAD6	A18			
N/A	TXPPAD6	A17			
N/A	GNDA6	C16			
N/A	GNDA6	C16			
N/A	RXPPAD6	A16			
N/A	RXNPAD6	A15			
N/A	VTRXPAD6	B16			

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	AVCCAUXRX6	B15			
N/A	AVCCAUXRX19	AE15			
N/A	VTRXPAD19	AE16			
N/A	RXNPAD19	AF15			
N/A	RXPPAD19	AF16			
N/A	GNDA19	AD16			
N/A	GNDA19	AD16			
N/A	TXPPAD19	AF17			
N/A	TXNPAD19	AF18			
N/A	VTTXPAD19	AE18			
N/A	AVCCAUXTX19	AE17			
N/A	AVCCAUXRX21	AE20	NC	NC	
N/A	VTRXPAD21	AE21	NC	NC	
N/A	RXNPAD21	AF20	NC	NC	
N/A	RXPPAD21	AF21	NC	NC	
N/A	GNDA21	AD22	NC	NC	
N/A	GNDA21	AD22	NC	NC	
N/A	TXPPAD21	AF22	NC	NC	
N/A	TXNPAD21	AF23	NC	NC	
N/A	VTTXPAD21	AE23	NC	NC	
N/A	AVCCAUXTX21	AE22	NC	NC	
N/A	VCCINT	H8			
N/A	VCCINT	J9			
N/A	VCCINT	K9			
N/A	VCCINT	U9			
N/A	VCCINT	V9			
N/A	VCCINT	W8			
N/A	VCCINT	H19			
N/A	VCCINT	J10			
N/A	VCCINT	J17			
N/A	VCCINT	J18			
N/A	VCCINT	K11			
N/A	VCCINT	K16			
N/A	VCCINT	K18			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects XC2V P2	XC2V P4	XC2V P7
N/A	VCCINT	L10			
N/A	VCCINT	L17			
N/A	VCCINT	T10			
N/A	VCCINT	T17			
N/A	VCCINT	U11			
N/A	VCCINT	U16			
N/A	VCCINT	U18			
N/A	VCCINT	V10			
N/A	VCCINT	V17			
N/A	VCCINT	V18			
N/A	VCCINT	W19			
N/A	VCCAUX	B2			
N/A	VCCAUX	N1			
N/A	VCCAUX	P1			
N/A	VCCAUX	A13			
N/A	VCCAUX	A14			
N/A	VCCAUX	AE2			
N/A	VCCAUX	B25			
N/A	VCCAUX	N26			
N/A	VCCAUX	P26			
N/A	VCCAUX	AE25			
N/A	VCCAUX	AF13			
N/A	VCCAUX	AF14			
N/A	GND	C3			
N/A	GND	D4			
N/A	GND	E5			
N/A	GND	F6			
N/A	GND	G7			
N/A	GND	Y7			
N/A	GND	AA6			
N/A	GND	AB5			
N/A	GND	AC4			
N/A	GND	AD3			
N/A	GND	C24			
N/A	GND	D23			

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Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**

Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	GND	E22			
N/A	GND	F21			
N/A	GND	G20			
N/A	GND	K10			
N/A	GND	K12			
N/A	GND	K13			
N/A	GND	K14			
N/A	GND	K15			
N/A	GND	K17			
N/A	GND	L11			
N/A	GND	L12			
N/A	GND	L13			
N/A	GND	L14			
N/A	GND	L15			
N/A	GND	L16			
N/A	GND	M10			
N/A	GND	M11			
N/A	GND	M12			
N/A	GND	M13			
N/A	GND	M14			
N/A	GND	M15			
N/A	GND	M16			
N/A	GND	M17			
N/A	GND	N10			
N/A	GND	N11			
N/A	GND	N12			
N/A	GND	N13			
N/A	GND	N14			
N/A	GND	N15			
N/A	GND	N16			
N/A	GND	N17			
N/A	GND	P10			
N/A	GND	P11			
N/A	GND	P12			
N/A	GND	P13			

Table 8: **FF672 — XC2VP2, XC2VP4, and XC2VP7**
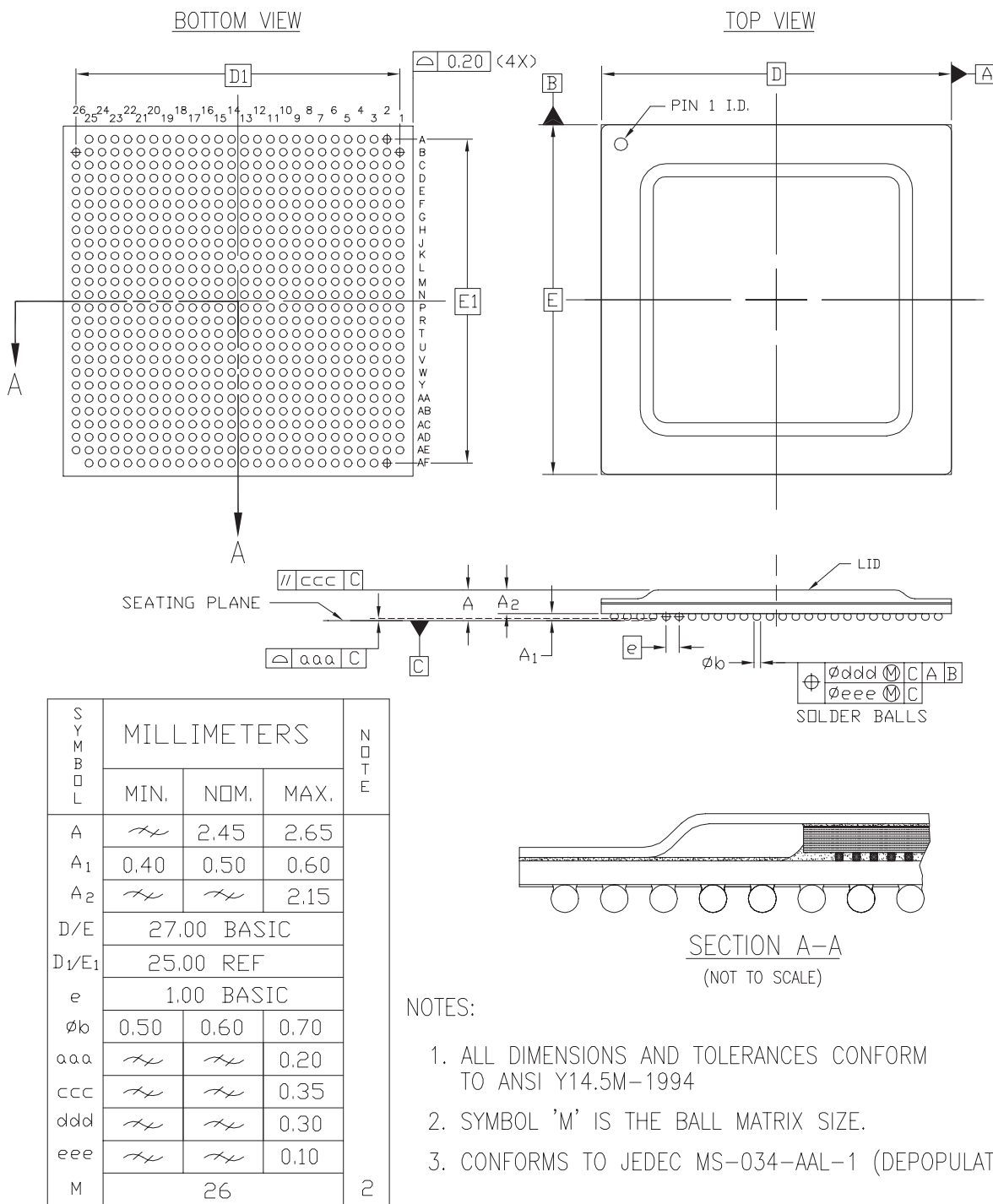
Bank	Pin Description	Pin Number	No Connects		
			XC2V P2	XC2V P4	XC2V P7
N/A	GND	P14			
N/A	GND	P15			
N/A	GND	P16			
N/A	GND	P17			
N/A	GND	R10			
N/A	GND	R11			
N/A	GND	R12			
N/A	GND	R13			
N/A	GND	R14			
N/A	GND	R15			
N/A	GND	R16			
N/A	GND	R17			
N/A	GND	T11			
N/A	GND	T12			
N/A	GND	T13			
N/A	GND	T14			
N/A	GND	T15			
N/A	GND	T16			
N/A	GND	U10			
N/A	GND	U12			
N/A	GND	U13			
N/A	GND	U14			
N/A	GND	U15			
N/A	GND	U17			
N/A	GND	Y20			
N/A	GND	AA21			
N/A	GND	AB22			
N/A	GND	AC23			
N/A	GND	AD24			

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FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

S Y M B O L	MILLIMETERS			N O T E
	MIN.	NOM.	MAX.	
A	~	2.45	2.65	
A$_1$	0.40	0.50	0.60	
A$_2$	~	~	2.15	
D/E	27.00 BASIC			
D$_1$/E$_1$	25.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994

2. SYMBOL 'M' IS THE BALL MATRIX SIZE.

3. CONFORMS TO JEDEC MS–034–AAL–1 (DEPOPULATED)

Figure 3: **FF672 Flip-Chip Fine-Pitch BGA Package Specifications**

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 9, the XC2VP7 and XC2VP20 Virtex-II Pro devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for differences shown in the "No Connects" column. Following this table are the **FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 9: **FF896 — XC2VP7 and XC2VP20**

			No Connects	
Bank	**Pin Description**	**Pin Number**	**XC2V P7**	**XC2V P20**
0	IO_L01N_0/VRP_0	E25		
0	IO_L01P_0/VRN_0	E24		
0	IO_L02N_0	F24		
0	IO_L02P_0	F23		
0	IO_L03N_0	E23		
0	IO_L03P_0/VREF_0	E22		
0	IO_L05_0/No_Pair	G23		
0	IO_L06N_0	H22		
0	IO_L06P_0	G22		
0	IO_L07N_0	F22		
0	IO_L07P_0	F21		
0	IO_L08N_0	D24		
0	IO_L08P_0	C24		
0	IO_L09N_0	H21		
0	IO_L09P_0/VREF_0	G21		
0	IO_L37N_0	E21		
0	IO_L37P_0	D21		
0	IO_L38N_0	D23		
0	IO_L38P_0	C23		
0	IO_L39N_0	H20		
0	IO_L39P_0	G20		
0	IO_L43N_0	E20		
0	IO_L43P_0	D20		
0	IO_L44N_0	B23		
0	IO_L44P_0	A23		
0	IO_L45N_0	H19		
0	IO_L45P_0/VREF_0	G19		
0	IO_L46N_0	E19	NC	
0	IO_L46P_0	E18	NC	
0	IO_L47N_0	C22	NC	
0	IO_L47P_0	B22	NC	
0	IO_L48N_0	F20	NC	
0	IO_L48P_0	F19	NC	

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
0	IO_L49N_0	G17	NC	
0	IO_L49P_0	F17	NC	
0	IO_L50_0/No_Pair	B21	NC	
0	IO_L53_0/No_Pair	A21	NC	
0	IO_L54N_0	H18	NC	
0	IO_L54P_0	G18	NC	
0	IO_L56N_0	C21	NC	
0	IO_L56P_0	C20	NC	
0	IO_L57N_0	J17	NC	
0	IO_L57P_0/VREF_0	H17	NC	
0	IO_L67N_0	E17		
0	IO_L67P_0	D17		
0	IO_L68N_0	D18		
0	IO_L68P_0	C18		
0	IO_L69N_0	J16		
0	IO_L69P_0/VREF_0	H16		
0	IO_L73N_0	E16		
0	IO_L73P_0	D16		
0	IO_L74N_0/GCLK7P	C16		
0	IO_L74P_0/GCLK6S	B16		
0	IO_L75N_0/GCLK5P	G16		
0	IO_L75P_0/GCLK4S	F16		
1	IO_L75N_1/GCLK3P	F15		
1	IO_L75P_1/GCLK2S	G15		
1	IO_L74N_1/GCLK1P	B15		
1	IO_L74P_1/GCLK0S	C15		
1	IO_L73N_1	D15		
1	IO_L73P_1	E15		
1	IO_L69N_1/VREF_1	H15		
1	IO_L69P_1	J15		
1	IO_L68N_1	C13		
1	IO_L68P_1	D13		
1	IO_L67N_1	D14		
1	IO_L67P_1	E14		
1	IO_L57N_1/VREF_1	H14	NC	
1	IO_L57P_1	J14	NC	

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
1	IO_L56N_1	C11	NC	
1	IO_L56P_1	C10	NC	
1	IO_L54N_1	G13	NC	
1	IO_L54P_1	H13	NC	
1	IO_L53_1/No_Pair	A10	NC	
1	IO_L50_1/No_Pair	B10	NC	
1	IO_L49N_1	F14	NC	
1	IO_L49P_1	G14	NC	
1	IO_L48N_1	F12	NC	
1	IO_L48P_1	F11	NC	
1	IO_L47N_1	B9	NC	
1	IO_L47P_1	C9	NC	
1	IO_L46N_1	E13	NC	
1	IO_L46P_1	E12	NC	
1	IO_L45N_1/VREF_1	G12		
1	IO_L45P_1	H12		
1	IO_L44N_1	A8		
1	IO_L44P_1	B8		
1	IO_L43N_1	D11		
1	IO_L43P_1	E11		
1	IO_L39N_1	G11		
1	IO_L39P_1	H11		
1	IO_L38N_1	C8		
1	IO_L38P_1	D8		
1	IO_L37N_1	D10		
1	IO_L37P_1	E10		
1	IO_L09N_1/VREF_1	G10		
1	IO_L09P_1	H10		
1	IO_L08N_1	C7		
1	IO_L08P_1	D7		
1	IO_L07N_1	F10		
1	IO_L07P_1	F9		
1	IO_L06N_1	G9		
1	IO_L06P_1	H9		
1	IO_L05_1/No_Pair	G8		
1	IO_L03N_1/VREF_1	E9		
1	IO_L03P_1	E8		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
1	IO_L02N_1	F8		
1	IO_L02P_1	F7		
1	IO_L01N_1/VRP_1	E7		
1	IO_L01P_1/VRN_1	E6		
2	IO_L01N_2/VRP_2	A3		
2	IO_L01P_2/VRN_2	B3		
2	IO_L02N_2	G6		
2	IO_L02P_2	G5		
2	IO_L03N_2	C5		
2	IO_L03P_2	D5		
2	IO_L04N_2/VREF_2	C2		
2	IO_L04P_2	C1		
2	IO_L05N_2	J8		
2	IO_L05P_2	J7		
2	IO_L06N_2	C4		
2	IO_L06P_2	D3		
2	IO_L31N_2	D2	NC	
2	IO_L31P_2	D1	NC	
2	IO_L32N_2	H6	NC	
2	IO_L32P_2	H5	NC	
2	IO_L33N_2	E4	NC	
2	IO_L33P_2	E3	NC	
2	IO_L34N_2/VREF_2	E2	NC	
2	IO_L34P_2	E1	NC	
2	IO_L35N_2	K8	NC	
2	IO_L35P_2	K7	NC	
2	IO_L36N_2	F4	NC	
2	IO_L36P_2	F3	NC	
2	IO_L37N_2	F2	NC	
2	IO_L37P_2	F1	NC	
2	IO_L38N_2	J6	NC	
2	IO_L38P_2	J5	NC	
2	IO_L39N_2	G4	NC	
2	IO_L39P_2	G3	NC	
2	IO_L40N_2/VREF_2	G2	NC	
2	IO_L40P_2	G1	NC	

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
2	IO_L41N_2	L8	NC	
2	IO_L41P_2	L7	NC	
2	IO_L42N_2	H4	NC	
2	IO_L42P_2	H3	NC	
2	IO_L43N_2	H2		
2	IO_L43P_2	J2		
2	IO_L44N_2	M8		
2	IO_L44P_2	M7		
2	IO_L45N_2	K6		
2	IO_L45P_2	K5		
2	IO_L46N_2/VREF_2	J1		
2	IO_L46P_2	K1		
2	IO_L47N_2	M6		
2	IO_L47P_2	M5		
2	IO_L48N_2	J4		
2	IO_L48P_2	J3		
2	IO_L49N_2	K2		
2	IO_L49P_2	L2		
2	IO_L50N_2	N8		
2	IO_L50P_2	N7		
2	IO_L51N_2	K4		
2	IO_L51P_2	K3		
2	IO_L52N_2/VREF_2	L1		
2	IO_L52P_2	M1		
2	IO_L53N_2	N6		
2	IO_L53P_2	N5		
2	IO_L54N_2	L5		
2	IO_L54P_2	L4		
2	IO_L55N_2	M2		
2	IO_L55P_2	N2		
2	IO_L56N_2	P9		
2	IO_L56P_2	R9		
2	IO_L57N_2	M4		
2	IO_L57P_2	M3		
2	IO_L58N_2/VREF_2	N1		
2	IO_L58P_2	P1		
2	IO_L59N_2	P8		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
2	IO_L59P_2	P7		
2	IO_L60N_2	N4		
2	IO_L60P_2	N3		
2	IO_L85N_2	P3		
2	IO_L85P_2	P2		
2	IO_L86N_2	R8		
2	IO_L86P_2	R7		
2	IO_L87N_2	P5		
2	IO_L87P_2	P4		
2	IO_L88N_2/VREF_2	R2		
2	IO_L88P_2	T2		
2	IO_L89N_2	R6		
2	IO_L89P_2	R5		
2	IO_L90N_2	R4		
2	IO_L90P_2	R3		
3	IO_L90N_3	U1		
3	IO_L90P_3	V1		
3	IO_L89N_3	T5		
3	IO_L89P_3	T6		
3	IO_L88N_3	T3		
3	IO_L88P_3	T4		
3	IO_L87N_3/VREF_3	U2		
3	IO_L87P_3	U3		
3	IO_L86N_3	T7		
3	IO_L86P_3	T8		
3	IO_L85N_3	U4		
3	IO_L85P_3	U5		
3	IO_L60N_3	V2		
3	IO_L60P_3	W2		
3	IO_L59N_3	T9		
3	IO_L59P_3	U9		
3	IO_L58N_3	V3		
3	IO_L58P_3	V4		
3	IO_L57N_3/VREF_3	W1		
3	IO_L57P_3	Y1		
3	IO_L56N_3	U7		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
3	IO_L56P_3	U8		
3	IO_L55N_3	V5		
3	IO_L55P_3	V6		
3	IO_L54N_3	Y2		
3	IO_L54P_3	AA2		
3	IO_L53N_3	V7		
3	IO_L53P_3	V8		
3	IO_L52N_3	W3		
3	IO_L52P_3	W4		
3	IO_L51N_3/VREF_3	AA1		
3	IO_L51P_3	AB1		
3	IO_L50N_3	W5		
3	IO_L50P_3	W6		
3	IO_L49N_3	Y4		
3	IO_L49P_3	Y5		
3	IO_L48N_3	AA3		
3	IO_L48P_3	AA4		
3	IO_L47N_3	W7		
3	IO_L47P_3	W8		
3	IO_L46N_3	AB3		
3	IO_L46P_3	AB4		
3	IO_L45N_3/VREF_3	AB2		
3	IO_L45P_3	AC2		
3	IO_L44N_3	AA5		
3	IO_L44P_3	AA6		
3	IO_L43N_3	AC3		
3	IO_L43P_3	AC4		
3	IO_L42N_3	AD1	NC	
3	IO_L42P_3	AD2	NC	
3	IO_L41N_3	Y7	NC	
3	IO_L41P_3	Y8	NC	
3	IO_L40N_3	AB5	NC	
3	IO_L40P_3	AB6	NC	
3	IO_L39N_3/VREF_3	AE1	NC	
3	IO_L39P_3	AE2	NC	
3	IO_L38N_3	AA7	NC	
3	IO_L38P_3	AA8	NC	

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
3	IO_L37N_3	AD3	NC	
3	IO_L37P_3	AD4	NC	
3	IO_L36N_3	AF1	NC	
3	IO_L36P_3	AF2	NC	
3	IO_L35N_3	AC5	NC	
3	IO_L35P_3	AC6	NC	
3	IO_L34N_3	AF3	NC	
3	IO_L34P_3	AF4	NC	
3	IO_L33N_3/VREF_3	AE3	NC	
3	IO_L33P_3	AE4	NC	
3	IO_L32N_3	AB7	NC	
3	IO_L32P_3	AB8	NC	
3	IO_L31N_3	AE5	NC	
3	IO_L31P_3	AF6	NC	
3	IO_L06N_3	AG1		
3	IO_L06P_3	AG2		
3	IO_L05N_3	AD5		
3	IO_L05P_3	AD6		
3	IO_L04N_3	AG3		
3	IO_L04P_3	AH4		
3	IO_L03N_3/VREF_3	AH1		
3	IO_L03P_3	AH2		
3	IO_L02N_3	AG5		
3	IO_L02P_3	AH5		
3	IO_L01N_3/VRP_3	AJ3		
3	IO_L01P_3/VRN_3	AK3		
4	IO_L01N_4/DOUT	AG6		
4	IO_L01P_4/INIT_B	AF7		
4	IO_L02N_4/D0	AC9		
4	IO_L02P_4/D1	AD9		
4	IO_L03N_4/D2	AG7		
4	IO_L03P_4/D3	AH7		
4	IO_L05_4/No_Pair	AD8		
4	IO_L06N_4/VRP_4	AG8		
4	IO_L06P_4/VRN_4	AH8		
4	IO_L07N_4	AC10		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
4	IO_L07P_4/VREF_4	AD10		
4	IO_L08N_4	AE7		
4	IO_L08P_4	AE8		
4	IO_L09N_4	AJ8		
4	IO_L09P_4/VREF_4	AK8		
4	IO_L37N_4	AC11		
4	IO_L37P_4	AD11		
4	IO_L38N_4	AF8		
4	IO_L38P_4	AF9		
4	IO_L39N_4	AF10		
4	IO_L39P_4	AG10		
4	IO_L43N_4	AC12		
4	IO_L43P_4	AD12		
4	IO_L44N_4	AE9		
4	IO_L44P_4	AE10		
4	IO_L45N_4	AH9		
4	IO_L45P_4/VREF_4	AJ9		
4	IO_L46N_4	AC13	NC	
4	IO_L46P_4	AD13	NC	
4	IO_L47N_4	AE11	NC	
4	IO_L47P_4	AE12	NC	
4	IO_L48N_4	AH10	NC	
4	IO_L48P_4	AH11	NC	
4	IO_L49N_4	AB14	NC	
4	IO_L49P_4	AC14	NC	
4	IO_L50_4/No_Pair	AF11	NC	
4	IO_L53_4/No_Pair	AG11	NC	
4	IO_L54N_4	AJ10	NC	
4	IO_L54P_4	AK10	NC	
4	IO_L56N_4	AF12	NC	
4	IO_L56P_4	AF13	NC	
4	IO_L57N_4	AG13	NC	
4	IO_L57P_4/VREF_4	AH13	NC	
4	IO_L67N_4	AB15		
4	IO_L67P_4	AC15		
4	IO_L68N_4	AD14		
4	IO_L68P_4	AE14		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
4	IO_L69N_4	AF14		
4	IO_L69P_4/VREF_4	AG14		
4	IO_L73N_4	AD15		
4	IO_L73P_4	AE15		
4	IO_L74N_4/GCLK3S	AF15		
4	IO_L74P_4/GCLK2P	AG15		
4	IO_L75N_4/GCLK1S	AH15		
4	IO_L75P_4/GCLK0P	AJ15		
5	IO_L75N_5/GCLK7S	AJ16		
5	IO_L75P_5/GCLK6P	AH16		
5	IO_L74N_5/GCLK5S	AG16		
5	IO_L74P_5/GCLK4P	AF16		
5	IO_L73N_5	AE16		
5	IO_L73P_5	AD16		
5	IO_L69N_5/VREF_5	AG17		
5	IO_L69P_5	AF17		
5	IO_L68N_5	AE17		
5	IO_L68P_5	AD17		
5	IO_L67N_5	AC16		
5	IO_L67P_5	AB16		
5	IO_L57N_5/VREF_5	AH18	NC	
5	IO_L57P_5	AG18	NC	
5	IO_L56N_5	AF18	NC	
5	IO_L56P_5	AF19	NC	
5	IO_L54N_5	AK21	NC	
5	IO_L54P_5	AJ21	NC	
5	IO_L53_5/No_Pair	AG20	NC	
5	IO_L50_5/No_Pair	AF20	NC	
5	IO_L49N_5	AC17	NC	
5	IO_L49P_5	AB17	NC	
5	IO_L48N_5	AH20	NC	
5	IO_L48P_5	AH21	NC	
5	IO_L47N_5	AE19	NC	
5	IO_L47P_5	AE20	NC	
5	IO_L46N_5	AD18	NC	
5	IO_L46P_5	AC18	NC	

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
5	IO_L45N_5/VREF_5	AJ22		
5	IO_L45P_5	AH22		
5	IO_L44N_5	AE21		
5	IO_L44P_5	AE22		
5	IO_L43N_5	AD19		
5	IO_L43P_5	AC19		
5	IO_L39N_5	AG21		
5	IO_L39P_5	AF21		
5	IO_L38N_5	AF22		
5	IO_L38P_5	AF23		
5	IO_L37N_5	AD20		
5	IO_L37P_5	AC20		
5	IO_L09N_5/VREF_5	AK23		
5	IO_L09P_5	AJ23		
5	IO_L08N_5	AE23		
5	IO_L08P_5	AE24		
5	IO_L07N_5/VREF_5	AD21		
5	IO_L07P_5	AC21		
5	IO_L06N_5/VRP_5	AH23		
5	IO_L06P_5/VRN_5	AG23		
5	IO_L05_5/No_Pair	AD23		
5	IO_L03N_5/D4	AH24		
5	IO_L03P_5/D5	AG24		
5	IO_L02N_5/D6	AD22		
5	IO_L02P_5/D7	AC22		
5	IO_L01N_5/RDWR_B	AF24		
5	IO_L01P_5/CS_B	AG25		
6	IO_L01P_6/VRN_6	AK28		
6	IO_L01N_6/VRP_6	AJ28		
6	IO_L02P_6	AH26		
6	IO_L02N_6	AG26		
6	IO_L03P_6	AH29		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AH27		
6	IO_L04N_6	AG28		
6	IO_L05P_6	AD25		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P7	XC2V P20
6	IO_L05N_6	AD26		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AG30		
6	IO_L31P_6	AF25	NC	
6	IO_L31N_6	AE26	NC	
6	IO_L32P_6	AB23	NC	
6	IO_L32N_6	AB24	NC	
6	IO_L33P_6	AE27	NC	
6	IO_L33N_6/VREF_6	AE28	NC	
6	IO_L34P_6	AF27	NC	
6	IO_L34N_6	AF28	NC	
6	IO_L35P_6	AC25	NC	
6	IO_L35N_6	AC26	NC	
6	IO_L36P_6	AF29	NC	
6	IO_L36N_6	AF30	NC	
6	IO_L37P_6	AD27	NC	
6	IO_L37N_6	AD28	NC	
6	IO_L38P_6	AA23	NC	
6	IO_L38N_6	AA24	NC	
6	IO_L39P_6	AE29	NC	
6	IO_L39N_6/VREF_6	AE30	NC	
6	IO_L40P_6	AB25	NC	
6	IO_L40N_6	AB26	NC	
6	IO_L41P_6	Y23	NC	
6	IO_L41N_6	Y24	NC	
6	IO_L42P_6	AD29	NC	
6	IO_L42N_6	AD30	NC	
6	IO_L43P_6	AC27		
6	IO_L43N_6	AC28		
6	IO_L44P_6	AA25		
6	IO_L44N_6	AA26		
6	IO_L45P_6	AC29		
6	IO_L45N_6/VREF_6	AB29		
6	IO_L46P_6	AB27		
6	IO_L46N_6	AB28		
6	IO_L47P_6	W23		
6	IO_L47N_6	W24		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	XC2V P20
6	IO_L48P_6	AA27		
6	IO_L48N_6	AA28		
6	IO_L49P_6	Y26		
6	IO_L49N_6	Y27		
6	IO_L50P_6	W25		
6	IO_L50N_6	W26		
6	IO_L51P_6	AB30		
6	IO_L51N_6/VREF_6	AA30		
6	IO_L52P_6	W27		
6	IO_L52N_6	W28		
6	IO_L53P_6	V23		
6	IO_L53N_6	V24		
6	IO_L54P_6	AA29		
6	IO_L54N_6	Y29		
6	IO_L55P_6	V25		
6	IO_L55N_6	V26		
6	IO_L56P_6	U23		
6	IO_L56N_6	U24		
6	IO_L57P_6	Y30		
6	IO_L57N_6/VREF_6	W30		
6	IO_L58P_6	V27		
6	IO_L58N_6	V28		
6	IO_L59P_6	U22		
6	IO_L59N_6	T22		
6	IO_L60P_6	W29		
6	IO_L60N_6	V29		
6	IO_L85P_6	U26		
6	IO_L85N_6	U27		
6	IO_L86P_6	T23		
6	IO_L86N_6	T24		
6	IO_L87P_6	U28		
6	IO_L87N_6/VREF_6	U29		
6	IO_L88P_6	T27		
6	IO_L88N_6	T28		
6	IO_L89P_6	T25		
6	IO_L89N_6	T26		
6	IO_L90P_6	V30		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P7	XC2V P20
6	IO_L90N_6	U30		
7	IO_L90P_7	R28		
7	IO_L90N_7	R27		
7	IO_L89P_7	R26		
7	IO_L89N_7	R25		
7	IO_L88P_7	T29		
7	IO_L88N_7/VREF_7	R29		
7	IO_L87P_7	P27		
7	IO_L87N_7	P26		
7	IO_L86P_7	R24		
7	IO_L86N_7	R23		
7	IO_L85P_7	P29		
7	IO_L85N_7	P28		
7	IO_L60P_7	N28		
7	IO_L60N_7	N27		
7	IO_L59P_7	P24		
7	IO_L59N_7	P23		
7	IO_L58P_7	P30		
7	IO_L58N_7/VREF_7	N30		
7	IO_L57P_7	M28		
7	IO_L57N_7	M27		
7	IO_L56P_7	R22		
7	IO_L56N_7	P22		
7	IO_L55P_7	N29		
7	IO_L55N_7	M29		
7	IO_L54P_7	L27		
7	IO_L54N_7	L26		
7	IO_L53P_7	N26		
7	IO_L53N_7	N25		
7	IO_L52P_7	M30		
7	IO_L52N_7/VREF_7	L30		
7	IO_L51P_7	K28		
7	IO_L51N_7	K27		
7	IO_L50P_7	N24		
7	IO_L50N_7	N23		
7	IO_L49P_7	L29		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
7	IO_L49N_7	K29		
7	IO_L48P_7	J28		
7	IO_L48N_7	J27		
7	IO_L47P_7	M26		
7	IO_L47N_7	M25		
7	IO_L46P_7	K30		
7	IO_L46N_7/VREF_7	J30		
7	IO_L45P_7	K26		
7	IO_L45N_7	K25		
7	IO_L44P_7	M24		
7	IO_L44N_7	M23		
7	IO_L43P_7	J29		
7	IO_L43N_7	H29		
7	IO_L42P_7	H28	NC	
7	IO_L42N_7	H27	NC	
7	IO_L41P_7	L24	NC	
7	IO_L41N_7	L23	NC	
7	IO_L40P_7	G30	NC	
7	IO_L40N_7/VREF_7	G29	NC	
7	IO_L39P_7	G28	NC	
7	IO_L39N_7	G27	NC	
7	IO_L38P_7	J26	NC	
7	IO_L38N_7	J25	NC	
7	IO_L37P_7	F30	NC	
7	IO_L37N_7	F29	NC	
7	IO_L36P_7	F28	NC	
7	IO_L36N_7	F27	NC	
7	IO_L35P_7	K24	NC	
7	IO_L35N_7	K23	NC	
7	IO_L34P_7	E30	NC	
7	IO_L34N_7/VREF_7	E29	NC	
7	IO_L33P_7	E28	NC	
7	IO_L33N_7	E27	NC	
7	IO_L32P_7	H26	NC	
7	IO_L32N_7	H25	NC	
7	IO_L31P_7	D30	NC	
7	IO_L31N_7	D29	NC	

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P7	XC2V P20
7	IO_L06P_7	D28		
7	IO_L06N_7	C27		
7	IO_L05P_7	J24		
7	IO_L05N_7	J23		
7	IO_L04P_7	C30		
7	IO_L04N_7/VREF_7	C29		
7	IO_L03P_7	D26		
7	IO_L03N_7	C26		
7	IO_L02P_7	G26		
7	IO_L02N_7	G25		
7	IO_L01P_7/VRN_7	B28		
7	IO_L01N_7/VRP_7	A28		
0	VCCO_0	K21		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	K10		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
2	VCCO_2	M10		
2	VCCO_2	M9		
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	J9		
3	VCCO_3	AB9		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
4	VCCO_4	AA10		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA21		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		
6	VCCO_6	AB22		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	XC2V P20
6	VCCO_6	AA22		
6	VCCO_6	Y22		
6	VCCO_6	Y21		
6	VCCO_6	W22		
6	VCCO_6	W21		
6	VCCO_6	V22		
6	VCCO_6	V21		
6	VCCO_6	U21		
6	VCCO_6	T21		
7	VCCO_7	R21		
7	VCCO_7	P21		
7	VCCO_7	N22		
7	VCCO_7	N21		
7	VCCO_7	M22		
7	VCCO_7	M21		
7	VCCO_7	L22		
7	VCCO_7	L21		
7	VCCO_7	K22		
7	VCCO_7	J22		
N/A	CCLK	AC7		
N/A	PROG_B	G24		
N/A	DONE	AC8		
N/A	M0	AD24		
N/A	M1	AC24		
N/A	M2	AC23		
N/A	TCK	G7		
N/A	TDI	F26		
N/A	TDO	F5		
N/A	TMS	H8		
N/A	PWRDWN_B	AD7		
N/A	HSWAP_EN	H23		
N/A	RSVD	D6		
N/A	VBATT	H7		
N/A	DXP	H24		
N/A	DXN	D25		
N/A	AVCCAUXTX4	B26		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
N/A	VTTXPAD4	B27		
N/A	TXNPAD4	A27		
N/A	TXPPAD4	A26		
N/A	GNDA4	C25		
N/A	GNDA4	C25		
N/A	RXPPAD4	A25		
N/A	RXNPAD4	A24		
N/A	VTRXPAD4	B25		
N/A	AVCCAUXRX4	B24		
N/A	AVCCAUXTX6	B19		
N/A	VTTXPAD6	B20		
N/A	TXNPAD6	A20		
N/A	TXPPAD6	A19		
N/A	GNDA6	C19		
N/A	GNDA6	C19		
N/A	RXPPAD6	A18		
N/A	RXNPAD6	A17		
N/A	VTRXPAD6	B18		
N/A	AVCCAUXRX6	B17		
N/A	AVCCAUXTX7	B13		
N/A	VTTXPAD7	B14		
N/A	TXNPAD7	A14		
N/A	TXPPAD7	A13		
N/A	GNDA7	C12		
N/A	GNDA7	C12		
N/A	RXPPAD7	A12		
N/A	RXNPAD7	A11		
N/A	VTRXPAD7	B12		
N/A	AVCCAUXRX7	B11		
N/A	AVCCAUXTX9	B6		
N/A	VTTXPAD9	B7		
N/A	TXNPAD9	A7		
N/A	TXPPAD9	A6		
N/A	GNDA9	C6		
N/A	GNDA9	C6		
N/A	RXPPAD9	A5		
N/A	RXNPAD9	A4		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P7	**XC2V P20**
N/A	VTRXPAD9	B5		
N/A	AVCCAUXRX9	B4		
N/A	AVCCAUXRX16	AJ4		
N/A	VTRXPAD16	AJ5		
N/A	RXNPAD16	AK4		
N/A	RXPPAD16	AK5		
N/A	GNDA16	AH6		
N/A	GNDA16	AH6		
N/A	TXPPAD16	AK6		
N/A	TXNPAD16	AK7		
N/A	VTTXPAD16	AJ7		
N/A	AVCCAUXTX16	AJ6		
N/A	AVCCAUXRX18	AJ11		
N/A	VTRXPAD18	AJ12		
N/A	RXNPAD18	AK11		
N/A	RXPPAD18	AK12		
N/A	GNDA18	AH12		
N/A	GNDA18	AH12		
N/A	TXPPAD18	AK13		
N/A	TXNPAD18	AK14		
N/A	VTTXPAD18	AJ14		
N/A	AVCCAUXTX18	AJ13		
N/A	AVCCAUXRX19	AJ17		
N/A	VTRXPAD19	AJ18		
N/A	RXNPAD19	AK17		
N/A	RXPPAD19	AK18		
N/A	GNDA19	AH19		
N/A	GNDA19	AH19		
N/A	TXPPAD19	AK19		
N/A	TXNPAD19	AK20		
N/A	VTTXPAD19	AJ20		
N/A	AVCCAUXTX19	AJ19		
N/A	AVCCAUXRX21	AJ24		
N/A	VTRXPAD21	AJ25		
N/A	RXNPAD21	AK24		
N/A	RXPPAD21	AK25		
N/A	GNDA21	AH25		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
N/A	GNDA21	AH25		
N/A	TXPPAD21	AK26		
N/A	TXNPAD21	AK27		
N/A	VTTXPAD21	AJ27		
N/A	AVCCAUXTX21	AJ26		
N/A	VCCAUX	AK29		
N/A	VCCAUX	AK16		
N/A	VCCAUX	AK15		
N/A	VCCAUX	AK2		
N/A	VCCAUX	AJ30		
N/A	VCCAUX	AJ1		
N/A	VCCAUX	T30		
N/A	VCCAUX	T1		
N/A	VCCAUX	R30		
N/A	VCCAUX	R1		
N/A	VCCAUX	B30		
N/A	VCCAUX	B1		
N/A	VCCAUX	A29		
N/A	VCCAUX	A16		
N/A	VCCAUX	A15		
N/A	VCCAUX	A2		
N/A	VCCINT	Y19		
N/A	VCCINT	Y18		
N/A	VCCINT	Y17		
N/A	VCCINT	Y16		
N/A	VCCINT	Y15		
N/A	VCCINT	Y14		
N/A	VCCINT	Y13		
N/A	VCCINT	Y12		
N/A	VCCINT	W20		
N/A	VCCINT	W11		
N/A	VCCINT	V20		
N/A	VCCINT	V11		
N/A	VCCINT	U20		
N/A	VCCINT	U11		
N/A	VCCINT	T20		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P7	XC2V P20
N/A	VCCINT	T11		
N/A	VCCINT	R20		
N/A	VCCINT	R11		
N/A	VCCINT	P20		
N/A	VCCINT	P11		
N/A	VCCINT	N20		
N/A	VCCINT	N11		
N/A	VCCINT	M20		
N/A	VCCINT	M11		
N/A	VCCINT	L19		
N/A	VCCINT	L18		
N/A	VCCINT	L17		
N/A	VCCINT	L16		
N/A	VCCINT	L15		
N/A	VCCINT	L14		
N/A	VCCINT	L13		
N/A	VCCINT	L12		
N/A	GND	AK22		
N/A	GND	AK9		
N/A	GND	AJ29		
N/A	GND	AJ2		
N/A	GND	AH28		
N/A	GND	AH17		
N/A	GND	AH14		
N/A	GND	AH3		
N/A	GND	AG27		
N/A	GND	AG22		
N/A	GND	AG19		
N/A	GND	AG12		
N/A	GND	AG9		
N/A	GND	AG4		
N/A	GND	AF26		
N/A	GND	AF5		
N/A	GND	AE25		
N/A	GND	AE18		
N/A	GND	AE13		
N/A	GND	AE6		

Table 9: **FF896 — XC2VP7 and XC2VP20**

| | | | No Connects | |
| | | | XC2V
P7 | XC2V
P20 |
Bank	Pin Description	Pin Number		
N/A	GND	AC30		
N/A	GND	AC1		
N/A	GND	Y28		
N/A	GND	Y25		
N/A	GND	Y20		
N/A	GND	Y11		
N/A	GND	Y6		
N/A	GND	Y3		
N/A	GND	W19		
N/A	GND	W18		
N/A	GND	W17		
N/A	GND	W16		
N/A	GND	W15		
N/A	GND	W14		
N/A	GND	W13		
N/A	GND	W12		
N/A	GND	V19		
N/A	GND	V18		
N/A	GND	V17		
N/A	GND	V16		
N/A	GND	V15		
N/A	GND	V14		
N/A	GND	V13		
N/A	GND	V12		
N/A	GND	U25		
N/A	GND	U19		
N/A	GND	U18		
N/A	GND	U17		
N/A	GND	U16		
N/A	GND	U15		
N/A	GND	U14		
N/A	GND	U13		
N/A	GND	U12		
N/A	GND	U6		
N/A	GND	T19		
N/A	GND	T18		
N/A	GND	T17		

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Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	No Connects XC2V P20
N/A	GND	T16		
N/A	GND	T15		
N/A	GND	T14		
N/A	GND	T13		
N/A	GND	T12		
N/A	GND	R19		
N/A	GND	R18		
N/A	GND	R17		
N/A	GND	R16		
N/A	GND	R15		
N/A	GND	R14		
N/A	GND	R13		
N/A	GND	R12		
N/A	GND	P25		
N/A	GND	P19		
N/A	GND	P18		
N/A	GND	P17		
N/A	GND	P16		
N/A	GND	P15		
N/A	GND	P14		
N/A	GND	P13		
N/A	GND	P12		
N/A	GND	P6		
N/A	GND	N19		
N/A	GND	N18		
N/A	GND	N17		
N/A	GND	N16		
N/A	GND	N15		
N/A	GND	N14		
N/A	GND	N13		
N/A	GND	N12		
N/A	GND	M19		
N/A	GND	M18		
N/A	GND	M17		
N/A	GND	M16		
N/A	GND	M15		
N/A	GND	M14		

Table 9: **FF896 — XC2VP7 and XC2VP20**

Bank	Pin Description	Pin Number	No Connects XC2V P7	XC2V P20
N/A	GND	M13		
N/A	GND	M12		
N/A	GND	L28		
N/A	GND	L25		
N/A	GND	L20		
N/A	GND	L11		
N/A	GND	L6		
N/A	GND	L3		
N/A	GND	H30		
N/A	GND	H1		
N/A	GND	F25		
N/A	GND	F18		
N/A	GND	F13		
N/A	GND	F6		
N/A	GND	E26		
N/A	GND	E5		
N/A	GND	D27		
N/A	GND	D22		
N/A	GND	D19		
N/A	GND	D12		
N/A	GND	D9		
N/A	GND	D4		
N/A	GND	C28		
N/A	GND	C17		
N/A	GND	C14		
N/A	GND	C3		
N/A	GND	B29		
N/A	GND	B2		
N/A	GND	A22		
N/A	GND	A9		

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FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

BOTTOM VIEW

TOP VIEW

SECTION A-A
(NOT TO SCALE)

S Y M B O L	MILLIMETERS			N O T E
	MIN.	NOM.	MAX.	
A	~	3.20	3.40	
A$_1$	0.40	0.50	0.60	
A$_2$	~	~	2.80	
D/E	31.00 BASIC			
D$_1$/E$_1$	29.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994

2. SYMBOL 'M' IS THE BALL MATRIX SIZE.

3. CONFORMS TO JEDEC MS-034-AAN-1 (DEPOPULATED)

Figure 4: **FF896 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 10, XC2VP20 and XC2VP50 Virtex-II Pro devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the differences shown in the No Connect column. Following this table are the **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
0	IO_L01N_0/VRP_0	E29		
0	IO_L01P_0/VRN_0	E28		
0	IO_L02N_0	H26		
0	IO_L02P_0	G26		
0	IO_L03N_0	H25		
0	IO_L03P_0/VREF_0	G25		
0	IO_L05_0/No_Pair	J25		
0	IO_L06N_0	K24		
0	IO_L06P_0	J24		
0	IO_L07N_0	F26		
0	IO_L07P_0	E26		
0	IO_L08N_0	D30		
0	IO_L08P_0	D29		
0	IO_L09N_0	K23		
0	IO_L09P_0/VREF_0	J23		
0	IO_L19N_0	F24	NC	
0	IO_L19P_0	E24	NC	
0	IO_L20N_0	D28	NC	
0	IO_L20P_0	C28	NC	
0	IO_L21N_0	H24	NC	
0	IO_L21P_0	G24	NC	
0	IO_L25N_0	G23	NC	
0	IO_L25P_0	F23	NC	
0	IO_L26N_0	E27	NC	
0	IO_L26P_0	D27	NC	
0	IO_L27N_0	K22	NC	
0	IO_L27P_0/VREF_0	J22	NC	
0	IO_L37N_0	H22		
0	IO_L37P_0	G22		
0	IO_L38N_0	D26		
0	IO_L38P_0	C26		
0	IO_L39N_0	K21		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	**XC2V P50**
0	IO_L39P_0	J21		
0	IO_L43N_0	F22		
0	IO_L43P_0	E22		
0	IO_L44N_0	E25		
0	IO_L44P_0	D25		
0	IO_L45N_0	H21		
0	IO_L45P_0/VREF_0	G21		
0	IO_L46N_0	D22		
0	IO_L46P_0	D23		
0	IO_L47N_0	D24		
0	IO_L47P_0	C24		
0	IO_L48N_0	K20		
0	IO_L48P_0	J20		
0	IO_L49N_0	F21		
0	IO_L49P_0	E21		
0	IO_L50_0/No_Pair	C21		
0	IO_L53_0/No_Pair	C22		
0	IO_L54N_0	L19		
0	IO_L54P_0	K19		
0	IO_L55N_0	G20		
0	IO_L55P_0	F20		
0	IO_L56N_0	D21		
0	IO_L56P_0	D20		
0	IO_L57N_0	J19		
0	IO_L57P_0/VREF_0	H19		
0	IO_L67N_0	G19		
0	IO_L67P_0	F19		
0	IO_L68N_0	E19		
0	IO_L68P_0	D19		
0	IO_L69N_0	L18		
0	IO_L69P_0/VREF_0	K18		
0	IO_L73N_0	G18		
0	IO_L73P_0	F18		
0	IO_L74N_0/GCLK7P	E18		
0	IO_L74P_0/GCLK6S	D18		
0	IO_L75N_0/GCLK5P	J18		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
0	IO_L75P_0/GCLK4S	H18		
1	IO_L75N_1/GCLK3P	H17		
1	IO_L75P_1/GCLK2S	J17		
1	IO_L74N_1/GCLK1P	D17		
1	IO_L74P_1/GCLK0S	E17		
1	IO_L73N_1	F17		
1	IO_L73P_1	G17		
1	IO_L69N_1/VREF_1	K17		
1	IO_L69P_1	L17		
1	IO_L68N_1	D16		
1	IO_L68P_1	E16		
1	IO_L67N_1	F16		
1	IO_L67P_1	G16		
1	IO_L57N_1/VREF_1	H16		
1	IO_L57P_1	J16		
1	IO_L56N_1	D15		
1	IO_L56P_1	D14		
1	IO_L55N_1	F15		
1	IO_L55P_1	G15		
1	IO_L54N_1	K16		
1	IO_L54P_1	L16		
1	IO_L53_1/No_Pair	C13		
1	IO_L50_1/No_Pair	C14		
1	IO_L49N_1	E14		
1	IO_L49P_1	F14		
1	IO_L48N_1	J15		
1	IO_L48P_1	K15		
1	IO_L47N_1	C11		
1	IO_L47P_1	D11		
1	IO_L46N_1	D12		
1	IO_L46P_1	D13		
1	IO_L45N_1/VREF_1	G14		
1	IO_L45P_1	H14		
1	IO_L44N_1	D10		
1	IO_L44P_1	E10		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
1	IO_L43N_1	E13		
1	IO_L43P_1	F13		
1	IO_L39N_1	J14		
1	IO_L39P_1	K14		
1	IO_L38N_1	C9		
1	IO_L38P_1	D9		
1	IO_L37N_1	G13		
1	IO_L37P_1	H13		
1	IO_L27N_1/VREF_1	J13	NC	
1	IO_L27P_1	K13	NC	
1	IO_L26N_1	D8	NC	
1	IO_L26P_1	E8	NC	
1	IO_L25N_1	F12	NC	
1	IO_L25P_1	G12	NC	
1	IO_L21N_1	G11	NC	
1	IO_L21P_1	H11	NC	
1	IO_L20N_1	C7	NC	
1	IO_L20P_1	D7	NC	
1	IO_L19N_1	E11	NC	
1	IO_L19P_1	F11	NC	
1	IO_L09N_1/VREF_1	J12		
1	IO_L09P_1	K12		
1	IO_L08N_1	D6		
1	IO_L08P_1	D5		
1	IO_L07N_1	E9		
1	IO_L07P_1	F9		
1	IO_L06N_1	J11		
1	IO_L06P_1	K11		
1	IO_L05_1/No_Pair	J10		
1	IO_L03N_1/VREF_1	G10		
1	IO_L03P_1	H10		
1	IO_L02N_1	G9		
1	IO_L02P_1	H9		
1	IO_L01N_1/VRP_1	E7		
1	IO_L01P_1/VRN_1	E6		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
2	IO_L01N_2/VRP_2	D2		
2	IO_L01P_2/VRN_2	D1		
2	IO_L02N_2	F8		
2	IO_L02P_2	F7		
2	IO_L03N_2	E4		
2	IO_L03P_2	E3		
2	IO_L04N_2/VREF_2	E2		
2	IO_L04P_2	E1		
2	IO_L05N_2	J8		
2	IO_L05P_2	J7		
2	IO_L06N_2	F5		
2	IO_L06P_2	F4		
2	IO_L07N_2	G4	NC	
2	IO_L07P_2	G3	NC	
2	IO_L09N_2	G6	NC	
2	IO_L09P_2	G5	NC	
2	IO_L10N_2/VREF_2	F2	NC	
2	IO_L10P_2	F1	NC	
2	IO_L11N_2	L10	NC	
2	IO_L11P_2	L9	NC	
2	IO_L12N_2	H6	NC	
2	IO_L12P_2	H5	NC	
2	IO_L13N_2	G2	NC	
2	IO_L13P_2	G1	NC	
2	IO_L15N_2	J6	NC	
2	IO_L15P_2	J5	NC	
2	IO_L16N_2/VREF_2	J4	NC	
2	IO_L16P_2	J3	NC	
2	IO_L17N_2	K8	NC	
2	IO_L17P_2	K7	NC	
2	IO_L18N_2	H4	NC	
2	IO_L18P_2	H3	NC	
2	IO_L31N_2	H2		
2	IO_L31P_2	H1		
2	IO_L32N_2	M10		
2	IO_L32P_2	M9		

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Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
2	IO_L33N_2	K5		
2	IO_L33P_2	K4		
2	IO_L34N_2/VREF_2	J2		
2	IO_L34P_2	K2		
2	IO_L35N_2	L8		
2	IO_L35P_2	L7		
2	IO_L36N_2	L6		
2	IO_L36P_2	L5		
2	IO_L37N_2	K1		
2	IO_L37P_2	L1		
2	IO_L38N_2	N10		
2	IO_L38P_2	N9		
2	IO_L39N_2	M7		
2	IO_L39P_2	M6		
2	IO_L40N_2/VREF_2	L2		
2	IO_L40P_2	M2		
2	IO_L41N_2	N8		
2	IO_L41P_2	N7		
2	IO_L42N_2	L4		
2	IO_L42P_2	L3		
2	IO_L43N_2	M4		
2	IO_L43P_2	M3		
2	IO_L44N_2	P10		
2	IO_L44P_2	P9		
2	IO_L45N_2	N6		
2	IO_L45P_2	N5		
2	IO_L46N_2/VREF_2	M1		
2	IO_L46P_2	N1		
2	IO_L47N_2	P8		
2	IO_L47P_2	P7		
2	IO_L48N_2	N4		
2	IO_L48P_2	N3		
2	IO_L49N_2	N2		
2	IO_L49P_2	P2		
2	IO_L50N_2	R10		
2	IO_L50P_2	R9		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2VP20	No Connects XC2VP50
2	IO_L51N_2	P6		
2	IO_L51P_2	P5		
2	IO_L52N_2/VREF_2	P4		
2	IO_L52P_2	P3		
2	IO_L53N_2	T11		
2	IO_L53P_2	U11		
2	IO_L54N_2	R7		
2	IO_L54P_2	R6		
2	IO_L55N_2	P1		
2	IO_L55P_2	R1		
2	IO_L56N_2	T10		
2	IO_L56P_2	T9		
2	IO_L57N_2	R4		
2	IO_L57P_2	R3		
2	IO_L58N_2/VREF_2	R2		
2	IO_L58P_2	T2		
2	IO_L59N_2	T8		
2	IO_L59P_2	T7		
2	IO_L60N_2	T6		
2	IO_L60P_2	T5		
2	IO_L85N_2	T4		
2	IO_L85P_2	T3		
2	IO_L86N_2	U10		
2	IO_L86P_2	U9		
2	IO_L87N_2	U6		
2	IO_L87P_2	U5		
2	IO_L88N_2/VREF_2	U2		
2	IO_L88P_2	V2		
2	IO_L89N_2	U8		
2	IO_L89P_2	U7		
2	IO_L90N_2	U4		
2	IO_L90P_2	U3		
3	IO_L90N_3	V3		
3	IO_L90P_3	V4		
3	IO_L89N_3	V7		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2VP20	No Connects XC2VP50
3	IO_L89P_3	V8		
3	IO_L88N_3	V5		
3	IO_L88P_3	V6		
3	IO_L87N_3/VREF_3	W2		
3	IO_L87P_3	Y2		
3	IO_L86N_3	V9		
3	IO_L86P_3	V10		
3	IO_L85N_3	W3		
3	IO_L85P_3	W4		
3	IO_L60N_3	Y1		
3	IO_L60P_3	AA1		
3	IO_L59N_3	V11		
3	IO_L59P_3	W11		
3	IO_L58N_3	W5		
3	IO_L58P_3	W6		
3	IO_L57N_3/VREF_3	Y3		
3	IO_L57P_3	Y4		
3	IO_L56N_3	W7		
3	IO_L56P_3	W8		
3	IO_L55N_3	Y6		
3	IO_L55P_3	Y7		
3	IO_L54N_3	AA2		
3	IO_L54P_3	AB2		
3	IO_L53N_3	W9		
3	IO_L53P_3	W10		
3	IO_L52N_3	AA3		
3	IO_L52P_3	AA4		
3	IO_L51N_3/VREF_3	AB1		
3	IO_L51P_3	AC1		
3	IO_L50N_3	Y9		
3	IO_L50P_3	Y10		
3	IO_L49N_3	AA5		
3	IO_L49P_3	AA6		
3	IO_L48N_3	AB3		
3	IO_L48P_3	AB4		
3	IO_L47N_3	AA7		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
3	IO_L47P_3	AA8		
3	IO_L46N_3	AB5		
3	IO_L46P_3	AB6		
3	IO_L45N_3/VREF_3	AC2		
3	IO_L45P_3	AD2		
3	IO_L44N_3	AA9		
3	IO_L44P_3	AA10		
3	IO_L43N_3	AC3		
3	IO_L43P_3	AC4		
3	IO_L42N_3	AD1		
3	IO_L42P_3	AE1		
3	IO_L41N_3	AB7		
3	IO_L41P_3	AB8		
3	IO_L40N_3	AC6		
3	IO_L40P_3	AC7		
3	IO_L39N_3/VREF_3	AD3		
3	IO_L39P_3	AD4		
3	IO_L38N_3	AB9		
3	IO_L38P_3	AB10		
3	IO_L37N_3	AD5		
3	IO_L37P_3	AD6		
3	IO_L36N_3	AE2		
3	IO_L36P_3	AF2		
3	IO_L35N_3	AD7		
3	IO_L35P_3	AD8		
3	IO_L34N_3	AE4		
3	IO_L34P_3	AE5		
3	IO_L33N_3/VREF_3	AG1		
3	IO_L33P_3	AG2		
3	IO_L32N_3	AC9		
3	IO_L32P_3	AC10		
3	IO_L31N_3	AF3		
3	IO_L31P_3	AF4		
3	IO_L18N_3	AH1	NC	
3	IO_L18P_3	AH2	NC	
3	IO_L17N_3	AE7	NC	

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
3	IO_L17P_3	AE8	NC	
3	IO_L16N_3	AF5	NC	
3	IO_L16P_3	AF6	NC	
3	IO_L15N_3/VREF_3	AG3	NC	
3	IO_L15P_3	AG4	NC	
3	IO_L14N_3	AD9	NC	
3	IO_L14P_3	AD10	NC	
3	IO_L13N_3	AH3	NC	
3	IO_L13P_3	AH4	NC	
3	IO_L12N_3	AJ1	NC	
3	IO_L12P_3	AJ2	NC	
3	IO_L11N_3	AF7	NC	
3	IO_L11P_3	AF8	NC	
3	IO_L09N_3/VREF_3	AK1	NC	
3	IO_L09P_3	AK2	NC	
3	IO_L07N_3	AG5	NC	
3	IO_L07P_3	AG6	NC	
3	IO_L06N_3	AL1		
3	IO_L06P_3	AL2		
3	IO_L05N_3	AG7		
3	IO_L05P_3	AH8		
3	IO_L04N_3	AH5		
3	IO_L04P_3	AH6		
3	IO_L03N_3/VREF_3	AK3		
3	IO_L03P_3	AK4		
3	IO_L02N_3	AJ7		
3	IO_L02P_3	AJ8		
3	IO_L01N_3/VRP_3	AJ4		
3	IO_L01P_3/VRN_3	AJ5		
4	IO_L01N_4/DOUT	AL5		
4	IO_L01P_4/INIT_B	AL6		
4	IO_L02N_4/D0	AG9		
4	IO_L02P_4/D1	AH9		
4	IO_L03N_4/D2	AK6		
4	IO_L03P_4/D3	AK7		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
4	IO_L05_4/No_Pair	AF10		
4	IO_L06N_4/VRP_4	AL7		
4	IO_L06P_4/VRN_4	AM7		
4	IO_L07N_4	AE11		
4	IO_L07P_4/VREF_4	AF11		
4	IO_L08N_4	AG10		
4	IO_L08P_4	AH10		
4	IO_L09N_4	AK8		
4	IO_L09P_4/VREF_4	AL8		
4	IO_L19N_4	AE12	NC	
4	IO_L19P_4	AF12	NC	
4	IO_L20N_4	AJ9	NC	
4	IO_L20P_4	AK9	NC	
4	IO_L21N_4	AL9	NC	
4	IO_L21P_4	AM9	NC	
4	IO_L25N_4	AG11	NC	
4	IO_L25P_4	AH11	NC	
4	IO_L26N_4	AH12	NC	
4	IO_L26P_4	AJ12	NC	
4	IO_L27N_4	AK10	NC	
4	IO_L27P_4/VREF_4	AL10	NC	
4	IO_L37N_4	AE13		
4	IO_L37P_4	AF13		
4	IO_L38N_4	AG13		
4	IO_L38P_4	AH13		
4	IO_L39N_4	AJ11		
4	IO_L39P_4	AK11		
4	IO_L43N_4	AE14		
4	IO_L43P_4	AF14		
4	IO_L44N_4	AJ13		
4	IO_L44P_4	AK13		
4	IO_L45N_4	AL11		
4	IO_L45P_4/VREF_4	AM11		
4	IO_L46N_4	AE15		
4	IO_L46P_4	AF15		
4	IO_L47N_4	AG14		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2VP20	No Connects XC2VP50
4	IO_L47P_4	AH14		
4	IO_L48N_4	AL13		
4	IO_L48P_4	AL12		
4	IO_L49N_4	AD16		
4	IO_L49P_4	AE16		
4	IO_L50_4/No_Pair	AJ14		
4	IO_L53_4/No_Pair	AK14		
4	IO_L54N_4	AM14		
4	IO_L54P_4	AM13		
4	IO_L55N_4	AF16		
4	IO_L55P_4	AG16		
4	IO_L56N_4	AH15		
4	IO_L56P_4	AJ15		
4	IO_L57N_4	AL14		
4	IO_L57P_4/VREF_4	AL15		
4	IO_L67N_4	AD17		
4	IO_L67P_4	AE17		
4	IO_L68N_4	AH16		
4	IO_L68P_4	AJ16		
4	IO_L69N_4	AK16		
4	IO_L69P_4/VREF_4	AL16		
4	IO_L73N_4	AF17		
4	IO_L73P_4	AG17		
4	IO_L74N_4/GCLK3S	AH17		
4	IO_L74P_4/GCLK2P	AJ17		
4	IO_L75N_4/GCLK1S	AK17		
4	IO_L75P_4/GCLK0P	AL17		
5	IO_L75N_5/GCLK7S	AL18		
5	IO_L75P_5/GCLK6P	AK18		
5	IO_L74N_5/GCLK5S	AJ18		
5	IO_L74P_5/GCLK4P	AH18		
5	IO_L73N_5	AG18		
5	IO_L73P_5	AF18		
5	IO_L69N_5/VREF_5	AL19		
5	IO_L69P_5	AK19		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
5	IO_L68N_5	AJ19		
5	IO_L68P_5	AH19		
5	IO_L67N_5	AE18		
5	IO_L67P_5	AD18		
5	IO_L57N_5/VREF_5	AL20		
5	IO_L57P_5	AL21		
5	IO_L56N_5	AJ20		
5	IO_L56P_5	AH20		
5	IO_L55N_5	AG19		
5	IO_L55P_5	AF19		
5	IO_L54N_5	AM22		
5	IO_L54P_5	AM21		
5	IO_L53_5/No_Pair	AK21		
5	IO_L50_5/No_Pair	AJ21		
5	IO_L49N_5	AE19		
5	IO_L49P_5	AD19		
5	IO_L48N_5	AL23		
5	IO_L48P_5	AL22		
5	IO_L47N_5	AH21		
5	IO_L47P_5	AG21		
5	IO_L46N_5	AF20		
5	IO_L46P_5	AE20		
5	IO_L45N_5/VREF_5	AM24		
5	IO_L45P_5	AL24		
5	IO_L44N_5	AK22		
5	IO_L44P_5	AJ22		
5	IO_L43N_5	AF21		
5	IO_L43P_5	AE21		
5	IO_L39N_5	AK24		
5	IO_L39P_5	AJ24		
5	IO_L38N_5	AH22		
5	IO_L38P_5	AG22		
5	IO_L37N_5	AF22		
5	IO_L37P_5	AE22		
5	IO_L27N_5/VREF_5	AL25	NC	
5	IO_L27P_5	AK25	NC	

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Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
5	IO_L26N_5	AJ23	NC	
5	IO_L26P_5	AH23	NC	
5	IO_L25N_5	AH24	NC	
5	IO_L25P_5	AG24	NC	
5	IO_L21N_5	AM26	NC	
5	IO_L21P_5	AL26	NC	
5	IO_L20N_5	AK26	NC	
5	IO_L20P_5	AJ26	NC	
5	IO_L19N_5	AF23	NC	
5	IO_L19P_5	AE23	NC	
5	IO_L09N_5/VREF_5	AL27		
5	IO_L09P_5	AK27		
5	IO_L08N_5	AH25		
5	IO_L08P_5	AG25		
5	IO_L07N_5/VREF_5	AF24		
5	IO_L07P_5	AE24		
5	IO_L06N_5/VRP_5	AM28		
5	IO_L06P_5/VRN_5	AL28		
5	IO_L05_5/No_Pair	AF25		
5	IO_L03N_5/D4	AK28		
5	IO_L03P_5/D5	AK29		
5	IO_L02N_5/D6	AH26		
5	IO_L02P_5/D7	AG26		
5	IO_L01N_5/RDWR_B	AL29		
5	IO_L01P_5/CS_B	AL30		
6	IO_L01P_6/VRN_6	AJ30		
6	IO_L01N_6/VRP_6	AJ31		
6	IO_L02P_6	AJ27		
6	IO_L02N_6	AJ28		
6	IO_L03P_6	AK31		
6	IO_L03N_6/VREF_6	AK32		
6	IO_L04P_6	AH29		
6	IO_L04N_6	AH30		
6	IO_L05P_6	AH27		
6	IO_L05N_6	AG28		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
6	IO_L06P_6	AL33		
6	IO_L06N_6	AL34		
6	IO_L07P_6	AG29	NC	
6	IO_L07N_6	AG30	NC	
6	IO_L09P_6	AK33	NC	
6	IO_L09N_6/VREF_6	AK34	NC	
6	IO_L11P_6	AF27	NC	
6	IO_L11N_6	AF28	NC	
6	IO_L12P_6	AJ33	NC	
6	IO_L12N_6	AJ34	NC	
6	IO_L13P_6	AH31	NC	
6	IO_L13N_6	AH32	NC	
6	IO_L14P_6	AD25	NC	
6	IO_L14N_6	AD26	NC	
6	IO_L15P_6	AG31	NC	
6	IO_L15N_6/VREF_6	AG32	NC	
6	IO_L16P_6	AF29	NC	
6	IO_L16N_6	AF30	NC	
6	IO_L17P_6	AE27	NC	
6	IO_L17N_6	AE28	NC	
6	IO_L18P_6	AH33	NC	
6	IO_L18N_6	AH34	NC	
6	IO_L31P_6	AF31		
6	IO_L31N_6	AF32		
6	IO_L32P_6	AC25		
6	IO_L32N_6	AC26		
6	IO_L33P_6	AG33		
6	IO_L33N_6/VREF_6	AG34		
6	IO_L34P_6	AE30		
6	IO_L34N_6	AE31		
6	IO_L35P_6	AD27		
6	IO_L35N_6	AD28		
6	IO_L36P_6	AF33		
6	IO_L36N_6	AE33		
6	IO_L37P_6	AD29		
6	IO_L37N_6	AD30		

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
6	IO_L38P_6	AB25		
6	IO_L38N_6	AB26		
6	IO_L39P_6	AD31		
6	IO_L39N_6/VREF_6	AD32		
6	IO_L40P_6	AC28		
6	IO_L40N_6	AC29		
6	IO_L41P_6	AB27		
6	IO_L41N_6	AB28		
6	IO_L42P_6	AE34		
6	IO_L42N_6	AD34		
6	IO_L43P_6	AC31		
6	IO_L43N_6	AC32		
6	IO_L44P_6	AA25		
6	IO_L44N_6	AA26		
6	IO_L45P_6	AD33		
6	IO_L45N_6/VREF_6	AC33		
6	IO_L46P_6	AB29		
6	IO_L46N_6	AB30		
6	IO_L47P_6	AA27		
6	IO_L47N_6	AA28		
6	IO_L48P_6	AB31		
6	IO_L48N_6	AB32		
6	IO_L49P_6	AA29		
6	IO_L49N_6	AA30		
6	IO_L50P_6	Y25		
6	IO_L50N_6	Y26		
6	IO_L51P_6	AC34		
6	IO_L51N_6/VREF_6	AB34		
6	IO_L52P_6	AA31		
6	IO_L52N_6	AA32		
6	IO_L53P_6	W25		
6	IO_L53N_6	W26		
6	IO_L54P_6	AB33		
6	IO_L54N_6	AA33		
6	IO_L55P_6	Y28		
6	IO_L55N_6	Y29		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
6	IO_L56P_6	W27		
6	IO_L56N_6	W28		
6	IO_L57P_6	Y31		
6	IO_L57N_6/VREF_6	Y32		
6	IO_L58P_6	W29		
6	IO_L58N_6	W30		
6	IO_L59P_6	W24		
6	IO_L59N_6	V24		
6	IO_L60P_6	AA34		
6	IO_L60N_6	Y34		
6	IO_L85P_6	W31		
6	IO_L85N_6	W32		
6	IO_L86P_6	V25		
6	IO_L86N_6	V26		
6	IO_L87P_6	Y33		
6	IO_L87N_6/VREF_6	W33		
6	IO_L88P_6	V29		
6	IO_L88N_6	V30		
6	IO_L89P_6	V27		
6	IO_L89N_6	V28		
6	IO_L90P_6	V31		
6	IO_L90N_6	V32		
7	IO_L90P_7	U32		
7	IO_L90N_7	U31		
7	IO_L89P_7	U28		
7	IO_L89N_7	U27		
7	IO_L88P_7	V33		
7	IO_L88N_7/VREF_7	U33		
7	IO_L87P_7	U30		
7	IO_L87N_7	U29		
7	IO_L86P_7	U26		
7	IO_L86N_7	U25		
7	IO_L85P_7	T32		
7	IO_L85N_7	T31		
7	IO_L60P_7	T30		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
7	IO_L60N_7	T29		
7	IO_L59P_7	T28		
7	IO_L59N_7	T27		
7	IO_L58P_7	T33		
7	IO_L58N_7/VREF_7	R33		
7	IO_L57P_7	R32		
7	IO_L57N_7	R31		
7	IO_L56P_7	T26		
7	IO_L56N_7	T25		
7	IO_L55P_7	R34		
7	IO_L55N_7	P34		
7	IO_L54P_7	R29		
7	IO_L54N_7	R28		
7	IO_L53P_7	U24		
7	IO_L53N_7	T24		
7	IO_L52P_7	P32		
7	IO_L52N_7/VREF_7	P31		
7	IO_L51P_7	P30		
7	IO_L51N_7	P29		
7	IO_L50P_7	R26		
7	IO_L50N_7	R25		
7	IO_L49P_7	P33		
7	IO_L49N_7	N33		
7	IO_L48P_7	N32		
7	IO_L48N_7	N31		
7	IO_L47P_7	P28		
7	IO_L47N_7	P27		
7	IO_L46P_7	N34		
7	IO_L46N_7/VREF_7	M34		
7	IO_L45P_7	N30		
7	IO_L45N_7	N29		
7	IO_L44P_7	P26		
7	IO_L44N_7	P25		
7	IO_L43P_7	M32		
7	IO_L43N_7	M31		
7	IO_L42P_7	L32		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
7	IO_L42N_7	L31		
7	IO_L41P_7	N28		
7	IO_L41N_7	N27		
7	IO_L40P_7	M33		
7	IO_L40N_7/VREF_7	L33		
7	IO_L39P_7	M29		
7	IO_L39N_7	M28		
7	IO_L38P_7	N26		
7	IO_L38N_7	N25		
7	IO_L37P_7	L34		
7	IO_L37N_7	K34		
7	IO_L36P_7	L30		
7	IO_L36N_7	L29		
7	IO_L35P_7	L28		
7	IO_L35N_7	L27		
7	IO_L34P_7	K33		
7	IO_L34N_7/VREF_7	J33		
7	IO_L33P_7	K31		
7	IO_L33N_7	K30		
7	IO_L32P_7	M26		
7	IO_L32N_7	M25		
7	IO_L31P_7	H34		
7	IO_L31N_7	H33		
7	IO_L18P_7	H32	NC	
7	IO_L18N_7	H31	NC	
7	IO_L17P_7	K28	NC	
7	IO_L17N_7	K27	NC	
7	IO_L16P_7	J32	NC	
7	IO_L16N_7/VREF_7	J31	NC	
7	IO_L15P_7	J30	NC	
7	IO_L15N_7	J29	NC	
7	IO_L13P_7	G34	NC	
7	IO_L13N_7	G33	NC	
7	IO_L12P_7	H30	NC	
7	IO_L12N_7	H29	NC	
7	IO_L11P_7	L26	NC	

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
7	IO_L11N_7	L25	NC	
7	IO_L10P_7	F34	NC	
7	IO_L10N_7/VREF_7	F33	NC	
7	IO_L09P_7	G30	NC	
7	IO_L09N_7	G29	NC	
7	IO_L07P_7	G32	NC	
7	IO_L07N_7	G31	NC	
7	IO_L06P_7	F31		
7	IO_L06N_7	F30		
7	IO_L05P_7	J28		
7	IO_L05N_7	J27		
7	IO_L04P_7	E34		
7	IO_L04N_7/VREF_7	E33		
7	IO_L03P_7	E32		
7	IO_L03N_7	E31		
7	IO_L02P_7	F28		
7	IO_L02N_7	F27		
7	IO_L01P_7/VRN_7	D34		
7	IO_L01N_7/VRP_7	D33		
0	VCCO_0	C29		
0	VCCO_0	E20		
0	VCCO_0	F25		
0	VCCO_0	L20		
0	VCCO_0	L21		
0	VCCO_0	L22		
0	VCCO_0	L23		
0	VCCO_0	M18		
0	VCCO_0	M19		
0	VCCO_0	M20		
0	VCCO_0	M21		
0	VCCO_0	M22		
1	VCCO_1	C6		
1	VCCO_1	E15		
1	VCCO_1	F10		
1	VCCO_1	L12		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
1	VCCO_1	L13		
1	VCCO_1	L14		
1	VCCO_1	L15		
1	VCCO_1	M13		
1	VCCO_1	M14		
1	VCCO_1	M15		
1	VCCO_1	M16		
1	VCCO_1	M17		
2	VCCO_2	F3		
2	VCCO_2	K6		
2	VCCO_2	M11		
2	VCCO_2	N11		
2	VCCO_2	N12		
2	VCCO_2	P11		
2	VCCO_2	P12		
2	VCCO_2	R5		
2	VCCO_2	R11		
2	VCCO_2	R12		
2	VCCO_2	T12		
2	VCCO_2	U12		
3	VCCO_3	V12		
3	VCCO_3	W12		
3	VCCO_3	Y5		
3	VCCO_3	Y11		
3	VCCO_3	Y12		
3	VCCO_3	AA11		
3	VCCO_3	AA12		
3	VCCO_3	AB11		
3	VCCO_3	AB12		
3	VCCO_3	AC11		
3	VCCO_3	AE6		
3	VCCO_3	AJ3		
4	VCCO_4	AC13		
4	VCCO_4	AC14		
4	VCCO_4	AC15		
4	VCCO_4	AC16		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
4	VCCO_4	AC17		
4	VCCO_4	AD12		
4	VCCO_4	AD13		
4	VCCO_4	AD14		
4	VCCO_4	AD15		
4	VCCO_4	AJ10		
4	VCCO_4	AK15		
4	VCCO_4	AM6		
5	VCCO_5	AC18		
5	VCCO_5	AC19		
5	VCCO_5	AC20		
5	VCCO_5	AC21		
5	VCCO_5	AC22		
5	VCCO_5	AD20		
5	VCCO_5	AD21		
5	VCCO_5	AD22		
5	VCCO_5	AD23		
5	VCCO_5	AJ25		
5	VCCO_5	AK20		
5	VCCO_5	AM29		
6	VCCO_6	V23		
6	VCCO_6	W23		
6	VCCO_6	Y23		
6	VCCO_6	Y24		
6	VCCO_6	Y30		
6	VCCO_6	AA23		
6	VCCO_6	AA24		
6	VCCO_6	AB23		
6	VCCO_6	AB24		
6	VCCO_6	AC24		
6	VCCO_6	AE29		
6	VCCO_6	AJ32		
7	VCCO_7	F32		
7	VCCO_7	K29		
7	VCCO_7	M24		
7	VCCO_7	N23		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
7	VCCO_7	N24		
7	VCCO_7	P23		
7	VCCO_7	P24		
7	VCCO_7	R23		
7	VCCO_7	R24		
7	VCCO_7	R30		
7	VCCO_7	T23		
7	VCCO_7	U23		
N/A	CCLK	AE9		
N/A	PROG_B	J26		
N/A	DONE	AE10		
N/A	M0	AF26		
N/A	M1	AE26		
N/A	M2	AE25		
N/A	TCK	J9		
N/A	TDI	H28		
N/A	TDO	H7		
N/A	TMS	K10		
N/A	PWRDWN_B	AF9		
N/A	HSWAP_EN	K25		
N/A	RSVD	G8		
N/A	VBATT	K9		
N/A	DXP	K26		
N/A	DXN	G27		
N/A	AVCCAUXTX2	B32	NC	
N/A	VTTXPAD2	B33	NC	
N/A	TXNPAD2	A33	NC	
N/A	TXPPAD2	A32	NC	
N/A	GNDA2	C30	NC	
N/A	GNDA2	C30	NC	
N/A	RXPPAD2	A31	NC	
N/A	RXNPAD2	A30	NC	
N/A	VTRXPAD2	B31	NC	
N/A	AVCCAUXRX2	B30	NC	
N/A	AVCCAUXTX4	B28		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	VTTXPAD4	B29		
N/A	TXNPAD4	A29		
N/A	TXPPAD4	A28		
N/A	GNDA4	C27		
N/A	GNDA4	C27		
N/A	RXPPAD4	A27		
N/A	RXNPAD4	A26		
N/A	VTRXPAD4	B27		
N/A	AVCCAUXRX4	B26		
N/A	AVCCAUXTX5	B24	NC	
N/A	VTTXPAD5	B25	NC	
N/A	TXNPAD5	A25	NC	
N/A	TXPPAD5	A24	NC	
N/A	GNDA5	C23	NC	
N/A	GNDA5	C23	NC	
N/A	RXPPAD5	A23	NC	
N/A	RXNPAD5	A22	NC	
N/A	VTRXPAD5	B23	NC	
N/A	AVCCAUXRX5	B22	NC	
N/A	AVCCAUXTX6	B20		
N/A	VTTXPAD6	B21		
N/A	TXNPAD6	A21		
N/A	TXPPAD6	A20		
N/A	GNDA6	C20		
N/A	GNDA6	C20		
N/A	RXPPAD6	A19		
N/A	RXNPAD6	A18		
N/A	VTRXPAD6	B19		
N/A	AVCCAUXRX6	B18		
N/A	AVCCAUXTX7	B16		
N/A	VTTXPAD7	B17		
N/A	TXNPAD7	A17		
N/A	TXPPAD7	A16		
N/A	GNDA7	C15		
N/A	GNDA7	C15		
N/A	RXPPAD7	A15		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	RXNPAD7	A14		
N/A	VTRXPAD7	B15		
N/A	AVCCAUXRX7	B14		
N/A	AVCCAUXTX8	B12	NC	
N/A	VTTXPAD8	B13	NC	
N/A	TXNPAD8	A13	NC	
N/A	TXPPAD8	A12	NC	
N/A	GNDA8	C12	NC	
N/A	GNDA8	C12	NC	
N/A	RXPPAD8	A11	NC	
N/A	RXNPAD8	A10	NC	
N/A	VTRXPAD8	B11	NC	
N/A	AVCCAUXRX8	B10	NC	
N/A	AVCCAUXTX9	B8		
N/A	VTTXPAD9	B9		
N/A	TXNPAD9	A9		
N/A	TXPPAD9	A8		
N/A	GNDA9	C8		
N/A	GNDA9	C8		
N/A	RXPPAD9	A7		
N/A	RXNPAD9	A6		
N/A	VTRXPAD9	B7		
N/A	AVCCAUXRX9	B6		
N/A	AVCCAUXTX11	B4	NC	
N/A	VTTXPAD11	B5	NC	
N/A	TXNPAD11	A5	NC	
N/A	TXPPAD11	A4	NC	
N/A	GNDA11	C5	NC	
N/A	GNDA11	C5	NC	
N/A	RXPPAD11	A3	NC	
N/A	RXNPAD11	A2	NC	
N/A	VTRXPAD11	B3	NC	
N/A	AVCCAUXRX11	B2	NC	
N/A	AVCCAUXRX14	AN2	NC	
N/A	VTRXPAD14	AN3	NC	
N/A	RXNPAD14	AP2	NC	

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
N/A	RXPPAD14	AP3	NC	
N/A	GNDA14	AM5	NC	
N/A	GNDA14	AM5	NC	
N/A	TXPPAD14	AP4	NC	
N/A	TXNPAD14	AP5	NC	
N/A	VTTXPAD14	AN5	NC	
N/A	AVCCAUXTX14	AN4	NC	
N/A	AVCCAUXRX16	AN6		
N/A	VTRXPAD16	AN7		
N/A	RXNPAD16	AP6		
N/A	RXPPAD16	AP7		
N/A	GNDA16	AM8		
N/A	GNDA16	AM8		
N/A	TXPPAD16	AP8		
N/A	TXNPAD16	AP9		
N/A	VTTXPAD16	AN9		
N/A	AVCCAUXTX16	AN8		
N/A	AVCCAUXRX17	AN10	NC	
N/A	VTRXPAD17	AN11	NC	
N/A	RXNPAD17	AP10	NC	
N/A	RXPPAD17	AP11	NC	
N/A	GNDA17	AM12	NC	
N/A	GNDA17	AM12	NC	
N/A	TXPPAD17	AP12	NC	
N/A	TXNPAD17	AP13	NC	
N/A	VTTXPAD17	AN13	NC	
N/A	AVCCAUXTX17	AN12	NC	
N/A	AVCCAUXRX18	AN14		
N/A	VTRXPAD18	AN15		
N/A	RXNPAD18	AP14		
N/A	RXPPAD18	AP15		
N/A	GNDA18	AM15		
N/A	GNDA18	AM15		
N/A	TXPPAD18	AP16		
N/A	TXNPAD18	AP17		
N/A	VTTXPAD18	AN17		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
N/A	AVCCAUXTX18	AN16		
N/A	AVCCAUXRX19	AN18		
N/A	VTRXPAD19	AN19		
N/A	RXNPAD19	AP18		
N/A	RXPPAD19	AP19		
N/A	GNDA19	AM20		
N/A	GNDA19	AM20		
N/A	TXPPAD19	AP20		
N/A	TXNPAD19	AP21		
N/A	VTTXPAD19	AN21		
N/A	AVCCAUXTX19	AN20		
N/A	AVCCAUXRX20	AN22	NC	
N/A	VTRXPAD20	AN23	NC	
N/A	RXNPAD20	AP22	NC	
N/A	RXPPAD20	AP23	NC	
N/A	GNDA20	AM23	NC	
N/A	GNDA20	AM23	NC	
N/A	TXPPAD20	AP24	NC	
N/A	TXNPAD20	AP25	NC	
N/A	VTTXPAD20	AN25	NC	
N/A	AVCCAUXTX20	AN24	NC	
N/A	AVCCAUXRX21	AN26		
N/A	VTRXPAD21	AN27		
N/A	RXNPAD21	AP26		
N/A	RXPPAD21	AP27		
N/A	GNDA21	AM27		
N/A	GNDA21	AM27		
N/A	TXPPAD21	AP28		
N/A	TXNPAD21	AP29		
N/A	VTTXPAD21	AN29		
N/A	AVCCAUXTX21	AN28		
N/A	AVCCAUXRX23	AN30	NC	
N/A	VTRXPAD23	AN31	NC	
N/A	RXNPAD23	AP30	NC	
N/A	RXPPAD23	AP31	NC	
N/A	GNDA23	AM30	NC	

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	GNDA23	AM30	NC	
N/A	TXPPAD23	AP32	NC	
N/A	TXNPAD23	AP33	NC	
N/A	VTTXPAD23	AN33	NC	
N/A	AVCCAUXTX23	AN32	NC	
N/A	VCCINT	L11		
N/A	VCCINT	L24		
N/A	VCCINT	M12		
N/A	VCCINT	M23		
N/A	VCCINT	N13		
N/A	VCCINT	N14		
N/A	VCCINT	N15		
N/A	VCCINT	N16		
N/A	VCCINT	N17		
N/A	VCCINT	N18		
N/A	VCCINT	N19		
N/A	VCCINT	N20		
N/A	VCCINT	N21		
N/A	VCCINT	N22		
N/A	VCCINT	P13		
N/A	VCCINT	P22		
N/A	VCCINT	R13		
N/A	VCCINT	R22		
N/A	VCCINT	T13		
N/A	VCCINT	T22		
N/A	VCCINT	U13		
N/A	VCCINT	U22		
N/A	VCCINT	V13		
N/A	VCCINT	V22		
N/A	VCCINT	W13		
N/A	VCCINT	W22		
N/A	VCCINT	Y13		
N/A	VCCINT	Y22		
N/A	VCCINT	AA13		
N/A	VCCINT	AA22		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	VCCINT	AB13		
N/A	VCCINT	AB14		
N/A	VCCINT	AB15		
N/A	VCCINT	AB16		
N/A	VCCINT	AB17		
N/A	VCCINT	AB18		
N/A	VCCINT	AB19		
N/A	VCCINT	AB20		
N/A	VCCINT	AB21		
N/A	VCCINT	AB22		
N/A	VCCINT	AC12		
N/A	VCCINT	AC23		
N/A	VCCINT	AD11		
N/A	VCCINT	AD24		
N/A	VCCAUX	C3		
N/A	VCCAUX	C4		
N/A	VCCAUX	C17		
N/A	VCCAUX	C18		
N/A	VCCAUX	C31		
N/A	VCCAUX	C32		
N/A	VCCAUX	D3		
N/A	VCCAUX	D32		
N/A	VCCAUX	U1		
N/A	VCCAUX	V1		
N/A	VCCAUX	U34		
N/A	VCCAUX	V34		
N/A	VCCAUX	AL3		
N/A	VCCAUX	AL32		
N/A	VCCAUX	AM3		
N/A	VCCAUX	AM4		
N/A	VCCAUX	AM17		
N/A	VCCAUX	AM18		
N/A	VCCAUX	AM31		
N/A	VCCAUX	AM32		
N/A	GND	AF34		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	**XC2V P50**
N/A	GND	B34		
N/A	GND	C1		
N/A	GND	C2		
N/A	GND	C10		
N/A	GND	C16		
N/A	GND	C19		
N/A	GND	C25		
N/A	GND	C33		
N/A	GND	C34		
N/A	GND	D4		
N/A	GND	D31		
N/A	GND	E5		
N/A	GND	E12		
N/A	GND	E23		
N/A	GND	E30		
N/A	GND	F6		
N/A	GND	F29		
N/A	GND	G7		
N/A	GND	G28		
N/A	GND	B1		
N/A	GND	H8		
N/A	GND	H12		
N/A	GND	H15		
N/A	GND	H20		
N/A	GND	J1		
N/A	GND	H27		
N/A	GND	AF1		
N/A	GND	K3		
N/A	GND	K32		
N/A	GND	M5		
N/A	GND	M8		
N/A	GND	M27		
N/A	GND	M30		
N/A	GND	P14		
N/A	GND	P15		
N/A	GND	P16		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
N/A	GND	P17		
N/A	GND	P18		
N/A	GND	P19		
N/A	GND	P20		
N/A	GND	P21		
N/A	GND	R8		
N/A	GND	R14		
N/A	GND	R15		
N/A	GND	R16		
N/A	GND	R17		
N/A	GND	R18		
N/A	GND	R19		
N/A	GND	R20		
N/A	GND	R21		
N/A	GND	R27		
N/A	GND	T1		
N/A	GND	T14		
N/A	GND	T15		
N/A	GND	T16		
N/A	GND	T17		
N/A	GND	T18		
N/A	GND	T19		
N/A	GND	T20		
N/A	GND	T21		
N/A	GND	T34		
N/A	GND	U14		
N/A	GND	U15		
N/A	GND	U16		
N/A	GND	U17		
N/A	GND	U18		
N/A	GND	U19		
N/A	GND	U20		
N/A	GND	U21		
N/A	GND	V14		
N/A	GND	V15		
N/A	GND	V16		

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Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	GND	V17		
N/A	GND	V18		
N/A	GND	V19		
N/A	GND	V20		
N/A	GND	V21		
N/A	GND	W1		
N/A	GND	W14		
N/A	GND	W15		
N/A	GND	W16		
N/A	GND	W17		
N/A	GND	W18		
N/A	GND	W19		
N/A	GND	W20		
N/A	GND	W21		
N/A	GND	W34		
N/A	GND	Y8		
N/A	GND	Y14		
N/A	GND	Y15		
N/A	GND	Y16		
N/A	GND	Y17		
N/A	GND	Y18		
N/A	GND	Y19		
N/A	GND	Y20		
N/A	GND	Y21		
N/A	GND	Y27		
N/A	GND	AA14		
N/A	GND	AA15		
N/A	GND	AA16		
N/A	GND	AA17		
N/A	GND	AA18		
N/A	GND	AA19		
N/A	GND	AA20		
N/A	GND	AA21		
N/A	GND	AC5		
N/A	GND	AC8		
N/A	GND	AC27		

Table 10: **FF1152 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
N/A	GND	AC30		
N/A	GND	AE3		
N/A	GND	AE32		
N/A	GND	H23		
N/A	GND	AG8		
N/A	GND	AG12		
N/A	GND	AG15		
N/A	GND	AG20		
N/A	GND	AG23		
N/A	GND	AG27		
N/A	GND	J34		
N/A	GND	AH7		
N/A	GND	AH28		
N/A	GND	AJ6		
N/A	GND	AJ29		
N/A	GND	AK5		
N/A	GND	AK12		
N/A	GND	AK23		
N/A	GND	AK30		
N/A	GND	AL4		
N/A	GND	AL31		
N/A	GND	AM1		
N/A	GND	AM2		
N/A	GND	AM10		
N/A	GND	AM16		
N/A	GND	AM19		
N/A	GND	AM25		
N/A	GND	AM33		
N/A	GND	AM34		
N/A	GND	AN1		
N/A	GND	AN34		

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FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)
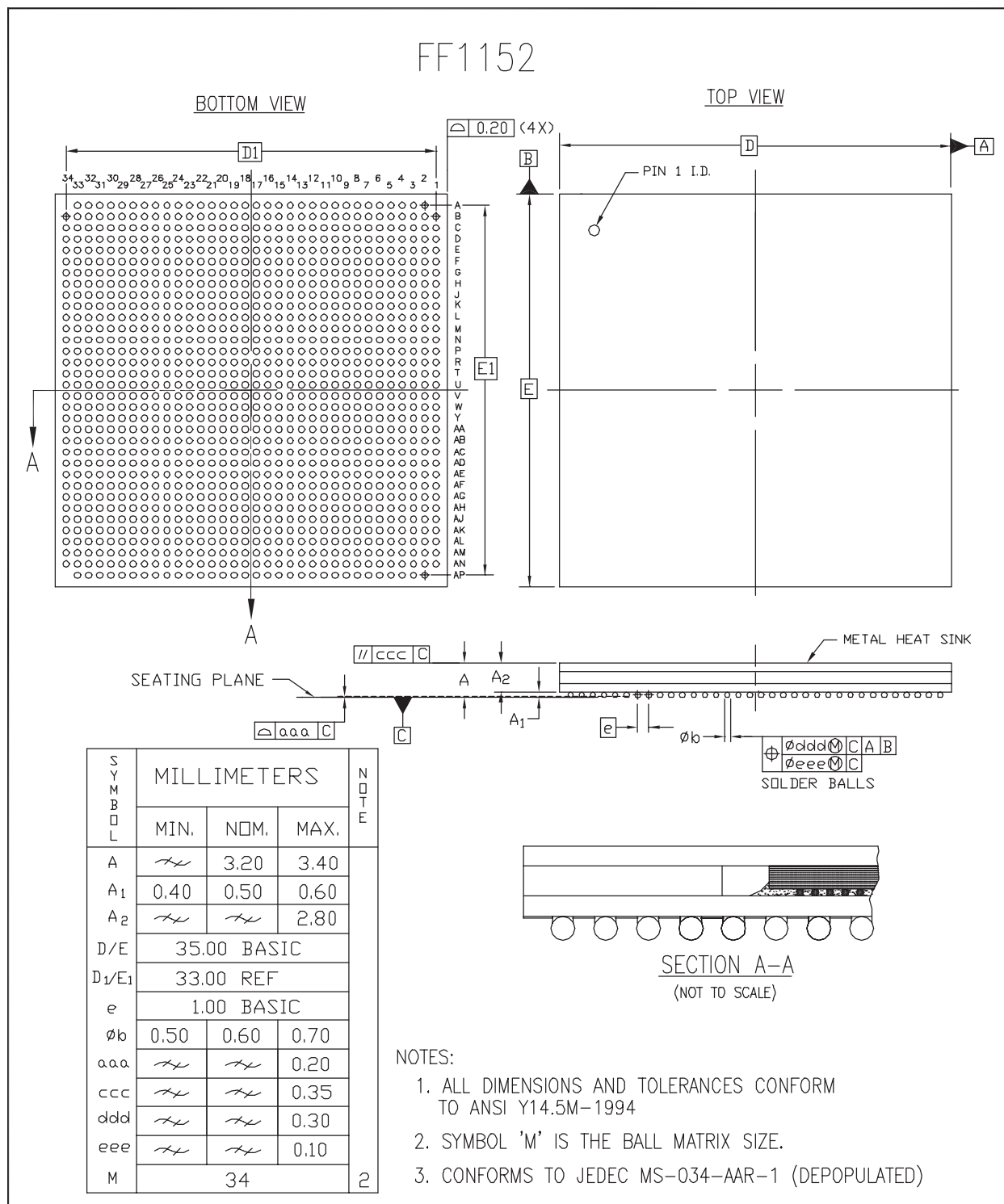
Figure 5: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, the XC2VP50 Virtex-II Pro device is available in the FF1517 flip-chip fine-pitch BGA package. Following this table are the **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)**.

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
0	IO_L01N_0/VRP_0	F32
0	IO_L01P_0/VRN_0	E32
0	IO_L02N_0	K29
0	IO_L02P_0	J29
0	IO_L03N_0	K28
0	IO_L03P_0/VREF_0	K27
0	IO_L05_0/No_Pair	H30
0	IO_L06N_0	H29
0	IO_L06P_0	G29
0	IO_L07N_0	G31
0	IO_L07P_0	F31
0	IO_L08N_0	D32
0	IO_L08P_0	C32
0	IO_L09N_0	J28
0	IO_L09P_0/VREF_0	H28
0	IO_L19N_0	G30
0	IO_L19P_0	F30
0	IO_L20N_0	E31
0	IO_L20P_0	D31
0	IO_L21N_0	J27
0	IO_L21P_0	H27
0	IO_L25N_0	F29
0	IO_L25P_0	E29
0	IO_L26N_0	E30
0	IO_L26P_0	D30
0	IO_L27N_0	K26
0	IO_L27P_0/VREF_0	J26
0	IO_L37N_0	G28
0	IO_L37P_0	F28
0	IO_L38N_0	D29
0	IO_L38P_0	C29
0	IO_L39N_0	K25
0	IO_L39P_0	J25
0	IO_L43N_0	G27
0	IO_L43P_0	F27

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
0	IO_L44N_0	D28
0	IO_L44P_0	C28
0	IO_L45N_0	L24
0	IO_L45P_0/VREF_0	K24
0	IO_L46N_0	H26
0	IO_L46P_0	G26
0	IO_L47N_0	E27
0	IO_L47P_0	D27
0	IO_L48N_0	H25
0	IO_L48P_0	G25
0	IO_L49N_0	F25
0	IO_L49P_0	E25
0	IO_L50_0/No_Pair	E26
0	IO_L53_0/No_Pair	D26
0	IO_L54N_0	J24
0	IO_L54P_0	H24
0	IO_L55N_0	G24
0	IO_L55P_0	F24
0	IO_L56N_0	D25
0	IO_L56P_0	C25
0	IO_L57N_0	K23
0	IO_L57P_0/VREF_0	J23
0	IO_L58N_0	G23
0	IO_L58P_0	F23
0	IO_L59N_0	E24
0	IO_L59P_0	D24
0	IO_L60N_0	K22
0	IO_L60P_0	J22
0	IO_L64N_0	H22
0	IO_L64P_0	G22
0	IO_L65N_0	D23
0	IO_L65P_0	C23
0	IO_L66N_0	K21
0	IO_L66P_0/VREF_0	J21
0	IO_L67N_0	F22
0	IO_L67P_0	E22
0	IO_L68N_0	D22
0	IO_L68P_0	C22

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
0	IO_L69N_0	H21
0	IO_L69P_0/VREF_0	G21
0	IO_L73N_0	F21
0	IO_L73P_0	E21
0	IO_L74N_0/GCLK7P	D21
0	IO_L74P_0/GCLK6S	C21
0	IO_L75N_0/GCLK5P	F20
0	IO_L75P_0/GCLK4S	E20
1	IO_L75N_1/GCLK3P	H20
1	IO_L75P_1/GCLK2S	J20
1	IO_L74N_1/GCLK1P	C19
1	IO_L74P_1/GCLK0S	D19
1	IO_L73N_1	E19
1	IO_L73P_1	F19
1	IO_L69N_1/VREF_1	G19
1	IO_L69P_1	H19
1	IO_L68N_1	C18
1	IO_L68P_1	D18
1	IO_L67N_1	E18
1	IO_L67P_1	F18
1	IO_L66N_1/VREF_1	J19
1	IO_L66P_1	K19
1	IO_L65N_1	C17
1	IO_L65P_1	D17
1	IO_L64N_1	G18
1	IO_L64P_1	H18
1	IO_L60N_1	J18
1	IO_L60P_1	K18
1	IO_L59N_1	D16
1	IO_L59P_1	E16
1	IO_L58N_1	F17
1	IO_L58P_1	G17
1	IO_L57N_1/VREF_1	J17
1	IO_L57P_1	K17
1	IO_L56N_1	C15
1	IO_L56P_1	D15
1	IO_L55N_1	F16

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
1	IO_L55P_1	G16
1	IO_L54N_1	H16
1	IO_L54P_1	J16
1	IO_L53_1/No_Pair	D14
1	IO_L50_1/No_Pair	E14
1	IO_L49N_1	E15
1	IO_L49P_1	F15
1	IO_L48N_1	G15
1	IO_L48P_1	H15
1	IO_L47N_1	D13
1	IO_L47P_1	E13
1	IO_L46N_1	G14
1	IO_L46P_1	H14
1	IO_L45N_1/VREF_1	K16
1	IO_L45P_1	L16
1	IO_L44N_1	C12
1	IO_L44P_1	D12
1	IO_L43N_1	F13
1	IO_L43P_1	G13
1	IO_L39N_1	J15
1	IO_L39P_1	K15
1	IO_L38N_1	C11
1	IO_L38P_1	D11
1	IO_L37N_1	F12
1	IO_L37P_1	G12
1	IO_L27N_1/VREF_1	J14
1	IO_L27P_1	K14
1	IO_L26N_1	D10
1	IO_L26P_1	E10
1	IO_L25N_1	E11
1	IO_L25P_1	F11
1	IO_L21N_1	H13
1	IO_L21P_1	J13
1	IO_L20N_1	D9
1	IO_L20P_1	E9
1	IO_L19N_1	F10
1	IO_L19P_1	G10
1	IO_L09N_1/VREF_1	H12

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
1	IO_L09P_1	J12
1	IO_L08N_1	C8
1	IO_L08P_1	D8
1	IO_L07N_1	F9
1	IO_L07P_1	G9
1	IO_L06N_1	G11
1	IO_L06P_1	H11
1	IO_L05_1/No_Pair	H10
1	IO_L03N_1/VREF_1	K13
1	IO_L03P_1	K12
1	IO_L02N_1	J11
1	IO_L02P_1	K11
1	IO_L01N_1/VRP_1	E8
1	IO_L01P_1/VRN_1	F8
2	IO_L01N_2/VRP_2	E4
2	IO_L01P_2/VRN_2	E3
2	IO_L02N_2	G8
2	IO_L02P_2	H7
2	IO_L03N_2	C5
2	IO_L03P_2	D5
2	IO_L04N_2/VREF_2	D2
2	IO_L04P_2	D1
2	IO_L05N_2	J8
2	IO_L05P_2	J7
2	IO_L06N_2	E6
2	IO_L06P_2	F5
2	IO_L07N_2	E2
2	IO_L07P_2	E1
2	IO_L08N_2	K9
2	IO_L08P_2	K8
2	IO_L09N_2	G6
2	IO_L09P_2	G5
2	IO_L10N_2/VREF_2	G4
2	IO_L10P_2	G3
2	IO_L11N_2	N12
2	IO_L11P_2	N11
2	IO_L12N_2	F4

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
2	IO_L12P_2	F3
2	IO_L13N_2	F2
2	IO_L13P_2	F1
2	IO_L14N_2	L8
2	IO_L14P_2	L7
2	IO_L15N_2	H6
2	IO_L15P_2	H5
2	IO_L16N_2/VREF_2	H4
2	IO_L16P_2	H3
2	IO_L17N_2	P12
2	IO_L17P_2	P11
2	IO_L18N_2	J6
2	IO_L18P_2	J5
2	IO_L19N_2	G2
2	IO_L19P_2	G1
2	IO_L20N_2	N10
2	IO_L20P_2	N9
2	IO_L21N_2	K7
2	IO_L21P_2	K6
2	IO_L22N_2/VREF_2	H2
2	IO_L22P_2	H1
2	IO_L23N_2	R12
2	IO_L23P_2	R11
2	IO_L24N_2	J4
2	IO_L24P_2	J3
2	IO_L25N_2	J2
2	IO_L25P_2	J1
2	IO_L26N_2	P10
2	IO_L26P_2	P9
2	IO_L27N_2	K5
2	IO_L27P_2	K4
2	IO_L28N_2/VREF_2	K2
2	IO_L28P_2	K1
2	IO_L29N_2	P8
2	IO_L29P_2	P7
2	IO_L30N_2	L6
2	IO_L30P_2	L5
2	IO_L31N_2	L3

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
2	IO_L31P_2	L2
2	IO_L32N_2	R10
2	IO_L32P_2	R9
2	IO_L33N_2	N8
2	IO_L33P_2	N7
2	IO_L34N_2/VREF_2	M4
2	IO_L34P_2	M3
2	IO_L35N_2	T12
2	IO_L35P_2	T11
2	IO_L36N_2	M6
2	IO_L36P_2	M5
2	IO_L37N_2	M2
2	IO_L37P_2	M1
2	IO_L38N_2	T10
2	IO_L38P_2	T9
2	IO_L39N_2	N6
2	IO_L39P_2	N5
2	IO_L40N_2/VREF_2	N4
2	IO_L40P_2	N3
2	IO_L41N_2	U12
2	IO_L41P_2	U11
2	IO_L42N_2	P5
2	IO_L42P_2	P4
2	IO_L43N_2	N2
2	IO_L43P_2	N1
2	IO_L44N_2	T8
2	IO_L44P_2	T7
2	IO_L45N_2	R7
2	IO_L45P_2	R6
2	IO_L46N_2/VREF_2	P2
2	IO_L46P_2	P1
2	IO_L47N_2	U10
2	IO_L47P_2	U9
2	IO_L48N_2	R5
2	IO_L48P_2	R4
2	IO_L49N_2	R3
2	IO_L49P_2	R2
2	IO_L50N_2	V12

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
2	IO_L50P_2	V11
2	IO_L51N_2	T6
2	IO_L51P_2	T5
2	IO_L52N_2/VREF_2	T2
2	IO_L52P_2	T1
2	IO_L53N_2	V10
2	IO_L53P_2	V9
2	IO_L54N_2	T4
2	IO_L54P_2	T3
2	IO_L55N_2	U4
2	IO_L55P_2	U3
2	IO_L56N_2	V8
2	IO_L56P_2	V7
2	IO_L57N_2	U7
2	IO_L57P_2	U6
2	IO_L58N_2/VREF_2	U2
2	IO_L58P_2	U1
2	IO_L59N_2	W12
2	IO_L59P_2	W11
2	IO_L60N_2	V6
2	IO_L60P_2	V5
2	IO_L85N_2	V4
2	IO_L85P_2	V3
2	IO_L86N_2	W10
2	IO_L86P_2	W9
2	IO_L87N_2	W6
2	IO_L87P_2	W5
2	IO_L88N_2/VREF_2	V2
2	IO_L88P_2	V1
2	IO_L89N_2	W8
2	IO_L89P_2	W7
2	IO_L90N_2	W4
2	IO_L90P_2	W3
3	IO_L90N_3	AA3
3	IO_L90P_3	AA4
3	IO_L89N_3	AA7
3	IO_L89P_3	AA8

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
3	IO_L88N_3	AA5
3	IO_L88P_3	AA6
3	IO_L87N_3/VREF_3	AB1
3	IO_L87P_3	AB2
3	IO_L86N_3	AA9
3	IO_L86P_3	AA10
3	IO_L85N_3	AB3
3	IO_L85P_3	AB4
3	IO_L60N_3	AC1
3	IO_L60P_3	AC2
3	IO_L59N_3	AA11
3	IO_L59P_3	AA12
3	IO_L58N_3	AB5
3	IO_L58P_3	AB6
3	IO_L57N_3/VREF_3	AC3
3	IO_L57P_3	AC4
3	IO_L56N_3	AB7
3	IO_L56P_3	AB8
3	IO_L55N_3	AC6
3	IO_L55P_3	AC7
3	IO_L54N_3	AD1
3	IO_L54P_3	AD2
3	IO_L53N_3	AB9
3	IO_L53P_3	AB10
3	IO_L52N_3	AD5
3	IO_L52P_3	AD6
3	IO_L51N_3/VREF_3	AD3
3	IO_L51P_3	AD4
3	IO_L50N_3	AB11
3	IO_L50P_3	AB12
3	IO_L49N_3	AE4
3	IO_L49P_3	AE5
3	IO_L48N_3	AE2
3	IO_L48P_3	AE3
3	IO_L47N_3	AC9
3	IO_L47P_3	AC10
3	IO_L46N_3	AE6
3	IO_L46P_3	AE7

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
3	IO_L45N_3/VREF_3	AF1
3	IO_L45P_3	AF2
3	IO_L44N_3	AD7
3	IO_L44P_3	AD8
3	IO_L43N_3	AF4
3	IO_L43P_3	AF5
3	IO_L42N_3	AG1
3	IO_L42P_3	AG2
3	IO_L41N_3	AC11
3	IO_L41P_3	AC12
3	IO_L40N_3	AG3
3	IO_L40P_3	AG4
3	IO_L39N_3/VREF_3	AH1
3	IO_L39P_3	AH2
3	IO_L38N_3	AD9
3	IO_L38P_3	AD10
3	IO_L37N_3	AF7
3	IO_L37P_3	AF8
3	IO_L36N_3	AH3
3	IO_L36P_3	AH4
3	IO_L35N_3	AD11
3	IO_L35P_3	AD12
3	IO_L34N_3	AG5
3	IO_L34P_3	AG6
3	IO_L33N_3/VREF_3	AJ2
3	IO_L33P_3	AJ3
3	IO_L32N_3	AE9
3	IO_L32P_3	AE10
3	IO_L31N_3	AH5
3	IO_L31P_3	AH6
3	IO_L30N_3	AK1
3	IO_L30P_3	AK2
3	IO_L29N_3	AG7
3	IO_L29P_3	AG8
3	IO_L28N_3	AJ5
3	IO_L28P_3	AJ6
3	IO_L27N_3/VREF_3	AL1
3	IO_L27P_3	AL2

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
3	IO_L26N_3	AF9
3	IO_L26P_3	AF10
3	IO_L25N_3	AK4
3	IO_L25P_3	AK5
3	IO_L24N_3	AM1
3	IO_L24P_3	AM2
3	IO_L23N_3	AE11
3	IO_L23P_3	AE12
3	IO_L22N_3	AM3
3	IO_L22P_3	AM4
3	IO_L21N_3/VREF_3	AL3
3	IO_L21P_3	AL4
3	IO_L20N_3	AG9
3	IO_L20P_3	AG10
3	IO_L19N_3	AK6
3	IO_L19P_3	AK7
3	IO_L18N_3	AN1
3	IO_L18P_3	AN2
3	IO_L17N_3	AF11
3	IO_L17P_3	AF12
3	IO_L16N_3	AL5
3	IO_L16P_3	AL6
3	IO_L15N_3/VREF_3	AP1
3	IO_L15P_3	AP2
3	IO_L14N_3	AJ7
3	IO_L14P_3	AJ8
3	IO_L13N_3	AM5
3	IO_L13P_3	AM6
3	IO_L12N_3	AN3
3	IO_L12P_3	AN4
3	IO_L11N_3	AG11
3	IO_L11P_3	AG12
3	IO_L10N_3	AN5
3	IO_L10P_3	AN6
3	IO_L09N_3/VREF_3	AR1
3	IO_L09P_3	AR2
3	IO_L08N_3	AK8
3	IO_L08P_3	AK9

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
3	IO_L07N_3	AR3
3	IO_L07P_3	AR4
3	IO_L06N_3	AP3
3	IO_L06P_3	AP4
3	IO_L05N_3	AL7
3	IO_L05P_3	AL8
3	IO_L04N_3	AP5
3	IO_L04P_3	AR6
3	IO_L03N_3/VREF_3	AT1
3	IO_L03P_3	AT2
3	IO_L02N_3	AM7
3	IO_L02P_3	AN8
3	IO_L01N_3/VRP_3	AT5
3	IO_L01P_3/VRN_3	AU5
4	IO_L01N_4/DOUT	AP7
4	IO_L01P_4/INIT_B	AR7
4	IO_L02N_4/D0	AP8
4	IO_L02P_4/D1	AR8
4	IO_L03N_4/D2	AT8
4	IO_L03P_4/D3	AU8
4	IO_L05_4/No_Pair	AM10
4	IO_L06N_4/VRP_4	AR9
4	IO_L06P_4/VRN_4	AT9
4	IO_L07N_4	AK11
4	IO_L07P_4/VREF_4	AL11
4	IO_L08N_4	AN9
4	IO_L08P_4	AP9
4	IO_L09N_4	AR10
4	IO_L09P_4/VREF_4	AT10
4	IO_L19N_4	AK12
4	IO_L19P_4	AK13
4	IO_L20N_4	AN10
4	IO_L20P_4	AP10
4	IO_L21N_4	AP11
4	IO_L21P_4	AR11
4	IO_L25N_4	AL12
4	IO_L25P_4	AM12

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
4	IO_L26N_4	AM11
4	IO_L26P_4	AN11
4	IO_L27N_4	AT11
4	IO_L27P_4/VREF_4	AU11
4	IO_L37N_4	AL13
4	IO_L37P_4	AM13
4	IO_L38N_4	AN12
4	IO_L38P_4	AP12
4	IO_L39N_4	AT12
4	IO_L39P_4	AU12
4	IO_L43N_4	AK14
4	IO_L43P_4	AL14
4	IO_L44N_4	AN13
4	IO_L44P_4	AP13
4	IO_L45N_4	AR13
4	IO_L45P_4/VREF_4	AT13
4	IO_L46N_4	AK15
4	IO_L46P_4	AL15
4	IO_L47N_4	AM14
4	IO_L47P_4	AN14
4	IO_L48N_4	AR14
4	IO_L48P_4	AT14
4	IO_L49N_4	AJ16
4	IO_L49P_4	AK16
4	IO_L50_4/No_Pair	AP15
4	IO_L53_4/No_Pair	AR15
4	IO_L54N_4	AT15
4	IO_L54P_4	AU15
4	IO_L55N_4	AM15
4	IO_L55P_4	AN15
4	IO_L56N_4	AN16
4	IO_L56P_4	AP16
4	IO_L57N_4	AR16
4	IO_L57P_4/VREF_4	AT16
4	IO_L58N_4	AL16
4	IO_L58P_4	AM16
4	IO_L59N_4	AN17
4	IO_L59P_4	AP17

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
4	IO_L60N_4	AT17
4	IO_L60P_4	AU17
4	IO_L64N_4	AK17
4	IO_L64P_4	AL17
4	IO_L65N_4	AM18
4	IO_L65P_4	AN18
4	IO_L66N_4	AP18
4	IO_L66P_4/VREF_4	AR18
4	IO_L67N_4	AK18
4	IO_L67P_4	AL18
4	IO_L68N_4	AM19
4	IO_L68P_4	AN19
4	IO_L69N_4	AT18
4	IO_L69P_4/VREF_4	AU18
4	IO_L73N_4	AK19
4	IO_L73P_4	AL19
4	IO_L74N_4/GCLK3S	AP19
4	IO_L74P_4/GCLK2P	AR19
4	IO_L75N_4/GCLK1S	AT19
4	IO_L75P_4/GCLK0P	AU19
5	IO_L75N_5/GCLK7S	AU21
5	IO_L75P_5/GCLK6P	AT21
5	IO_L74N_5/GCLK5S	AR21
5	IO_L74P_5/GCLK4P	AP21
5	IO_L73N_5	AL21
5	IO_L73P_5	AK21
5	IO_L69N_5/VREF_5	AU22
5	IO_L69P_5	AT22
5	IO_L68N_5	AN21
5	IO_L68P_5	AM21
5	IO_L67N_5	AL22
5	IO_L67P_5	AK22
5	IO_L66N_5/VREF_5	AR22
5	IO_L66P_5	AP22
5	IO_L65N_5	AN22
5	IO_L65P_5	AM22
5	IO_L64N_5	AL23

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
5	IO_L64P_5	AK23
5	IO_L60N_5	AU23
5	IO_L60P_5	AT23
5	IO_L59N_5	AP23
5	IO_L59P_5	AN23
5	IO_L58N_5	AM24
5	IO_L58P_5	AL24
5	IO_L57N_5/VREF_5	AT24
5	IO_L57P_5	AR24
5	IO_L56N_5	AP24
5	IO_L56P_5	AN24
5	IO_L55N_5	AN25
5	IO_L55P_5	AM25
5	IO_L54N_5	AU25
5	IO_L54P_5	AT25
5	IO_L53_5/No_Pair	AR25
5	IO_L50_5/No_Pair	AP25
5	IO_L49N_5	AK24
5	IO_L49P_5	AJ24
5	IO_L48N_5	AT26
5	IO_L48P_5	AR26
5	IO_L47N_5	AN26
5	IO_L47P_5	AM26
5	IO_L46N_5	AL25
5	IO_L46P_5	AK25
5	IO_L45N_5/VREF_5	AT27
5	IO_L45P_5	AR27
5	IO_L44N_5	AP27
5	IO_L44P_5	AN27
5	IO_L43N_5	AL26
5	IO_L43P_5	AK26
5	IO_L39N_5	AU28
5	IO_L39P_5	AT28
5	IO_L38N_5	AP28
5	IO_L38P_5	AN28
5	IO_L37N_5	AM27
5	IO_L37P_5	AL27
5	IO_L27N_5/VREF_5	AU29

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
5	IO_L27P_5	AT29
5	IO_L26N_5	AN29
5	IO_L26P_5	AM29
5	IO_L25N_5	AM28
5	IO_L25P_5	AL28
5	IO_L21N_5	AR29
5	IO_L21P_5	AP29
5	IO_L20N_5	AP30
5	IO_L20P_5	AN30
5	IO_L19N_5	AK27
5	IO_L19P_5	AK28
5	IO_L09N_5/VREF_5	AT30
5	IO_L09P_5	AR30
5	IO_L08N_5	AP31
5	IO_L08P_5	AN31
5	IO_L07N_5/VREF_5	AL29
5	IO_L07P_5	AK29
5	IO_L06N_5/VRP_5	AT31
5	IO_L06P_5/VRN_5	AR31
5	IO_L05_5/No_Pair	AM30
5	IO_L03N_5/D4	AU32
5	IO_L03P_5/D5	AT32
5	IO_L02N_5/D6	AR32
5	IO_L02P_5/D7	AP32
5	IO_L01N_5/RDWR_B	AR33
5	IO_L01P_5/CS_B	AP33
6	IO_L01P_6/VRN_6	AU35
6	IO_L01N_6/VRP_6	AT35
6	IO_L02P_6	AN32
6	IO_L02N_6	AM33
6	IO_L03P_6	AT38
6	IO_L03N_6/VREF_6	AT39
6	IO_L04P_6	AR34
6	IO_L04N_6	AP35
6	IO_L05P_6	AL32
6	IO_L05N_6	AL33
6	IO_L06P_6	AP36

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
6	IO_L06N_6	AP37
6	IO_L07P_6	AR36
6	IO_L07N_6	AR37
6	IO_L08P_6	AK31
6	IO_L08N_6	AK32
6	IO_L09P_6	AR38
6	IO_L09N_6/VREF_6	AR39
6	IO_L10P_6	AN34
6	IO_L10N_6	AN35
6	IO_L11P_6	AG28
6	IO_L11N_6	AG29
6	IO_L12P_6	AN36
6	IO_L12N_6	AN37
6	IO_L13P_6	AM34
6	IO_L13N_6	AM35
6	IO_L14P_6	AJ32
6	IO_L14N_6	AJ33
6	IO_L15P_6	AP38
6	IO_L15N_6/VREF_6	AP39
6	IO_L16P_6	AL34
6	IO_L16N_6	AL35
6	IO_L17P_6	AF28
6	IO_L17N_6	AF29
6	IO_L18P_6	AN38
6	IO_L18N_6	AN39
6	IO_L19P_6	AK33
6	IO_L19N_6	AK34
6	IO_L20P_6	AG30
6	IO_L20N_6	AG31
6	IO_L21P_6	AL36
6	IO_L21N_6/VREF_6	AL37
6	IO_L22P_6	AM36
6	IO_L22N_6	AM37
6	IO_L23P_6	AE28
6	IO_L23N_6	AE29
6	IO_L24P_6	AM38
6	IO_L24N_6	AM39
6	IO_L25P_6	AK35

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
6	IO_L25N_6	AK36
6	IO_L26P_6	AF30
6	IO_L26N_6	AF31
6	IO_L27P_6	AL38
6	IO_L27N_6/VREF_6	AL39
6	IO_L28P_6	AJ34
6	IO_L28N_6	AJ35
6	IO_L29P_6	AG32
6	IO_L29N_6	AG33
6	IO_L30P_6	AK38
6	IO_L30N_6	AK39
6	IO_L31P_6	AH34
6	IO_L31N_6	AH35
6	IO_L32P_6	AE30
6	IO_L32N_6	AE31
6	IO_L33P_6	AJ37
6	IO_L33N_6/VREF_6	AJ38
6	IO_L34P_6	AG34
6	IO_L34N_6	AG35
6	IO_L35P_6	AD28
6	IO_L35N_6	AD29
6	IO_L36P_6	AH36
6	IO_L36N_6	AH37
6	IO_L37P_6	AF32
6	IO_L37N_6	AF33
6	IO_L38P_6	AD30
6	IO_L38N_6	AD31
6	IO_L39P_6	AH38
6	IO_L39N_6/VREF_6	AH39
6	IO_L40P_6	AG36
6	IO_L40N_6	AG37
6	IO_L41P_6	AC28
6	IO_L41N_6	AC29
6	IO_L42P_6	AG38
6	IO_L42N_6	AG39
6	IO_L43P_6	AF35
6	IO_L43N_6	AF36
6	IO_L44P_6	AD32

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
6	IO_L44N_6	AD33
6	IO_L45P_6	AF38
6	IO_L45N_6/VREF_6	AF39
6	IO_L46P_6	AE33
6	IO_L46N_6	AE34
6	IO_L47P_6	AC30
6	IO_L47N_6	AC31
6	IO_L48P_6	AE37
6	IO_L48N_6	AE38
6	IO_L49P_6	AE35
6	IO_L49N_6	AE36
6	IO_L50P_6	AB28
6	IO_L50N_6	AB29
6	IO_L51P_6	AD36
6	IO_L51N_6/VREF_6	AD37
6	IO_L52P_6	AD34
6	IO_L52N_6	AD35
6	IO_L53P_6	AB30
6	IO_L53N_6	AB31
6	IO_L54P_6	AD38
6	IO_L54N_6	AD39
6	IO_L55P_6	AC33
6	IO_L55N_6	AC34
6	IO_L56P_6	AB32
6	IO_L56N_6	AB33
6	IO_L57P_6	AC36
6	IO_L57N_6/VREF_6	AC37
6	IO_L58P_6	AB34
6	IO_L58N_6	AB35
6	IO_L59P_6	AA28
6	IO_L59N_6	AA29
6	IO_L60P_6	AC38
6	IO_L60N_6	AC39
6	IO_L85P_6	AB36
6	IO_L85N_6	AB37
6	IO_L86P_6	AA30
6	IO_L86N_6	AA31
6	IO_L87P_6	AB38

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
6	IO_L87N_6/VREF_6	AB39
6	IO_L88P_6	AA34
6	IO_L88N_6	AA35
6	IO_L89P_6	AA32
6	IO_L89N_6	AA33
6	IO_L90P_6	AA36
6	IO_L90N_6	AA37
7	IO_L90P_7	W37
7	IO_L90N_7	W36
7	IO_L89P_7	W33
7	IO_L89N_7	W32
7	IO_L88P_7	V39
7	IO_L88N_7/VREF_7	V38
7	IO_L87P_7	W35
7	IO_L87N_7	W34
7	IO_L86P_7	W31
7	IO_L86N_7	W30
7	IO_L85P_7	V37
7	IO_L85N_7	V36
7	IO_L60P_7	V35
7	IO_L60N_7	V34
7	IO_L59P_7	W29
7	IO_L59N_7	W28
7	IO_L58P_7	U39
7	IO_L58N_7/VREF_7	U38
7	IO_L57P_7	U34
7	IO_L57N_7	U33
7	IO_L56P_7	V33
7	IO_L56N_7	V32
7	IO_L55P_7	U37
7	IO_L55N_7	U36
7	IO_L54P_7	T37
7	IO_L54N_7	T36
7	IO_L53P_7	V31
7	IO_L53N_7	V30
7	IO_L52P_7	T39
7	IO_L52N_7/VREF_7	T38

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
7	IO_L51P_7	T35
7	IO_L51N_7	T34
7	IO_L50P_7	V29
7	IO_L50N_7	V28
7	IO_L49P_7	R38
7	IO_L49N_7	R37
7	IO_L48P_7	R36
7	IO_L48N_7	R35
7	IO_L47P_7	U31
7	IO_L47N_7	U30
7	IO_L46P_7	P39
7	IO_L46N_7/VREF_7	P38
7	IO_L45P_7	R34
7	IO_L45N_7	R33
7	IO_L44P_7	T33
7	IO_L44N_7	T32
7	IO_L43P_7	N39
7	IO_L43N_7	N38
7	IO_L42P_7	P36
7	IO_L42N_7	P35
7	IO_L41P_7	U29
7	IO_L41N_7	U28
7	IO_L40P_7	N37
7	IO_L40N_7/VREF_7	N36
7	IO_L39P_7	N35
7	IO_L39N_7	N34
7	IO_L38P_7	T31
7	IO_L38N_7	T30
7	IO_L37P_7	M39
7	IO_L37N_7	M38
7	IO_L36P_7	M35
7	IO_L36N_7	M34
7	IO_L35P_7	T29
7	IO_L35N_7	T28
7	IO_L34P_7	M37
7	IO_L34N_7/VREF_7	M36
7	IO_L33P_7	N33
7	IO_L33N_7	N32

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
7	IO_L32P_7	R31
7	IO_L32N_7	R30
7	IO_L31P_7	L38
7	IO_L31N_7	L37
7	IO_L30P_7	L35
7	IO_L30N_7	L34
7	IO_L29P_7	P33
7	IO_L29N_7	P32
7	IO_L28P_7	K39
7	IO_L28N_7/VREF_7	K38
7	IO_L27P_7	K36
7	IO_L27N_7	K35
7	IO_L26P_7	P31
7	IO_L26N_7	P30
7	IO_L25P_7	J39
7	IO_L25N_7	J38
7	IO_L24P_7	J37
7	IO_L24N_7	J36
7	IO_L23P_7	R29
7	IO_L23N_7	R28
7	IO_L22P_7	H39
7	IO_L22N_7/VREF_7	H38
7	IO_L21P_7	K34
7	IO_L21N_7	K33
7	IO_L20P_7	N31
7	IO_L20N_7	N30
7	IO_L19P_7	G39
7	IO_L19N_7	G38
7	IO_L18P_7	J35
7	IO_L18N_7	J34
7	IO_L17P_7	P29
7	IO_L17N_7	P28
7	IO_L16P_7	H37
7	IO_L16N_7/VREF_7	H36
7	IO_L15P_7	H35
7	IO_L15N_7	H34
7	IO_L14P_7	L33
7	IO_L14N_7	L32

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
7	IO_L13P_7	F39
7	IO_L13N_7	F38
7	IO_L12P_7	F37
7	IO_L12N_7	F36
7	IO_L11P_7	N29
7	IO_L11N_7	N28
7	IO_L10P_7	G37
7	IO_L10N_7/VREF_7	G36
7	IO_L09P_7	G35
7	IO_L09N_7	G34
7	IO_L08P_7	K32
7	IO_L08N_7	K31
7	IO_L07P_7	E39
7	IO_L07N_7	E38
7	IO_L06P_7	F35
7	IO_L06N_7	E34
7	IO_L05P_7	J33
7	IO_L05N_7	J32
7	IO_L04P_7	D39
7	IO_L04N_7/VREF_7	D38
7	IO_L03P_7	D35
7	IO_L03N_7	C35
7	IO_L02P_7	H33
7	IO_L02N_7	G32
7	IO_L01P_7/VRN_7	E37
7	IO_L01N_7/VRP_7	E36
0	VCCO_0	P25
0	VCCO_0	P24
0	VCCO_0	P23
0	VCCO_0	P22
0	VCCO_0	P21
0	VCCO_0	N26
0	VCCO_0	N25
0	VCCO_0	N24
0	VCCO_0	N23
0	VCCO_0	N22
0	VCCO_0	N21

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Bank	Pin Description	Pin Number
0	VCCO_0	N20
0	VCCO_0	H23
0	VCCO_0	F26
0	VCCO_0	E28
1	VCCO_1	P20
1	VCCO_1	P19
1	VCCO_1	P18
1	VCCO_1	P17
1	VCCO_1	P16
1	VCCO_1	P15
1	VCCO_1	N19
1	VCCO_1	N18
1	VCCO_1	N17
1	VCCO_1	N16
1	VCCO_1	N15
1	VCCO_1	N14
1	VCCO_1	H17
1	VCCO_1	F14
1	VCCO_1	E12
2	VCCO_2	Y13
2	VCCO_2	W14
2	VCCO_2	W13
2	VCCO_2	V14
2	VCCO_2	V13
2	VCCO_2	U14
2	VCCO_2	U13
2	VCCO_2	T14
2	VCCO_2	T13
2	VCCO_2	R14
2	VCCO_2	R13
2	VCCO_2	R8
2	VCCO_2	P13
2	VCCO_2	M7
2	VCCO_2	L4
3	VCCO_3	AJ4
3	VCCO_3	AH7
3	VCCO_3	AF13
3	VCCO_3	AE14

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
3	VCCO_3	AE13
3	VCCO_3	AE8
3	VCCO_3	AD14
3	VCCO_3	AD13
3	VCCO_3	AC14
3	VCCO_3	AC13
3	VCCO_3	AB14
3	VCCO_3	AB13
3	VCCO_3	AA14
3	VCCO_3	AA13
3	VCCO_3	Y14
4	VCCO_4	AR12
4	VCCO_4	AP14
4	VCCO_4	AM17
4	VCCO_4	AG20
4	VCCO_4	AG19
4	VCCO_4	AG18
4	VCCO_4	AG17
4	VCCO_4	AG16
4	VCCO_4	AG15
4	VCCO_4	AG14
4	VCCO_4	AF19
4	VCCO_4	AF18
4	VCCO_4	AF17
4	VCCO_4	AF16
4	VCCO_4	AF15
5	VCCO_5	AR28
5	VCCO_5	AP26
5	VCCO_5	AM23
5	VCCO_5	AG26
5	VCCO_5	AG25
5	VCCO_5	AG24
5	VCCO_5	AG23
5	VCCO_5	AG22
5	VCCO_5	AG21
5	VCCO_5	AF25
5	VCCO_5	AF24
5	VCCO_5	AF23

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
5	VCCO_5	AF22
5	VCCO_5	AF21
5	VCCO_5	AF20
6	VCCO_6	AJ36
6	VCCO_6	AH33
6	VCCO_6	AF27
6	VCCO_6	AE32
6	VCCO_6	AE27
6	VCCO_6	AE26
6	VCCO_6	AD27
6	VCCO_6	AD26
6	VCCO_6	AC27
6	VCCO_6	AC26
6	VCCO_6	AB27
6	VCCO_6	AB26
6	VCCO_6	AA27
6	VCCO_6	AA26
6	VCCO_6	Y27
7	VCCO_7	Y26
7	VCCO_7	W27
7	VCCO_7	W26
7	VCCO_7	V27
7	VCCO_7	V26
7	VCCO_7	U27
7	VCCO_7	U26
7	VCCO_7	T27
7	VCCO_7	T26
7	VCCO_7	R32
7	VCCO_7	R27
7	VCCO_7	R26
7	VCCO_7	P27
7	VCCO_7	M33
7	VCCO_7	L36
N/A	CCLK	AT6
N/A	PROG_B	E33
N/A	DONE	AL10
N/A	M0	AT33

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	M1	AT34
N/A	M2	AL30
N/A	TCK	E7
N/A	TDI	F33
N/A	TDO	F7
N/A	TMS	D6
N/A	PWRDWN_B	AT7
N/A	HSWAP_EN	D34
N/A	RSVD	D7
N/A	VBATT	J10
N/A	DXP	J30
N/A	DXN	D33
N/A	AVCCAUXTX2	B35
N/A	VTTXPAD2	B36
N/A	TXNPAD2	A36
N/A	TXPPAD2	A35
N/A	GNDA2	C34
N/A	GNDA2	C34
N/A	RXPPAD2	A34
N/A	RXNPAD2	A33
N/A	VTRXPAD2	B34
N/A	AVCCAUXRX2	B33
N/A	AVCCAUXTX4	B31
N/A	VTTXPAD4	B32
N/A	TXNPAD4	A32
N/A	TXPPAD4	A31
N/A	GNDA4	C31
N/A	GNDA4	C31
N/A	RXPPAD4	A30
N/A	RXNPAD4	A29
N/A	VTRXPAD4	B30
N/A	AVCCAUXRX4	B29
N/A	AVCCAUXTX5	B27
N/A	VTTXPAD5	B28
N/A	TXNPAD5	A28
N/A	TXPPAD5	A27
N/A	GNDA5	C27
N/A	GNDA5	C27

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	RXPPAD5	A26
N/A	RXNPAD5	A25
N/A	VTRXPAD5	B26
N/A	AVCCAUXRX5	B25
N/A	AVCCAUXTX6	B23
N/A	VTTXPAD6	B24
N/A	TXNPAD6	A24
N/A	TXPPAD6	A23
N/A	GNDA6	C24
N/A	GNDA6	C24
N/A	RXPPAD6	A22
N/A	RXNPAD6	A21
N/A	VTRXPAD6	B22
N/A	AVCCAUXRX6	B21
N/A	AVCCAUXTX7	B18
N/A	VTTXPAD7	B19
N/A	TXNPAD7	A19
N/A	TXPPAD7	A18
N/A	GNDA7	C16
N/A	GNDA7	C16
N/A	RXPPAD7	A17
N/A	RXNPAD7	A16
N/A	VTRXPAD7	B17
N/A	AVCCAUXRX7	B16
N/A	AVCCAUXTX8	B14
N/A	VTTXPAD8	B15
N/A	TXNPAD8	A15
N/A	TXPPAD8	A14
N/A	GNDA8	C13
N/A	GNDA8	C13
N/A	RXPPAD8	A13
N/A	RXNPAD8	A12
N/A	VTRXPAD8	B13
N/A	AVCCAUXRX8	B12
N/A	AVCCAUXTX9	B10
N/A	VTTXPAD9	B11
N/A	TXNPAD9	A11
N/A	TXPPAD9	A10

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Bank	Pin Description	Pin Number
N/A	GNDA9	C9
N/A	GNDA9	C9
N/A	RXPPAD9	A9
N/A	RXNPAD9	A8
N/A	VTRXPAD9	B9
N/A	AVCCAUXRX9	B8
N/A	AVCCAUXTX11	B6
N/A	VTTXPAD11	B7
N/A	TXNPAD11	A7
N/A	TXPPAD11	A6
N/A	GNDA11	C6
N/A	GNDA11	C6
N/A	RXPPAD11	A5
N/A	RXNPAD11	A4
N/A	VTRXPAD11	B5
N/A	AVCCAUXRX11	B4
N/A	AVCCAUXRX14	AV4
N/A	VTRXPAD14	AV5
N/A	RXNPAD14	AW4
N/A	RXPPAD14	AW5
N/A	GNDA14	AU6
N/A	GNDA14	AU6
N/A	TXPPAD14	AW6
N/A	TXNPAD14	AW7
N/A	VTTXPAD14	AV7
N/A	AVCCAUXTX14	AV6
N/A	AVCCAUXRX16	AV8
N/A	VTRXPAD16	AV9
N/A	RXNPAD16	AW8
N/A	RXPPAD16	AW9
N/A	GNDA16	AU9
N/A	GNDA16	AU9
N/A	TXPPAD16	AW10
N/A	TXNPAD16	AW11
N/A	VTTXPAD16	AV11
N/A	AVCCAUXTX16	AV10
N/A	AVCCAUXRX17	AV12
N/A	VTRXPAD17	AV13

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	RXNPAD17	AW12
N/A	RXPPAD17	AW13
N/A	GNDA17	AU13
N/A	GNDA17	AU13
N/A	TXPPAD17	AW14
N/A	TXNPAD17	AW15
N/A	VTTXPAD17	AV15
N/A	AVCCAUXTX17	AV14
N/A	AVCCAUXRX18	AV16
N/A	VTRXPAD18	AV17
N/A	RXNPAD18	AW16
N/A	RXPPAD18	AW17
N/A	GNDA18	AU16
N/A	GNDA18	AU16
N/A	TXPPAD18	AW18
N/A	TXNPAD18	AW19
N/A	VTTXPAD18	AV19
N/A	AVCCAUXTX18	AV18
N/A	AVCCAUXRX19	AV21
N/A	VTRXPAD19	AV22
N/A	RXNPAD19	AW21
N/A	RXPPAD19	AW22
N/A	GNDA19	AU24
N/A	GNDA19	AU24
N/A	TXPPAD19	AW23
N/A	TXNPAD19	AW24
N/A	VTTXPAD19	AV24
N/A	AVCCAUXTX19	AV23
N/A	AVCCAUXRX20	AV25
N/A	VTRXPAD20	AV26
N/A	RXNPAD20	AW25
N/A	RXPPAD20	AW26
N/A	GNDA20	AU27
N/A	GNDA20	AU27
N/A	TXPPAD20	AW27
N/A	TXNPAD20	AW28
N/A	VTTXPAD20	AV28
N/A	AVCCAUXTX20	AV27

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	AVCCAUXRX21	AV29
N/A	VTRXPAD21	AV30
N/A	RXNPAD21	AW29
N/A	RXPPAD21	AW30
N/A	GNDA21	AU31
N/A	GNDA21	AU31
N/A	TXPPAD21	AW31
N/A	TXNPAD21	AW32
N/A	VTTXPAD21	AV32
N/A	AVCCAUXTX21	AV31
N/A	AVCCAUXRX23	AV33
N/A	VTRXPAD23	AV34
N/A	RXNPAD23	AW33
N/A	RXPPAD23	AW34
N/A	GNDA23	AU34
N/A	GNDA23	AU34
N/A	TXPPAD23	AW35
N/A	TXNPAD23	AW36
N/A	VTTXPAD23	AV36
N/A	AVCCAUXTX23	AV35
N/A	VCCINT	AH28
N/A	VCCINT	AH12
N/A	VCCINT	AG27
N/A	VCCINT	AG13
N/A	VCCINT	AF26
N/A	VCCINT	AF14
N/A	VCCINT	AE25
N/A	VCCINT	AE24
N/A	VCCINT	AE23
N/A	VCCINT	AE22
N/A	VCCINT	AE21
N/A	VCCINT	AE20
N/A	VCCINT	AE19
N/A	VCCINT	AE18
N/A	VCCINT	AE17
N/A	VCCINT	AE16
N/A	VCCINT	AE15

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	VCCINT	AD25
N/A	VCCINT	AD24
N/A	VCCINT	AD16
N/A	VCCINT	AD15
N/A	VCCINT	AC25
N/A	VCCINT	AC15
N/A	VCCINT	AB25
N/A	VCCINT	AB15
N/A	VCCINT	AA25
N/A	VCCINT	AA15
N/A	VCCINT	Y25
N/A	VCCINT	Y15
N/A	VCCINT	W25
N/A	VCCINT	W15
N/A	VCCINT	V25
N/A	VCCINT	V15
N/A	VCCINT	U25
N/A	VCCINT	U15
N/A	VCCINT	T25
N/A	VCCINT	T24
N/A	VCCINT	T16
N/A	VCCINT	T15
N/A	VCCINT	R25
N/A	VCCINT	R24
N/A	VCCINT	R23
N/A	VCCINT	R22
N/A	VCCINT	R21
N/A	VCCINT	R20
N/A	VCCINT	R19
N/A	VCCINT	R18
N/A	VCCINT	R17
N/A	VCCINT	R16
N/A	VCCINT	R15
N/A	VCCINT	P26
N/A	VCCINT	P14
N/A	VCCINT	N27
N/A	VCCINT	N13
N/A	VCCINT	M28

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	VCCINT	M12
N/A	VCCAUX	AV20
N/A	VCCAUX	AU36
N/A	VCCAUX	AU20
N/A	VCCAUX	AU4
N/A	VCCAUX	AT37
N/A	VCCAUX	AT3
N/A	VCCAUX	AL31
N/A	VCCAUX	AL9
N/A	VCCAUX	AK30
N/A	VCCAUX	AK10
N/A	VCCAUX	AA39
N/A	VCCAUX	AA1
N/A	VCCAUX	Y39
N/A	VCCAUX	Y38
N/A	VCCAUX	Y2
N/A	VCCAUX	Y1
N/A	VCCAUX	W39
N/A	VCCAUX	W1
N/A	VCCAUX	K30
N/A	VCCAUX	K10
N/A	VCCAUX	J31
N/A	VCCAUX	J9
N/A	VCCAUX	D37
N/A	VCCAUX	D3
N/A	VCCAUX	C36
N/A	VCCAUX	C20
N/A	VCCAUX	C4
N/A	VCCAUX	B20
N/A	GND	AW38
N/A	GND	AW37
N/A	GND	AW20
N/A	GND	AW3
N/A	GND	AW2
N/A	GND	AV39
N/A	GND	AV38
N/A	GND	AV37
N/A	GND	AV3

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	GND	AV2
N/A	GND	AV1
N/A	GND	AU39
N/A	GND	AU38
N/A	GND	AU37
N/A	GND	AU30
N/A	GND	AU26
N/A	GND	AU14
N/A	GND	AU10
N/A	GND	AU3
N/A	GND	AU2
N/A	GND	AU1
N/A	GND	AT36
N/A	GND	AT20
N/A	GND	AT4
N/A	GND	AR35
N/A	GND	AR23
N/A	GND	AR17
N/A	GND	AR5
N/A	GND	AP34
N/A	GND	AP6
N/A	GND	AN33
N/A	GND	AN20
N/A	GND	AN7
N/A	GND	AM32
N/A	GND	AM8
N/A	GND	AK37
N/A	GND	AK20
N/A	GND	AK3
N/A	GND	AJ39
N/A	GND	AJ1
N/A	GND	AF37
N/A	GND	AF34
N/A	GND	AF6
N/A	GND	AF3
N/A	GND	AE39
N/A	GND	AE1
N/A	GND	AD23

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	GND	AD22
N/A	GND	AD21
N/A	GND	AD20
N/A	GND	AD19
N/A	GND	AD18
N/A	GND	AD17
N/A	GND	AC35
N/A	GND	AC32
N/A	GND	AC24
N/A	GND	AC23
N/A	GND	AC22
N/A	GND	AC21
N/A	GND	AC20
N/A	GND	AC19
N/A	GND	AC18
N/A	GND	AC17
N/A	GND	AC16
N/A	GND	AC8
N/A	GND	AC5
N/A	GND	AB24
N/A	GND	AB23
N/A	GND	AB22
N/A	GND	AB21
N/A	GND	AB20
N/A	GND	AB19
N/A	GND	AB18
N/A	GND	AB17
N/A	GND	AB16
N/A	GND	AA38
N/A	GND	AA24
N/A	GND	AA23
N/A	GND	AA22
N/A	GND	AA21
N/A	GND	AA20
N/A	GND	AA19
N/A	GND	AA18
N/A	GND	AA17
N/A	GND	AA16

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Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	GND	AA2
N/A	GND	Y37
N/A	GND	Y36
N/A	GND	Y33
N/A	GND	Y30
N/A	GND	Y24
N/A	GND	Y23
N/A	GND	Y22
N/A	GND	Y21
N/A	GND	Y20
N/A	GND	Y19
N/A	GND	Y18
N/A	GND	Y17
N/A	GND	Y16
N/A	GND	Y10
N/A	GND	Y7
N/A	GND	Y4
N/A	GND	Y3
N/A	GND	W38
N/A	GND	W24
N/A	GND	W23
N/A	GND	W22
N/A	GND	W21
N/A	GND	W20
N/A	GND	W19
N/A	GND	W18
N/A	GND	W17
N/A	GND	W16
N/A	GND	W2
N/A	GND	V24
N/A	GND	V23
N/A	GND	V22
N/A	GND	V21
N/A	GND	V20
N/A	GND	V19
N/A	GND	V18
N/A	GND	V17
N/A	GND	V16

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	GND	U35
N/A	GND	U32
N/A	GND	U24
N/A	GND	U23
N/A	GND	U22
N/A	GND	U21
N/A	GND	U20
N/A	GND	U19
N/A	GND	U18
N/A	GND	U17
N/A	GND	U16
N/A	GND	U8
N/A	GND	U5
N/A	GND	T23
N/A	GND	T22
N/A	GND	T21
N/A	GND	T20
N/A	GND	T19
N/A	GND	T18
N/A	GND	T17
N/A	GND	R39
N/A	GND	R1
N/A	GND	P37
N/A	GND	P34
N/A	GND	P6
N/A	GND	P3
N/A	GND	L39
N/A	GND	L1
N/A	GND	K37
N/A	GND	K20
N/A	GND	K3
N/A	GND	H32
N/A	GND	H8
N/A	GND	G33
N/A	GND	G20
N/A	GND	G7
N/A	GND	F34
N/A	GND	F6

Table 11: **FF1517 — XC2VP50**

Bank	Pin Description	Pin Number
N/A	GND	E35
N/A	GND	E23
N/A	GND	E17
N/A	GND	E5
N/A	GND	D36
N/A	GND	D20
N/A	GND	D4
N/A	GND	C39
N/A	GND	C38
N/A	GND	C37
N/A	GND	C30
N/A	GND	C26
N/A	GND	C14
N/A	GND	C10
N/A	GND	C3
N/A	GND	C2
N/A	GND	C1
N/A	GND	B39
N/A	GND	B38
N/A	GND	B37
N/A	GND	B3
N/A	GND	B2
N/A	GND	B1
N/A	GND	A38
N/A	GND	A37
N/A	GND	A20
N/A	GND	A3
N/A	GND	A2

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

S Y M B O L	MILLIMETERS			N O T E
	MIN.	NOM.	MAX.	
A	⌇	3.20	3.40	
A₁	0.40	0.50	0.60	
A₂	⌇	⌇	2.80	
D/E	40.00 BASIC			
D₁/E₁	38.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	⌇	⌇	0.20	
bbb	⌇	⌇	0.25	
ddd	⌇	⌇	0.25	
eee	⌇	⌇	0.10	
M		39		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994

2. SYMBOL "M" IS THE PIN MATRIX SIZE.

3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)
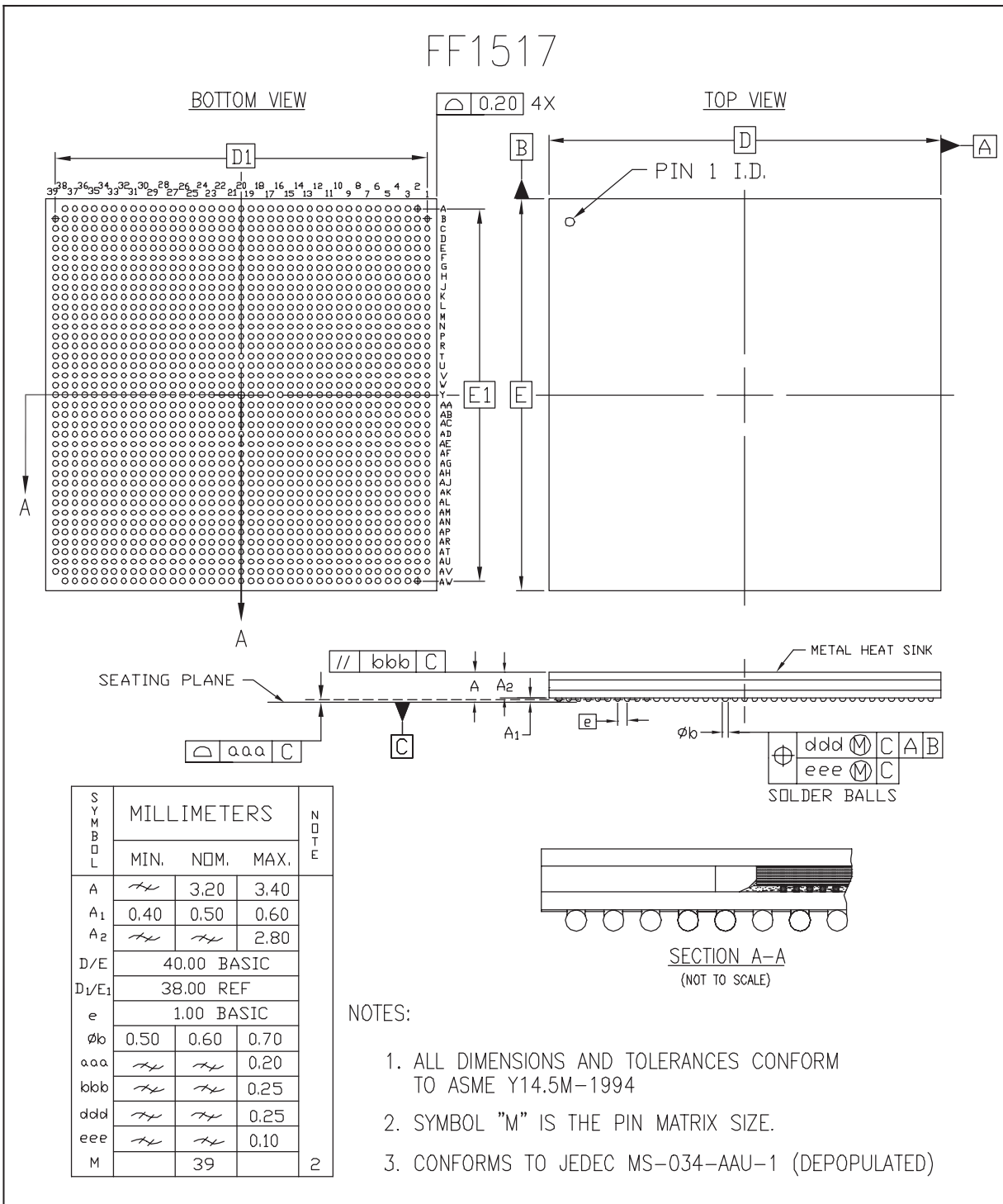
Figure 6: **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**

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BF957 Flip-Chip BGA Package

As shown in Table 12, XC2VP20 and XC2VP50 Virtex-II Pro devices are available in the BF957 flip-chip BGA package. Pins in each of these devices are the same, except for the differences shown in the "No Connects" column. Following this table are the **BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)**.

Table 12: **BF957 — XC2VP20 and XC2VP50**

| | | | No Connects | |
| | | | XC2V P20 | XC2V P50 |
Bank	Pin Description	Pin Number		
0	IO_L01N_0/VRP_0	E26		
0	IO_L01P_0/VRN_0	E25		
0	IO_L02N_0	H23		
0	IO_L02P_0	G23		
0	IO_L03N_0	F25		
0	IO_L03P_0/VREF_0	F24		
0	IO_L05_0/No_Pair	G24		
0	IO_L06N_0	J22		
0	IO_L06P_0	H22		
0	IO_L07N_0	F23		
0	IO_L07P_0	E23		
0	IO_L08N_0	D25		
0	IO_L08P_0	C25		
0	IO_L09N_0	K21		
0	IO_L09P_0/VREF_0	J21		
0	IO_L19N_0	G22	NC	
0	IO_L19P_0	F22	NC	
0	IO_L37N_0	H21		
0	IO_L37P_0	G21		
0	IO_L38N_0	E24		
0	IO_L38P_0	D24		
0	IO_L39N_0	K20		
0	IO_L39P_0	J20		
0	IO_L43N_0	F21		
0	IO_L43P_0	E21		
0	IO_L44N_0	D23		
0	IO_L44P_0	D22		
0	IO_L45N_0	H20		
0	IO_L45P_0/VREF_0	G20		
0	IO_L46N_0	F20		
0	IO_L46P_0	E20		
0	IO_L47N_0	C22		
0	IO_L47P_0	C21		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
0	IO_L48N_0	K19		
0	IO_L48P_0	J19		
0	IO_L49N_0	H19		
0	IO_L49P_0	G19		
0	IO_L50_0/No_Pair	D21		
0	IO_L53_0/No_Pair	D20		
0	IO_L54N_0	K18		
0	IO_L54P_0	J18		
0	IO_L55N_0	F18		
0	IO_L55P_0	E18		
0	IO_L56N_0	E19		
0	IO_L56P_0	D19		
0	IO_L57N_0	H18		
0	IO_L57P_0/VREF_0	G18		
0	IO_L67N_0	H17		
0	IO_L67P_0	G17		
0	IO_L68N_0	D18		
0	IO_L68P_0	C18		
0	IO_L69N_0	K17		
0	IO_L69P_0/VREF_0	J17		
0	IO_L73N_0	F17		
0	IO_L73P_0	E17		
0	IO_L74N_0/GCLK7P	D17		
0	IO_L74P_0/GCLK6S	C17		
0	IO_L75N_0/GCLK5P	F16		
0	IO_L75P_0/GCLK4S	E16		
1	IO_L75N_1/GCLK3P	H16		
1	IO_L75P_1/GCLK2S	J16		
1	IO_L74N_1/GCLK1P	C15		
1	IO_L74P_1/GCLK0S	D15		
1	IO_L73N_1	E15		
1	IO_L73P_1	F15		
1	IO_L69N_1/VREF_1	J15		
1	IO_L69P_1	K15		
1	IO_L68N_1	C14		
1	IO_L68P_1	D14		
1	IO_L67N_1	G15		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
1	IO_L67P_1	H15		
1	IO_L57N_1/VREF_1	G14		
1	IO_L57P_1	H14		
1	IO_L56N_1	D13		
1	IO_L56P_1	E13		
1	IO_L55N_1	E14		
1	IO_L55P_1	F14		
1	IO_L54N_1	J14		
1	IO_L54P_1	K14		
1	IO_L53_1/No_Pair	D12		
1	IO_L50_1/No_Pair	D11		
1	IO_L49N_1	G13		
1	IO_L49P_1	H13		
1	IO_L48N_1	J13		
1	IO_L48P_1	K13		
1	IO_L47N_1	C11		
1	IO_L47P_1	C10		
1	IO_L46N_1	E12		
1	IO_L46P_1	F12		
1	IO_L45N_1/VREF_1	G12		
1	IO_L45P_1	H12		
1	IO_L44N_1	D10		
1	IO_L44P_1	D9		
1	IO_L43N_1	E11		
1	IO_L43P_1	F11		
1	IO_L39N_1	J12		
1	IO_L39P_1	K12		
1	IO_L38N_1	D8		
1	IO_L38P_1	E8		
1	IO_L37N_1	G11		
1	IO_L37P_1	H11		
1	IO_L19N_1	F10	NC	
1	IO_L19P_1	G10	NC	
1	IO_L09N_1/VREF_1	J11		
1	IO_L09P_1	K11		
1	IO_L08N_1	C7		
1	IO_L08P_1	D7		
1	IO_L07N_1	E9		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
1	IO_L07P_1	F9		
1	IO_L06N_1	H10		
1	IO_L06P_1	J10		
1	IO_L05_1/No_Pair	G8		
1	IO_L03N_1/VREF_1	F8		
1	IO_L03P_1	F7		
1	IO_L02N_1	G9		
1	IO_L02P_1	H9		
1	IO_L01N_1/VRP_1	E7		
1	IO_L01P_1/VRN_1	E6		
2	IO_L01N_2/VRP_2	D2		
2	IO_L01P_2/VRN_2	D1		
2	IO_L02N_2	K9		
2	IO_L02P_2	K8		
2	IO_L03N_2	C4		
2	IO_L03P_2	D3		
2	IO_L04N_2/VREF_2	E2		
2	IO_L04P_2	E1		
2	IO_L05N_2	L10		
2	IO_L05P_2	L9		
2	IO_L06N_2	E4		
2	IO_L06P_2	E3		
2	IO_L18N_2	F5	NC	
2	IO_L18P_2	F4	NC	
2	IO_L31N_2	G4		
2	IO_L31P_2	G3		
2	IO_L32N_2	J7		
2	IO_L32P_2	J6		
2	IO_L33N_2	G6		
2	IO_L33P_2	G5		
2	IO_L34N_2/VREF_2	F2		
2	IO_L34P_2	F1		
2	IO_L35N_2	K7		
2	IO_L35P_2	K6		
2	IO_L36N_2	H5		
2	IO_L36P_2	H4		
2	IO_L37N_2	G2		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
2	IO_L37P_2	G1		
2	IO_L38N_2	M10		
2	IO_L38P_2	M9		
2	IO_L39N_2	J4		
2	IO_L39P_2	J3		
2	IO_L40N_2/VREF_2	H2		
2	IO_L40P_2	H1		
2	IO_L41N_2	L8		
2	IO_L41P_2	L7		
2	IO_L42N_2	K5		
2	IO_L42P_2	K4		
2	IO_L43N_2	J2		
2	IO_L43P_2	J1		
2	IO_L44N_2	M8		
2	IO_L44P_2	M7		
2	IO_L45N_2	L6		
2	IO_L45P_2	L5		
2	IO_L46N_2/VREF_2	K2		
2	IO_L46P_2	K1		
2	IO_L47N_2	N10		
2	IO_L47P_2	N9		
2	IO_L48N_2	L4		
2	IO_L48P_2	L3		
2	IO_L49N_2	L2		
2	IO_L49P_2	L1		
2	IO_L50N_2	M6		
2	IO_L50P_2	M5		
2	IO_L51N_2	M4		
2	IO_L51P_2	M3		
2	IO_L52N_2/VREF_2	M2		
2	IO_L52P_2	M1		
2	IO_L53N_2	N8		
2	IO_L53P_2	N7		
2	IO_L54N_2	N5		
2	IO_L54P_2	N4		
2	IO_L55N_2	N2		
2	IO_L55P_2	N1		
2	IO_L56N_2	P10		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
2	IO_L56P_2	P9		
2	IO_L57N_2	P6		
2	IO_L57P_2	P5		
2	IO_L58N_2/VREF_2	P4		
2	IO_L58P_2	P3		
2	IO_L59N_2	P8		
2	IO_L59P_2	P7		
2	IO_L60N_2	R6		
2	IO_L60P_2	R5		
2	IO_L85N_2	P2		
2	IO_L85P_2	P1		
2	IO_L86N_2	R10		
2	IO_L86P_2	R9		
2	IO_L87N_2	R4		
2	IO_L87P_2	R3		
2	IO_L88N_2/VREF_2	R2		
2	IO_L88P_2	R1		
2	IO_L89N_2	R8		
2	IO_L89P_2	R7		
2	IO_L90N_2	T5		
2	IO_L90P_2	T6		
3	IO_L90N_3	U1		
3	IO_L90P_3	U2		
3	IO_L89N_3	T8		
3	IO_L89P_3	T9		
3	IO_L88N_3	U3		
3	IO_L88P_3	U4		
3	IO_L87N_3/VREF_3	V1		
3	IO_L87P_3	V2		
3	IO_L86N_3	U7		
3	IO_L86P_3	U8		
3	IO_L85N_3	U5		
3	IO_L85P_3	U6		
3	IO_L60N_3	V3		
3	IO_L60P_3	V4		
3	IO_L59N_3	U9		
3	IO_L59P_3	U10		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
3	IO_L58N_3	V5		
3	IO_L58P_3	V6		
3	IO_L57N_3/VREF_3	W1		
3	IO_L57P_3	W2		
3	IO_L56N_3	V7		
3	IO_L56P_3	V8		
3	IO_L55N_3	W4		
3	IO_L55P_3	W5		
3	IO_L54N_3	Y1		
3	IO_L54P_3	Y2		
3	IO_L53N_3	V9		
3	IO_L53P_3	V10		
3	IO_L52N_3	Y3		
3	IO_L52P_3	Y4		
3	IO_L51N_3/VREF_3	AA1		
3	IO_L51P_3	AA2		
3	IO_L50N_3	W7		
3	IO_L50P_3	W8		
3	IO_L49N_3	Y5		
3	IO_L49P_3	Y6		
3	IO_L48N_3	AB1		
3	IO_L48P_3	AB2		
3	IO_L47N_3	W9		
3	IO_L47P_3	W10		
3	IO_L46N_3	AA3		
3	IO_L46P_3	AA4		
3	IO_L45N_3/VREF_3	AC1		
3	IO_L45P_3	AC2		
3	IO_L44N_3	Y7		
3	IO_L44P_3	Y8		
3	IO_L43N_3	AA5		
3	IO_L43P_3	AA6		
3	IO_L42N_3	AD1		
3	IO_L42P_3	AD2		
3	IO_L41N_3	AA7		
3	IO_L41P_3	AA8		
3	IO_L40N_3	AB4		
3	IO_L40P_3	AB5		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
3	IO_L39N_3/VREF_3	AC3		
3	IO_L39P_3	AC4		
3	IO_L38N_3	Y9		
3	IO_L38P_3	Y10		
3	IO_L37N_3	AD4		
3	IO_L37P_3	AD5		
3	IO_L36N_3	AE1		
3	IO_L36P_3	AE2		
3	IO_L35N_3	AB6		
3	IO_L35P_3	AB7		
3	IO_L34N_3	AE3		
3	IO_L34P_3	AE4		
3	IO_L33N_3/VREF_3	AF1		
3	IO_L33P_3	AF2		
3	IO_L32N_3	AC6		
3	IO_L32P_3	AC7		
3	IO_L31N_3	AE5		
3	IO_L31P_3	AE6		
3	IO_L18N_3	AG1	NC	
3	IO_L18P_3	AG2	NC	
3	IO_L17N_3	AA9	NC	
3	IO_L17P_3	AA10	NC	
3	IO_L06N_3	AH1		
3	IO_L06P_3	AH2		
3	IO_L05N_3	AB8		
3	IO_L05P_3	AB9		
3	IO_L04N_3	AF4		
3	IO_L04P_3	AF5		
3	IO_L03N_3/VREF_3	AG3		
3	IO_L03P_3	AG4		
3	IO_L02N_3	AD6		
3	IO_L02P_3	AD7		
3	IO_L01N_3/VRP_3	AH3		
3	IO_L01P_3/VRN_3	AJ4		
4	IO_L01N_4/DOUT	AG6		
4	IO_L01P_4/INIT_B	AG7		
4	IO_L02N_4/D0	AF7		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
4	IO_L02P_4/D1	AF8		
4	IO_L03N_4/D2	AH7		
4	IO_L03P_4/D3	AJ7		
4	IO_L05_4/No_Pair	AE8		
4	IO_L06N_4/VRP_4	AG8		
4	IO_L06P_4/VRN_4	AH8		
4	IO_L07N_4	AC10		
4	IO_L07P_4/VREF_4	AD10		
4	IO_L08N_4	AD9		
4	IO_L08P_4	AE9		
4	IO_L09N_4	AF9		
4	IO_L09P_4/VREF_4	AG9		
4	IO_L19N_4	AB11	NC	
4	IO_L19P_4	AC11	NC	
4	IO_L37N_4	AB12		
4	IO_L37P_4	AC12		
4	IO_L38N_4	AE10		
4	IO_L38P_4	AF10		
4	IO_L39N_4	AH9		
4	IO_L39P_4	AH10		
4	IO_L43N_4	AD11		
4	IO_L43P_4	AE11		
4	IO_L44N_4	AF11		
4	IO_L44P_4	AG11		
4	IO_L45N_4	AJ10		
4	IO_L45P_4/VREF_4	AJ11		
4	IO_L46N_4	AB13		
4	IO_L46P_4	AC13		
4	IO_L47N_4	AD12		
4	IO_L47P_4	AE12		
4	IO_L48N_4	AH11		
4	IO_L48P_4	AH12		
4	IO_L49N_4	AB14		
4	IO_L49P_4	AC14		
4	IO_L50_4/No_Pair	AF12		
4	IO_L53_4/No_Pair	AG12		
4	IO_L54N_4	AG13		
4	IO_L54P_4	AH13		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
4	IO_L55N_4	AD14		
4	IO_L55P_4	AE14		
4	IO_L56N_4	AD13		
4	IO_L56P_4	AE13		
4	IO_L57N_4	AF14		
4	IO_L57P_4/VREF_4	AG14		
4	IO_L67N_4	AB15		
4	IO_L67P_4	AC15		
4	IO_L68N_4	AD15		
4	IO_L68P_4	AE15		
4	IO_L69N_4	AH14		
4	IO_L69P_4/VREF_4	AJ14		
4	IO_L73N_4	AC16		
4	IO_L73P_4	AD16		
4	IO_L74N_4/GCLK3S	AF15		
4	IO_L74P_4/GCLK2P	AG15		
4	IO_L75N_4/GCLK1S	AH15		
4	IO_L75P_4/GCLK0P	AJ15		
5	IO_L75N_5/GCLK7S	AJ17		
5	IO_L75P_5/GCLK6P	AH17		
5	IO_L74N_5/GCLK5S	AG17		
5	IO_L74P_5/GCLK4P	AF17		
5	IO_L73N_5	AG16		
5	IO_L73P_5	AF16		
5	IO_L69N_5/VREF_5	AJ18		
5	IO_L69P_5	AH18		
5	IO_L68N_5	AE17		
5	IO_L68P_5	AD17		
5	IO_L67N_5	AC17		
5	IO_L67P_5	AB17		
5	IO_L57N_5/VREF_5	AG18		
5	IO_L57P_5	AF18		
5	IO_L56N_5	AE19		
5	IO_L56P_5	AD19		
5	IO_L55N_5	AE18		
5	IO_L55P_5	AD18		
5	IO_L54N_5	AH19		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
5	IO_L54P_5	AG19		
5	IO_L53_5/No_Pair	AG20		
5	IO_L50_5/No_Pair	AF20		
5	IO_L49N_5	AC18		
5	IO_L49P_5	AB18		
5	IO_L48N_5	AH20		
5	IO_L48P_5	AH21		
5	IO_L47N_5	AE20		
5	IO_L47P_5	AD20		
5	IO_L46N_5	AC19		
5	IO_L46P_5	AB19		
5	IO_L45N_5/VREF_5	AJ21		
5	IO_L45P_5	AJ22		
5	IO_L44N_5	AG21		
5	IO_L44P_5	AF21		
5	IO_L43N_5	AE21		
5	IO_L43P_5	AD21		
5	IO_L39N_5	AH22		
5	IO_L39P_5	AH23		
5	IO_L38N_5	AF22		
5	IO_L38P_5	AE22		
5	IO_L37N_5	AC20		
5	IO_L37P_5	AB20		
5	IO_L19N_5	AC21	NC	
5	IO_L19P_5	AB21	NC	
5	IO_L09N_5/VREF_5	AG23		
5	IO_L09P_5	AF23		
5	IO_L08N_5	AE23		
5	IO_L08P_5	AD23		
5	IO_L07N_5/VREF_5	AD22		
5	IO_L07P_5	AC22		
5	IO_L06N_5/VRP_5	AH24		
5	IO_L06P_5/VRN_5	AG24		
5	IO_L05_5/No_Pair	AE24		
5	IO_L03N_5/D4	AJ25		
5	IO_L03P_5/D5	AH25		
5	IO_L02N_5/D6	AF24		
5	IO_L02P_5/D7	AF25		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
5	IO_L01N_5/RDWR_B	AG25		
5	IO_L01P_5/CS_B	AG26		
6	IO_L01P_6/VRN_6	AJ28		
6	IO_L01N_6/VRP_6	AH29		
6	IO_L02P_6	AD25		
6	IO_L02N_6	AD26		
6	IO_L03P_6	AG28		
6	IO_L03N_6/VREF_6	AG29		
6	IO_L04P_6	AF27		
6	IO_L04N_6	AF28		
6	IO_L05P_6	AB23		
6	IO_L05N_6	AB24		
6	IO_L06P_6	AH30		
6	IO_L06N_6	AH31		
6	IO_L17P_6	AA22	NC	
6	IO_L17N_6	AA23	NC	
6	IO_L18P_6	AG30	NC	
6	IO_L18N_6	AG31	NC	
6	IO_L31P_6	AE26		
6	IO_L31N_6	AE27		
6	IO_L32P_6	AC25		
6	IO_L32N_6	AC26		
6	IO_L33P_6	AF30		
6	IO_L33N_6/VREF_6	AF31		
6	IO_L34P_6	AE28		
6	IO_L34N_6	AE29		
6	IO_L35P_6	AB25		
6	IO_L35N_6	AB26		
6	IO_L36P_6	AE30		
6	IO_L36N_6	AE31		
6	IO_L37P_6	AD27		
6	IO_L37N_6	AD28		
6	IO_L38P_6	Y22		
6	IO_L38N_6	Y23		
6	IO_L39P_6	AC28		
6	IO_L39N_6/VREF_6	AC29		
6	IO_L40P_6	AB27		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2VP20	No Connects XC2VP50
6	IO_L40N_6	AB28		
6	IO_L41P_6	AA24		
6	IO_L41N_6	AA25		
6	IO_L42P_6	AD30		
6	IO_L42N_6	AD31		
6	IO_L43P_6	AA26		
6	IO_L43N_6	AA27		
6	IO_L44P_6	Y24		
6	IO_L44N_6	Y25		
6	IO_L45P_6	AC30		
6	IO_L45N_6/VREF_6	AC31		
6	IO_L46P_6	AA28		
6	IO_L46N_6	AA29		
6	IO_L47P_6	W22		
6	IO_L47N_6	W23		
6	IO_L48P_6	AB30		
6	IO_L48N_6	AB31		
6	IO_L49P_6	Y26		
6	IO_L49N_6	Y27		
6	IO_L50P_6	W24		
6	IO_L50N_6	W25		
6	IO_L51P_6	AA30		
6	IO_L51N_6/VREF_6	AA31		
6	IO_L52P_6	Y28		
6	IO_L52N_6	Y29		
6	IO_L53P_6	V22		
6	IO_L53N_6	V23		
6	IO_L54P_6	Y30		
6	IO_L54N_6	Y31		
6	IO_L55P_6	W27		
6	IO_L55N_6	W28		
6	IO_L56P_6	V24		
6	IO_L56N_6	V25		
6	IO_L57P_6	W30		
6	IO_L57N_6/VREF_6	W31		
6	IO_L58P_6	V26		
6	IO_L58N_6	V27		
6	IO_L59P_6	U22		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
6	IO_L59N_6	U23		
6	IO_L60P_6	V28		
6	IO_L60N_6	V29		
6	IO_L85P_6	U26		
6	IO_L85N_6	U27		
6	IO_L86P_6	U24		
6	IO_L86N_6	U25		
6	IO_L87P_6	V30		
6	IO_L87N_6/VREF_6	V31		
6	IO_L88P_6	U28		
6	IO_L88N_6	U29		
6	IO_L89P_6	T23		
6	IO_L89N_6	T24		
6	IO_L90P_6	U30		
6	IO_L90N_6	U31		
7	IO_L90P_7	T26		
7	IO_L90N_7	T27		
7	IO_L89P_7	R25		
7	IO_L89N_7	R24		
7	IO_L88P_7	R31		
7	IO_L88N_7/VREF_7	R30		
7	IO_L87P_7	R29		
7	IO_L87N_7	R28		
7	IO_L86P_7	R23		
7	IO_L86N_7	R22		
7	IO_L85P_7	P31		
7	IO_L85N_7	P30		
7	IO_L60P_7	R27		
7	IO_L60N_7	R26		
7	IO_L59P_7	P25		
7	IO_L59N_7	P24		
7	IO_L58P_7	P29		
7	IO_L58N_7/VREF_7	P28		
7	IO_L57P_7	P27		
7	IO_L57N_7	P26		
7	IO_L56P_7	P23		
7	IO_L56N_7	P22		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2VP20	XC2VP50
7	IO_L55P_7	N31		
7	IO_L55N_7	N30		
7	IO_L54P_7	N28		
7	IO_L54N_7	N27		
7	IO_L53P_7	N25		
7	IO_L53N_7	N24		
7	IO_L52P_7	M31		
7	IO_L52N_7/VREF_7	M30		
7	IO_L51P_7	M29		
7	IO_L51N_7	M28		
7	IO_L50P_7	M27		
7	IO_L50N_7	M26		
7	IO_L49P_7	L31		
7	IO_L49N_7	L30		
7	IO_L48P_7	L29		
7	IO_L48N_7	L28		
7	IO_L47P_7	N23		
7	IO_L47N_7	N22		
7	IO_L46P_7	K31		
7	IO_L46N_7/VREF_7	K30		
7	IO_L45P_7	L27		
7	IO_L45N_7	L26		
7	IO_L44P_7	M25		
7	IO_L44N_7	M24		
7	IO_L43P_7	J31		
7	IO_L43N_7	J30		
7	IO_L42P_7	K28		
7	IO_L42N_7	K27		
7	IO_L41P_7	L25		
7	IO_L41N_7	L24		
7	IO_L40P_7	H31		
7	IO_L40N_7/VREF_7	H30		
7	IO_L39P_7	J29		
7	IO_L39N_7	J28		
7	IO_L38P_7	M23		
7	IO_L38N_7	M22		
7	IO_L37P_7	G31		
7	IO_L37N_7	G30		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
7	IO_L36P_7	H28		
7	IO_L36N_7	H27		
7	IO_L35P_7	K26		
7	IO_L35N_7	K25		
7	IO_L34P_7	F31		
7	IO_L34N_7/VREF_7	F30		
7	IO_L33P_7	G27		
7	IO_L33N_7	G26		
7	IO_L32P_7	J26		
7	IO_L32N_7	J25		
7	IO_L31P_7	G29		
7	IO_L31N_7	G28		
7	IO_L18P_7	F28	NC	
7	IO_L18N_7	F27	NC	
7	IO_L06P_7	E29		
7	IO_L06N_7	E28		
7	IO_L05P_7	L23		
7	IO_L05N_7	L22		
7	IO_L04P_7	E31		
7	IO_L04N_7/VREF_7	E30		
7	IO_L03P_7	D29		
7	IO_L03N_7	C28		
7	IO_L02P_7	K24		
7	IO_L02N_7	K23		
7	IO_L01P_7/VRN_7	D31		
7	IO_L01N_7/VRP_7	D30		
0	VCCO_0	M19		
0	VCCO_0	M18		
0	VCCO_0	M17		
0	VCCO_0	L20		
0	VCCO_0	L19		
0	VCCO_0	L18		
0	VCCO_0	L17		
0	VCCO_0	E22		
0	VCCO_0	C26		
0	VCCO_0	C19		
1	VCCO_1	M15		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
1	VCCO_1	M14		
1	VCCO_1	M13		
1	VCCO_1	L15		
1	VCCO_1	L14		
1	VCCO_1	L13		
1	VCCO_1	L12		
1	VCCO_1	E10		
1	VCCO_1	C13		
1	VCCO_1	C6		
2	VCCO_2	R12		
2	VCCO_2	R11		
2	VCCO_2	P12		
2	VCCO_2	P11		
2	VCCO_2	N12		
2	VCCO_2	N11		
2	VCCO_2	N3		
2	VCCO_2	M11		
2	VCCO_2	J5		
2	VCCO_2	F3		
3	VCCO_3	AF3		
3	VCCO_3	AC5		
3	VCCO_3	Y11		
3	VCCO_3	W12		
3	VCCO_3	W11		
3	VCCO_3	W3		
3	VCCO_3	V12		
3	VCCO_3	V11		
3	VCCO_3	U12		
3	VCCO_3	U11		
4	VCCO_4	AJ13		
4	VCCO_4	AJ6		
4	VCCO_4	AG10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	Y15		
4	VCCO_4	Y14		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
4	VCCO_4	Y13		
5	VCCO_5	AJ26		
5	VCCO_5	AJ19		
5	VCCO_5	AG22		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	Y19		
5	VCCO_5	Y18		
5	VCCO_5	Y17		
6	VCCO_6	AF29		
6	VCCO_6	AC27		
6	VCCO_6	Y21		
6	VCCO_6	W29		
6	VCCO_6	W21		
6	VCCO_6	W20		
6	VCCO_6	V21		
6	VCCO_6	V20		
6	VCCO_6	U21		
6	VCCO_6	U20		
7	VCCO_7	R21		
7	VCCO_7	R20		
7	VCCO_7	P21		
7	VCCO_7	P20		
7	VCCO_7	N29		
7	VCCO_7	N21		
7	VCCO_7	N20		
7	VCCO_7	M21		
7	VCCO_7	J27		
7	VCCO_7	F29		
N/A	CCLK	AC8		
N/A	PROG_B	J24		
N/A	DONE	AH6		
N/A	M0	AH27		
N/A	M1	AC24		
N/A	M2	AH26		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

			No Connects	
Bank	**Pin Description**	**Pin Number**	**XC2V P20**	**XC2V P50**
N/A	TCK	J8		
N/A	TDI	H26		
N/A	TDO	H6		
N/A	TMS	H7		
N/A	PWRDWN_B	AH5		
N/A	HSWAP_EN	H25		
N/A	RSVD	D6		
N/A	VBATT	D5		
N/A	DXP	D27		
N/A	DXN	D26		
N/A	AVCCAUXTX2	B27	NC	
N/A	VTTXPAD2	B28	NC	
N/A	TXNPAD2	A28	NC	
N/A	TXPPAD2	A27	NC	
N/A	GNDA2	C27	NC	
N/A	GNDA2	C27	NC	
N/A	RXPPAD2	A26	NC	
N/A	RXNPAD2	A25	NC	
N/A	VTRXPAD2	B26	NC	
N/A	AVCCAUXRX2	B25	NC	
N/A	AVCCAUXTX4	B23		
N/A	VTTXPAD4	B24		
N/A	TXNPAD4	A24		
N/A	TXPPAD4	A23		
N/A	GNDA4	C24		
N/A	GNDA4	C24		
N/A	RXPPAD4	A22		
N/A	RXNPAD4	A21		
N/A	VTRXPAD4	B22		
N/A	AVCCAUXRX4	B21		
N/A	AVCCAUXTX6	B19		
N/A	VTTXPAD6	B20		
N/A	TXNPAD6	A20		
N/A	TXPPAD6	A19		
N/A	GNDA6	C20		
N/A	GNDA6	C20		
N/A	RXPPAD6	A18		
N/A	RXNPAD6	A17		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	VTRXPAD6	B18		
N/A	AVCCAUXRX6	B17		
N/A	AVCCAUXTX7	B14		
N/A	VTTXPAD7	B15		
N/A	TXNPAD7	A15		
N/A	TXPPAD7	A14		
N/A	GNDA7	C12		
N/A	GNDA7	C12		
N/A	RXPPAD7	A13		
N/A	RXNPAD7	A12		
N/A	VTRXPAD7	B13		
N/A	AVCCAUXRX7	B12		
N/A	AVCCAUXTX9	B10		
N/A	VTTXPAD9	B11		
N/A	TXNPAD9	A11		
N/A	TXPPAD9	A10		
N/A	GNDA9	C8		
N/A	GNDA9	C8		
N/A	RXPPAD9	A9		
N/A	RXNPAD9	A8		
N/A	VTRXPAD9	B9		
N/A	AVCCAUXRX9	B8		
N/A	AVCCAUXTX11	B6	NC	
N/A	VTTXPAD11	B7	NC	
N/A	TXNPAD11	A7	NC	
N/A	TXPPAD11	A6	NC	
N/A	GNDA11	C5	NC	
N/A	GNDA11	C5	NC	
N/A	RXPPAD11	A5	NC	
N/A	RXNPAD11	A4	NC	
N/A	VTRXPAD11	B5	NC	
N/A	AVCCAUXRX11	B4	NC	
N/A	AVCCAUXRX14	AK4	NC	
N/A	VTRXPAD14	AK5	NC	
N/A	RXNPAD14	AL4	NC	
N/A	RXPPAD14	AL5	NC	
N/A	GNDA14	AJ5	NC	
N/A	GNDA14	AJ5	NC	

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
N/A	TXPPAD14	AL6	NC	
N/A	TXNPAD14	AL7	NC	
N/A	VTTXPAD14	AK7	NC	
N/A	AVCCAUXTX14	AK6	NC	
N/A	AVCCAUXRX16	AK8		
N/A	VTRXPAD16	AK9		
N/A	RXNPAD16	AL8		
N/A	RXPPAD16	AL9		
N/A	GNDA16	AJ8		
N/A	GNDA16	AJ8		
N/A	TXPPAD16	AL10		
N/A	TXNPAD16	AL11		
N/A	VTTXPAD16	AK11		
N/A	AVCCAUXTX16	AK10		
N/A	AVCCAUXRX18	AK12		
N/A	VTRXPAD18	AK13		
N/A	RXNPAD18	AL12		
N/A	RXPPAD18	AL13		
N/A	GNDA18	AJ12		
N/A	GNDA18	AJ12		
N/A	TXPPAD18	AL14		
N/A	TXNPAD18	AL15		
N/A	VTTXPAD18	AK15		
N/A	AVCCAUXTX18	AK14		
N/A	AVCCAUXRX19	AK17		
N/A	VTRXPAD19	AK18		
N/A	RXNPAD19	AL17		
N/A	RXPPAD19	AL18		
N/A	GNDA19	AJ20		
N/A	GNDA19	AJ20		
N/A	TXPPAD19	AL19		
N/A	TXNPAD19	AL20		
N/A	VTTXPAD19	AK20		
N/A	AVCCAUXTX19	AK19		
N/A	AVCCAUXRX21	AK21		
N/A	VTRXPAD21	AK22		
N/A	RXNPAD21	AL21		
N/A	RXPPAD21	AL22		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	GNDA21	AJ24		
N/A	GNDA21	AJ24		
N/A	TXPPAD21	AL23		
N/A	TXNPAD21	AL24		
N/A	VTTXPAD21	AK24		
N/A	AVCCAUXTX21	AK23		
N/A	AVCCAUXRX23	AK25	NC	
N/A	VTRXPAD23	AK26	NC	
N/A	RXNPAD23	AL25	NC	
N/A	RXPPAD23	AL26	NC	
N/A	GNDA23	AJ27	NC	
N/A	GNDA23	AJ27	NC	
N/A	TXPPAD23	AL27	NC	
N/A	TXNPAD23	AL28	NC	
N/A	VTTXPAD23	AK28	NC	
N/A	AVCCAUXTX23	AK27	NC	
N/A	VCCAUX	AK29		
N/A	VCCAUX	AK16		
N/A	VCCAUX	AK3		
N/A	VCCAUX	AJ30		
N/A	VCCAUX	AJ16		
N/A	VCCAUX	AJ2		
N/A	VCCAUX	T30		
N/A	VCCAUX	T29		
N/A	VCCAUX	T3		
N/A	VCCAUX	T2		
N/A	VCCAUX	C30		
N/A	VCCAUX	C16		
N/A	VCCAUX	C2		
N/A	VCCAUX	B29		
N/A	VCCAUX	B16		
N/A	VCCAUX	B3		
N/A	VCCINT	AA21		
N/A	VCCINT	AA16		
N/A	VCCINT	AA11		
N/A	VCCINT	Y20		
N/A	VCCINT	Y16		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	No Connects XC2V P50
N/A	VCCINT	Y12		
N/A	VCCINT	W19		
N/A	VCCINT	W18		
N/A	VCCINT	W17		
N/A	VCCINT	W16		
N/A	VCCINT	W15		
N/A	VCCINT	W14		
N/A	VCCINT	W13		
N/A	VCCINT	V19		
N/A	VCCINT	V13		
N/A	VCCINT	U19		
N/A	VCCINT	U13		
N/A	VCCINT	T21		
N/A	VCCINT	T20		
N/A	VCCINT	T19		
N/A	VCCINT	T13		
N/A	VCCINT	T12		
N/A	VCCINT	T11		
N/A	VCCINT	R19		
N/A	VCCINT	R13		
N/A	VCCINT	P19		
N/A	VCCINT	P13		
N/A	VCCINT	N19		
N/A	VCCINT	N18		
N/A	VCCINT	N17		
N/A	VCCINT	N16		
N/A	VCCINT	N15		
N/A	VCCINT	N14		
N/A	VCCINT	N13		
N/A	VCCINT	M20		
N/A	VCCINT	M16		
N/A	VCCINT	M12		
N/A	VCCINT	L21		
N/A	VCCINT	L16		
N/A	VCCINT	L11		
N/A	GND	AL30		
N/A	GND	AL29		
N/A	GND	AL16		

Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects	
			XC2V P20	XC2V P50
N/A	GND	AL3		
N/A	GND	AL2		
N/A	GND	AK31		
N/A	GND	AK30		
N/A	GND	AK2		
N/A	GND	AK1		
N/A	GND	AJ31		
N/A	GND	AJ29		
N/A	GND	AJ23		
N/A	GND	AJ9		
N/A	GND	AJ3		
N/A	GND	AJ1		
N/A	GND	AH28		
N/A	GND	AH16		
N/A	GND	AH4		
N/A	GND	AG27		
N/A	GND	AG5		
N/A	GND	AF26		
N/A	GND	AF19		
N/A	GND	AF13		
N/A	GND	AF6		
N/A	GND	AE25		
N/A	GND	AE16		
N/A	GND	AE7		
N/A	GND	AD29		
N/A	GND	AD24		
N/A	GND	AD8		
N/A	GND	AD3		
N/A	GND	AC23		
N/A	GND	AC9		
N/A	GND	AB29		
N/A	GND	AB22		
N/A	GND	AB16		
N/A	GND	AB10		
N/A	GND	AB3		
N/A	GND	W26		
N/A	GND	W6		
N/A	GND	V18		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

			No Connects	
Bank	**Pin Description**	**Pin Number**	**XC2V P20**	**XC2V P50**
N/A	GND	V17		
N/A	GND	V16		
N/A	GND	V15		
N/A	GND	V14		
N/A	GND	U18		
N/A	GND	U17		
N/A	GND	U16		
N/A	GND	U15		
N/A	GND	U14		
N/A	GND	T31		
N/A	GND	T28		
N/A	GND	T25		
N/A	GND	T22		
N/A	GND	T18		
N/A	GND	T17		
N/A	GND	T16		
N/A	GND	T15		
N/A	GND	T14		
N/A	GND	T10		
N/A	GND	T7		
N/A	GND	T4		
N/A	GND	T1		
N/A	GND	R18		
N/A	GND	R17		
N/A	GND	R16		
N/A	GND	R15		
N/A	GND	R14		
N/A	GND	P18		
N/A	GND	P17		
N/A	GND	P16		
N/A	GND	P15		
N/A	GND	P14		
N/A	GND	N26		
N/A	GND	N6		
N/A	GND	K29		
N/A	GND	K22		
N/A	GND	K16		
N/A	GND	K10		

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Table 12: **BF957 — XC2VP20 and XC2VP50**

Bank	Pin Description	Pin Number	No Connects XC2V P20	XC2V P50
N/A	GND	K3		
N/A	GND	J23		
N/A	GND	J9		
N/A	GND	H29		
N/A	GND	H24		
N/A	GND	H8		
N/A	GND	H3		
N/A	GND	G25		
N/A	GND	G16		
N/A	GND	G7		
N/A	GND	F26		
N/A	GND	F19		
N/A	GND	F13		
N/A	GND	F6		
N/A	GND	E27		
N/A	GND	E5		
N/A	GND	D28		
N/A	GND	D16		
N/A	GND	D4		
N/A	GND	C31		
N/A	GND	C29		
N/A	GND	C23		
N/A	GND	C9		
N/A	GND	C3		
N/A	GND	C1		
N/A	GND	B31		
N/A	GND	B30		
N/A	GND	B2		
N/A	GND	B1		
N/A	GND	A30		
N/A	GND	A29		
N/A	GND	A16		
N/A	GND	A3		
N/A	GND	A2		

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BF957 Flip-Chip BGA Package Specifications (1.27mm pitch)

SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	~	3.25	3.50	
A₁	0.50	0.60	0.70	
A₂	~	~	2.80	
A₃	0.20	~	~	
D/E	40.00 BSC			
D₁/E₁	38.10 REF.			
e	1.27 BSC			
Øb	0.60	0.75	0.90	
aaa	~	~	0.20	
bbb	~	~	0.25	
ccc	~	~	0.15	
ddd	~	~	0.30	
M	31			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
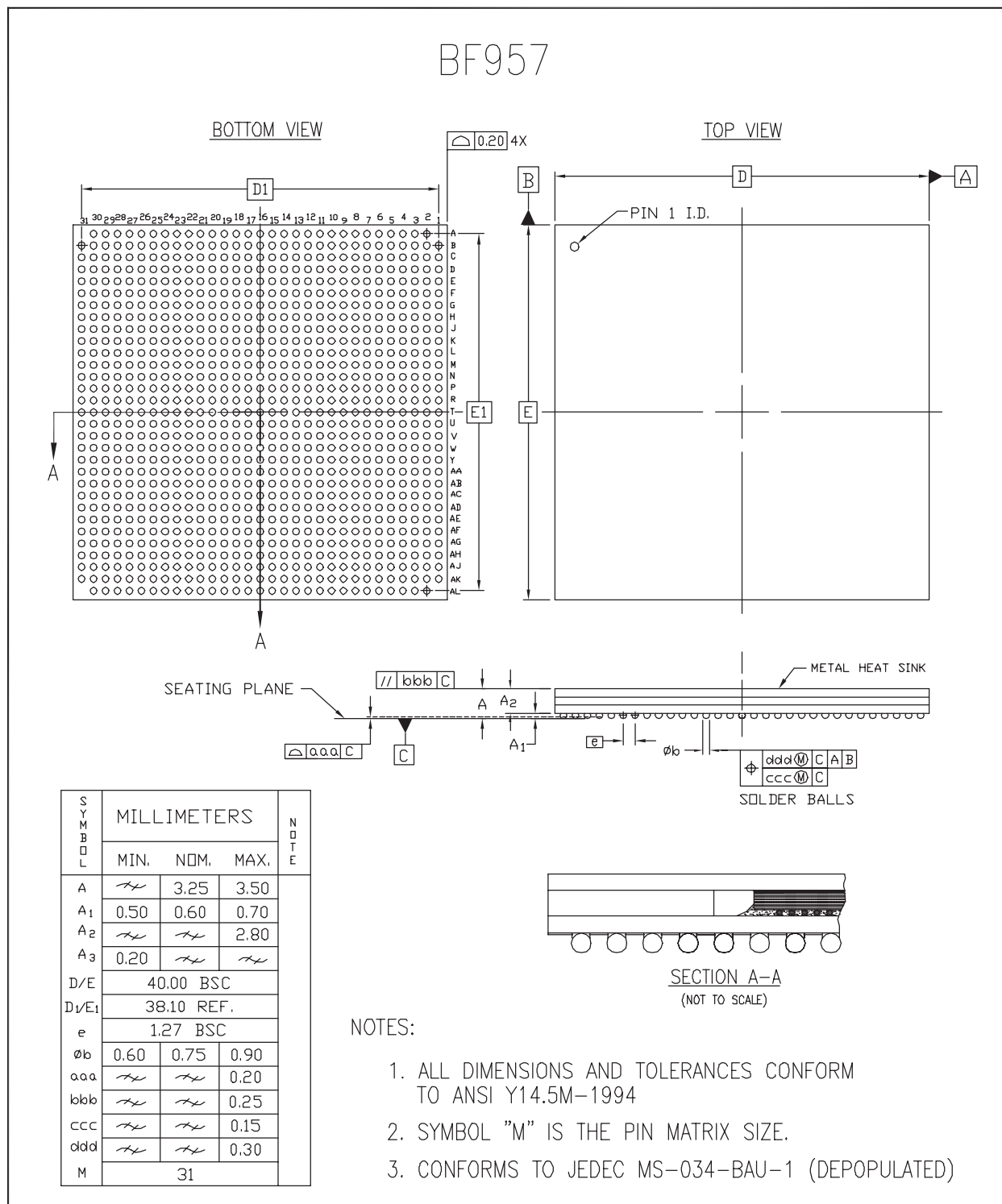3. CONFORMS TO JEDEC MS–034–BAU–1 (DEPOPULATED)

Figure 7: **BF957 Flip-Chip BGA Package Specifications**

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
1/31/02	1.0	Initial Xilinx release.

Virtex-II Pro Data Sheet Modules

The Virtex-II Pro Data Sheet contains the following modules:

- **Virtex-II Pro™ Platform FPGAs: Introduction and Overview (Module 1)**

- **Virtex-II Pro™ Platform FPGAs: Functional Description (Module 2)**

- **Virtex-II Pro™ Platform FPGAs: DC and Switching Characteristics (Module 3)**

- **Virtex-II Pro Platform FPGAs: Pinout Information (Module 4)**

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