Xilinx Parallel Cable IV

DS097 (v1.3) February 6, 2002 **Advance Product Specification**

Features

- Download speed of up to 4 Megabits per second (Mb/s)
- Over eight times faster than Xilinx Parallel Cable III using Xilinx iMPACT (v4.2i) download software
- ChipScope™ ILA compatible
- Configures all Xilinx devices
  - Virtex™/Virtex-E/Virtex-II
  - Spartan™/Spartan-XL/Spartan-II/Spartan-IIE
  - XC9500/ XC9500XL/ XC9500XV
  - CoolRunner™ (XPLA3)
  - XC18V00 ISP PROM Family
  - XC4000XL/XV/EX/E
  - System ACE™ Multi-Package Module (MPM)
- Automatically senses and adapts to correct I/O voltage
- Interfaces to devices operating at 5V (TTL), 3.3V (LVTTL), 2.5V, 1.8V, and 1.5V
- Supports JTAG (IEEE 1149.1) and Xilinx Slave Serial Modes
- J Drive IEEE 1532 Programming Engine compatible
- Includes high-performance ribbon cable
- Compliant with IEEE 1284 Level 2 Electrical Specification
- Externally powered using keyboard/mouse splitter cable or AC power brick
- LED status indicator
- Uses IEEE 1284 ECP protocol for high-speed communications

Parallel Cable IV Description

The new Xilinx Parallel Cable IV (PC IV) (Figure 1) is a high-speed download cable that configures or programs all Xilinx FPGA, CPLD, ISP PROM, and System ACE MPM devices. The cable takes advantage of the IEEE 1284 ECP protocol and Xilinx iMPACT software to increase download speeds over eight times faster than existing solutions. The cable automatically senses and adapts to target I/O voltages and is able to accommodate a wide range of I/O standards from 1.5V to 5V.

PC IV supports the widely used industry standard IEEE 1149.1 Boundary Scan (JTAG) specification using a four-wire interface. It also supports the Xilinx Slave Serial mode for Xilinx FPGA devices. It interfaces to target systems using a ribbon cable that features integral alternating ground leads to reduce noise and increase signal integrity.

The cable is externally powered from either a power “brick” or by interfacing to a standard PC mouse or keyboard connection. A bi-color status LED indicates the presence of operating and target reference voltages.

Connecting to Host Computer

The PC IV connects to any PC using Win98, Win2000, or WinNT (4.0 or higher) through the standard IEEE 1284 DB25 parallel (printer) port connector. To fully utilize the higher speeds of this cable, the host PC must have a parallel port that is enabled to support extended capability port (ECP) mode. If ECP mode is not enabled, the PC IV will default to compatibility mode and will not run at the optimum speeds listed.

Figure 1: **Xilinx Parallel Cable IV**

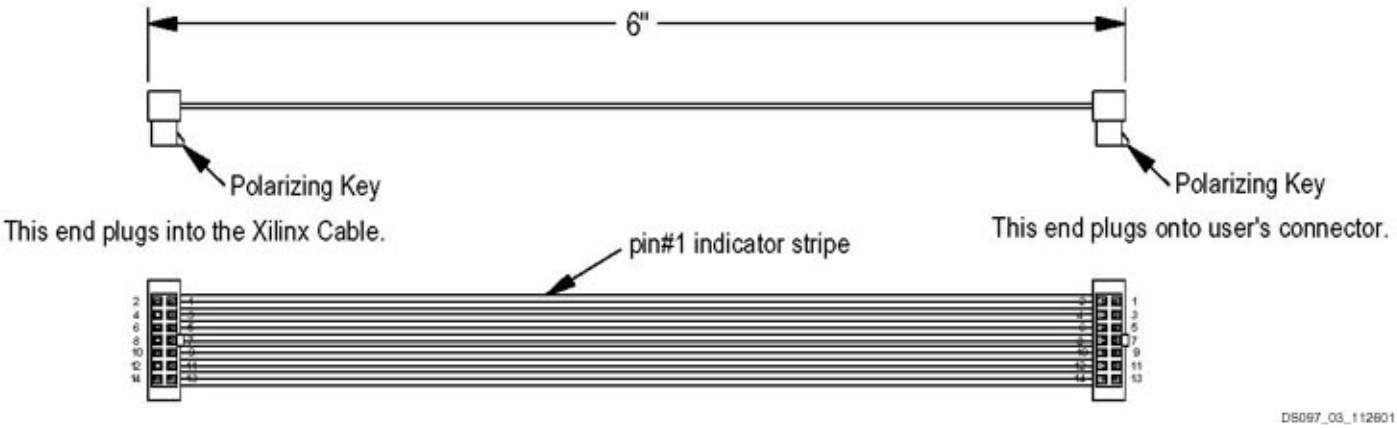
Notes:
1. Refer to host PC BIOS to see if ECP mode is enabled.

High Performance Ribbon Cable

An insulation displacement (IDC) ribbon cable is supplied and recommended for connection to target systems. See Figure 2 and Figure 3. This cable incorporates multiple signal-ground pairs and facilitates error-free connection. A very small footprint, keyed mating connector is all that is required on the target system. Refer to Figure 4 for the appropriate connector pin assignments and sample vendor part numbers.

The Parallel Cable IV can also interface to target systems using "flying lead wires." However, these are not included with PC IV and can be purchased separately from the Xilinx E-Commerce web site.

Figure 2: **High Performance Ribbon Cable**



Notes:
1. Ribbon Cable - 14 conductor 1.0mm centers Round Conductor Flat Cable; 28 AWG (7x36) stranded copper conductors; gray PVC with pin 1 edge marked.
2. 2mm Ribbon Female Polarized Connectors - IDC connection to ribbon; contacts are beryllium copper plated; 30 micro inches gold plating over 50 micro inches nickel; connectors mate to 0.5mm square posts on 2mm centers.

Figure 3: **Ribbon Cable Diagram**

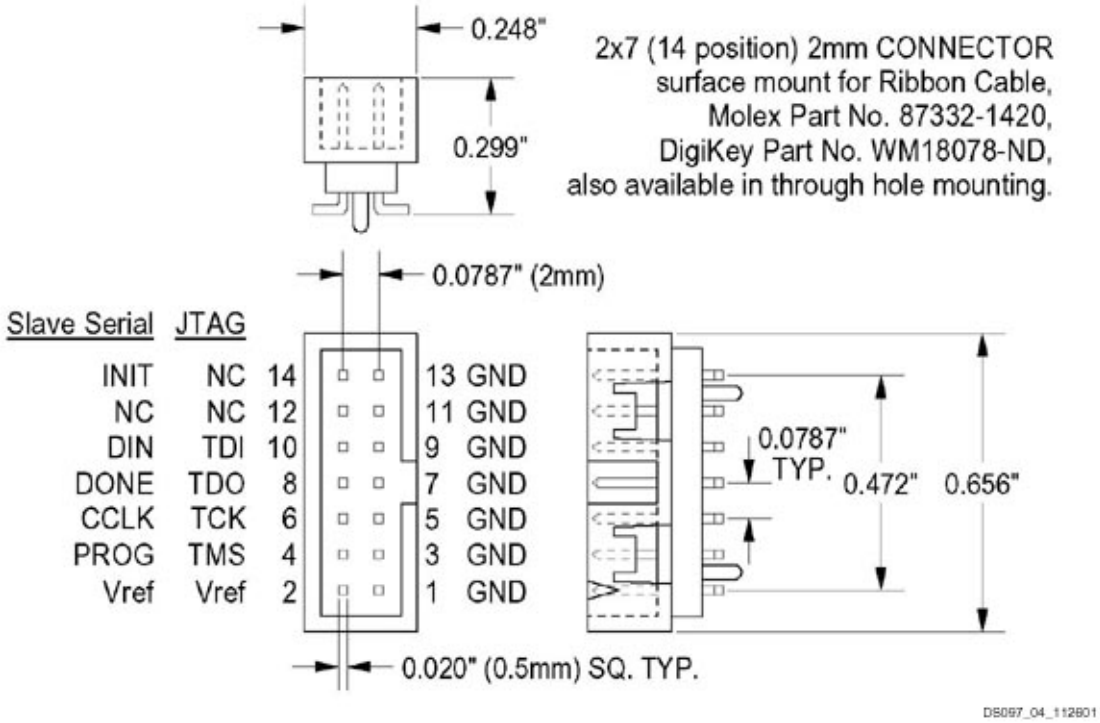


Figure 4: **Target Interface Connector Signal Assignments**

Table 1 provides some third-party sources for mating connectors that are compatible with the Parallel Cable IV ribbon cable.

Table 1: **Mating Connectors for 2mm pitch, 14 Conductor Ribbon Cable**

Manufacturer	SMT. Vertical	SMT. Right Angle	Through-Hole, Vertical	Through-Hole, Right Angle	Web Site
Molex	87332-1420	N/A	87331-1420	87333-1420	www.molex.com
FCI	95615-114	N/A	90309-114	95609-114	www.fciconnect.com
Comm Con Connectors	2475-14G2	N/A	2422-14G2	N/A	www.commcon.com

Cable Power

The host interface cable (Figure 5) includes a short power jack for connection to one of two possible +5V DC power sources: (1) the keyboard or mouse part of the host PC or (2) an external AC adapter. The supplied power splitter cable is required when using the first option. The splitter cable is installed between the mouse cable and the standard 6-pin mini-DIN connector on the host PC.

PC IV operating current is less than 100 mA. It draws approximately 15 mA from the target reference voltage bus to power the JTAG/Slave Serial buffers.

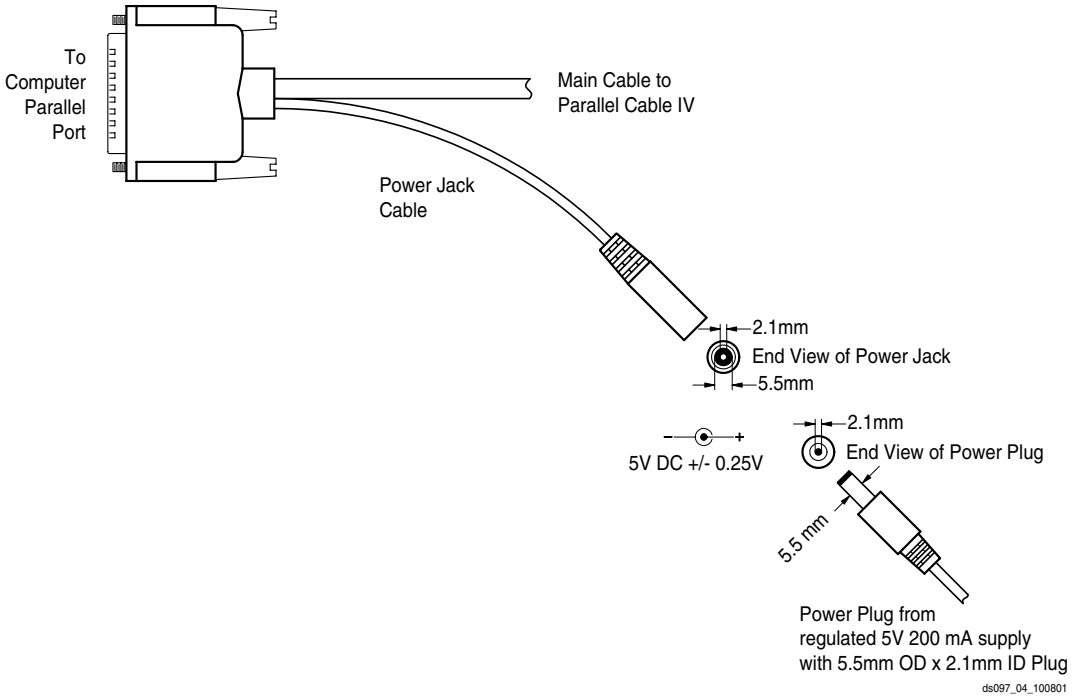


Figure 5: **Optional Power Brick Connection to Parallel Cable IV**

Power Supply Sources

Table 2 provides some third-party sources for power supplies that are compatible with the Parallel Cable IV.

Table 2: **Power Supply Sources**

Part Number	Description	Manufacturer	URL	Distributor	Distributor Part Number
DTS050240U/AC1-P5P	5V, 12W, 3 Prong Inlet	CUI Stack	www.cuistack.com	DigiKey	T805-P5P-ND
DTS050250SUDC-P5P	5V, 12W, 2 Prong Inlet	CUI Stack	www.cuistack.com	DigiKey	T850-P5P-ND
FW1805-S760 (1)	5V, 15W, 3 Prong Inlet	Elpac	www.elpac.com	-	-

Notes:

1. Elpac P/N FW1805-S760 can be purchased directly from the manufacturer when ordering a minimum of 250 pieces. Distributors only carry P/N FW1805-760, which uses a different size female jack on the DC output cable (2.5mm).
2. The 3-Prong Inlet power supplies are recommended for international use so that a variety of AC plug styles can be accommodated with a single power supply.
3. The PC IV *pigtail* connector will only mate with a power supply that uses a 2.1mm plug on its DC output cable.
4. The external power supply must provide a regulated +5.0V DC @ 200 mA minimum.

Status LED

The Status LED will indicate one of two possible conditions as shown in the following table.

LED State	Operating Condition
Solid Green	Power available to POD and V_{REF} detected.
Solid Amber	Power available to POD but no V_{REF} detected.

Notes:

1. If LED does not turn on, check to make sure that power has been connected to the PC IV either through the mouse/keyboard port, or through the external power connector.

Automatic I/O Voltage Sensing

Although JTAG configuration pins have typically operated at 3.3V or 5.0V, new devices support voltages as low as 1.5V. Voltage levels for Slave-Serial configuration pins follow the respective I/O bank voltage, which can be in the range from 1.5V to 5.0V. Consequently, the PC IV output buffers must be capable of driving at the voltage level expected by the receiving devices. The V_{REF} pin on the target device is used to bias the PC IV output buffers.

A sensing circuit continuously monitors the V_{REF} pin. If V_{REF} drops below 1.3V DC, all output buffers are 3-stated to avoid any possible damage when connected to an non-powered target system.

All pins are protected against continuous shorts to ground or voltages up to 5.5V DC.

IEEE 1284 Cable Specifications

Level 1 compliant host ports are only designed to operate over a maximum cable length of 10 ft. Level 2 compliant host ports will operate over a maximum cable length of 33 ft. PC IV uses a Level 2 compliant cable interface buffer.

For more cable information, see the following web site:
http://www.xilinx.com/support/programr/cables.htm

Signal Integrity Issues

The PC IV uses high slew rate buffers ti drive TCK, TMS, and TDI. Users should pay close attention to proper PWB layout and signal termination to avoid transmission line effects. Signal reflections due to improper termination on the target system, particularly TCK, can result in non-montonic waveforms. Users are encouraged to refer to the "**Signal Integrity**" documentation on the Xilinx web site:

and the Xilinx application note **XAPP361**.

PC IV Operating Characteristics

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply Voltage	5.5	V
T_A	Operating Temperature Range	0° to 70°	C
T_{STG}	Storage Temperature Range	–40° to 85°	C
P_D	Power Dissipation	750	mW
I_{OUT}	DC Output Current (TDI, TCK, TMS, INIT)	±32	mA

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	DC Supply Voltage	External P/S	4.75	5.25	V
V_{REF}	Target Reference Voltage		1.5	5.5	V
I_{CC}	Operating Current		60	100	mA
I_{REF}	Reference Current		6.0	15.0	mA
V_{OH}	High Level Output Voltage	V_{REF} = 3.3V DC, I_{OH} = –4 mA	2.7	-	V
V_{OL}	Low Level Output Voltage	V_{REF} = 3.3V DC, I_{OL} = +4 mA	-	0.36	V
V_{IH}	High Level Input Voltage	V_{REF} > 1.5V	1.2	-	V
V_{IL}	Low Level Input Voltage	V_{REF} > 1.5V	-	0.4	V

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/26/01	1.0	Initial Xilinx release.
11/30/01	1.1	Changed to Advance Product Specification.
01/21/02	1.2	Fixed the links in Table 2.
02/06/02	1.3	Added **Signal Integrity Issues** on page 5.