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RapidIO

Programmable Logic from the INSIDE OUT

Real RapidIO Core Enables Terabit Networks

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One of the major challenges in building terabit-capable systems is improving the performa system interconnect — the speed at which various components such as microprocessors, memory, and peripherals communicate with each other. However, with the RapidIO archite can boost system throughput significantly by eliminating chip-to-chip communication bottle the industry's first RapidIO solution, the Real RapidIO core is the latest in a series of high performance LogiCOREs fully supported through the Xilinx Platform FPGA SystemIO™ sol you can combine the advantages of the Platform FPGA and the RapidIO architecture to buil performance optical networks, gigabit and terabit routers, and network servers. This week, Athavale, the Solution Marketing Manager for System Interfaces Solutions at Xilinx, discuss capabilities of this new core.

Q: What is RapidIO Interconnect? The RapidIO specification defines a technology that can throughputs exceeding 10 Gbps by using high clock rates, LVDS signaling, and source syr clocking. It is a low latency, memory-address based protocol that supports multi-processin scalable, reliable, and transparent to application software.

Q: What are the key features of the new Real RapidIO IP Core? The Real RapidIO Physica Interface, a fixed netlist solution for creating the RapidIO interconnect, is a pre-implemente tested module for the latest, high-density Virtex™-II Platform FPGAs, offering:

- as an 8-bit LVDS port with 64-bit internal data path, 250 MHz clock, and 500 Mbps p pin pair throughput. The Virtex-II FPGAs meet all required electrical and timing para including setup, hold, and clock to output time, as well as AC output drive character stated in the 250 MHz RapidIO AC specification.
- Time-To-Market Advantage — Xilinx Smart-IP™ Technology ensures the highest pe predictability, repeatability, and flexibility in LogiCORE™ designs. By pre-defining th pinout and relative placement of the internal logic, and by controlling critical paths w constraints file to assure a predictable timing result, your product development time significantly reduced.

Q: How is the interoperability of the RapidIO solution ensured? The Real RapidIO core ha verified with v1.4 RapidIO Bus Functional Models provided by the RapidIO Trade Associatic members include Alcatel, Cisco, Ericsson, EMC, IBM, and Nortel. Xilinx has also teamed w Motorola, a founding member of the RapidIO Trade Association, for RapidIO product validat

For more information on the RapidIO solution, see: www.xilinx.com/rapidio.