techXclusives

Current *techXclusive*:

"Get Smart About Reset (Think Local, Not Global)"

(October 3 - 19)

By Ken Chapman

Staff Engineer, Core Applications - Xilinx UK

PREVIOUS *techXclusives*:

Peter Alfke

Director, Applications Engineering, Xilinx San Jose .

Peter Alfke came to the US in 1966, with a German MSEE degree and nine years experience in digital systems and circuit design at LM Ericsson and Litton Industries in Sweden. He has been manager, later director of applications engineering for over 30 years, at Fairchild, Zilog, AMD, and, since 1988, at Xilinx.

He holds thirteen patents, has written many Application Notes, presented at numerous design conferences, and has given many applications-oriented seminars in the US and in Europe. He is an active participant in the best newsgroup for FPGA users, comp.arch.fpga.

Ask questions. Float your great ideas. Give us your suggestions for the next *techXclusive*. Debate and discuss your ideas with other designers and industry experts.

"Choices, Choices, and Options"
(October 30-November 13, 2000)

"Printed Circuit Board Considerations"
(January 15-January 28, 2001)

"Using Leftover Multipliers and Block RAM"
(April 23, 2001 - May 7, 2001)

"Moving Data Across Asynchronous Clock Boundaries"
(July 10-July 24, 2001)

"Asynchronous FIFO in Virtex-II™ FPGAs"
(August 20 - September 5, 2001)

Ken Chapman

Staff Engineer, Core Applications, Xilinx UK

Ken Chapman holds a first class BSc Degree with honours in Electronic and Electrical Engineering from the University of Surrey. Before obtaining his degree, he spent 4 years working in production environments, making precision instruments and working his way through all levels of a

small electronics company. He spent 4 years at Racal Radar Defense Systems combining detailed digital design with all aspects of system integration.

Ken joined the UK division of Xilinx in 1991, and was instrumental in developing innovative methods of implementing DSP functions in the Xilinx devices. He has filed several patents while at Xilinx, including the 'MULT_AND' gate seen in each Virtex™ and Spartan™-II device that has made multipliers and other arithmetic functions smaller and faster.

"Saving Costs with the SRL16E" - Part 1
(November 13-27, 2000)
"Saving Costs with the SRL16E" - Part 2
(November 27-December 11, 2000)
"Saving Costs with the SRL16E" - Part 3
(December 11-27, 2000)

"8x12 Does NOT Equal 12x8: Multiplier Construction"
(January 29-February 12, 2001)

"Digitally Removing a DC Offset
(or 'DSP Without Math?')" - Part 1
(June 6-June 20, 2001)

"Digitally Removing a DC Offset
(or 'DSP Without Math?')" - Part 2
(June 20-July 10, 2001)

"Expanding Virtex-II™ Multipliers"
(July 30 - August 20, 2001)

"Get Smart About Reset (Think Global, Not Local)"
(October 3 - 19, 2001)

Amit Dhir

System Architect, Strategic Applications
Xilinx San Jose

Amit Dhir's primary responsibilities as a Manager in the Strategic Solutions Marketing group at Xilinx include technical and market research, and evangelizing new and emerging markets. He is the author of "The Home Networking Revolution - A Designer's Guide," a book focussed on home networking technologies and components of the consumer and broadband access market. He has published several articles and white papers on topics covering the role for FPGAs in Wireless, Embedded, Telecom, Networking, and Consumer applications, and has presented at several industry conferences and consortiums.

Amit has a BSEE from Purdue University and a MSEE from San Jose State University.

"FPGAs Driving Voice-Data Convergence - Part I"
(May 9 - May 23, 2001)

"FPGAs Driving Voice-Data Convergence - Part II"
(May 23- June 4, 2001)

Austin Lesea

Principal Engineer, Xilinx San Jose

Austin graduated from UC Berkeley in 1974 and 1975 with his BS EECS in Electromagnetic (E&M) Theory and MS EECS in Communications and Information Theory. He has worked in the telecommunications field for 20 years designing optical, microwave, and copper- based transmission systems. He developed SONET/SDH GPS-based Timing Systems for 12 of those years. At Xilinx, Austin is part of the Virtex™-II IC Design Team.

"Signal Integrity Tips and Tricks"
(December 28, 2000 - January 12, 2001)

Andy Miller

Staff Engineer, Xilinx UK

"Colour Space Conversion" - Part 1
(March 12, 2001 - March 26, 2001)
"Colour Space Conversion" - Part 2
(March 26, 2001 - April 9, 2001)