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Using the CoolRunner XPLA3 Timing Model

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All CoolRunner™ XPLA3 CPLDs have a uniform architecture and an identical timing model, making them very easy to use and understand. To determine specific timing details, users need only compare their paths of interest to the architectural diagrams and, using the timing model presented here, perform a simple addition of incremental time delays. This white paper will describe the XPLA3 timing model in great detail and provide examples which illustrate how to use this timing model.

Introduction

A brief overview of the XPLA3 architecture as it pertains to the timing model will be described in the following sections. The XPLA3 architecture is not fully described in this white paper. For more details on the XPLA3 architecture, please refer to white paper **WP105, "CoolRunner XPLA3 CPLD Architecture Overview".**

CoolRunner XPLA3 Architecture

The CoolRunner XPLA3 architecture consists of logic blocks that are interconnected by a routing matrix called the Zero-power Interconnect Array (ZIA). Each logic block contains 16 macrocells. The block diagram for a 64 macrocell device is shown in Figure 1. There are four universal control terms available to all logic blocks in a XPLA3 CPLD: a universal clock (UCLK), a universal reset (URST), a universal preset (UPST), and a universal output enable (UOE). One control term from each logic block is routed to a set of multiplexers that generates the four Universal Control Terms. The Universal Control Terms are then routed to each logic block for use by the macrocells.

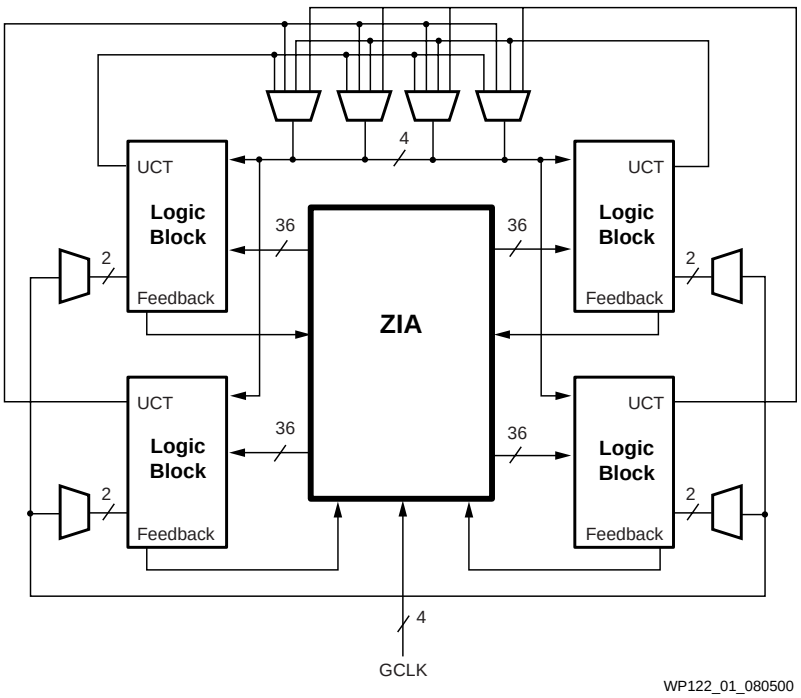

Figure 1: **XPLA3 High-Level Architecture (64 macrocell device shown)**

Each logic block contains a pure PLA array (programmable AND, programmable OR). The PLA array provides a pool of 48 product terms that can be used as macrocell clocks, control terms (reset, preset, clock-enables, or output-enables), or as needed by the 16 macrocells in the logic block. The first eight product terms in the PLA are used to generate eight Local Control Terms (LCT[0:7]). Note that if these product terms are not needed as control terms, they are available for other logic. Local Control Term 7 (LCT7) is routed from the logic block to the universal control term multiplexers.

As seen in Figure 2, both local and universal control terms can be used in the macrocell as the macrocell register clock, reset, and preset functions as well as the output enable

for the output buffer. In addition, Local Control Terms can be used as a hardware clock enable.

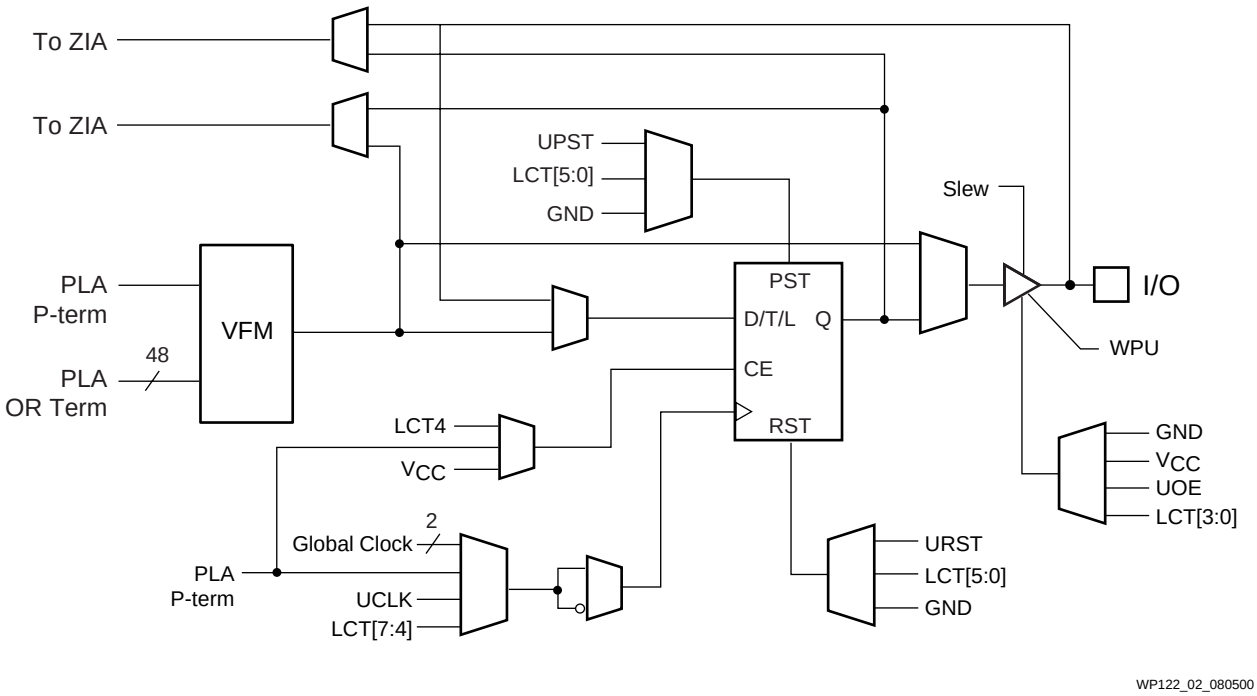

Figure 2: **XPLA3 Macrocell**

Device Timing Overview

External signals arrive at the pins and are delivered through the I/O block to the ZIA. From the ZIA, they are dispatched to the various logic blocks (LBs). As the signals enter the LBs, they incur incremental time delays depending on how the signals are used within the LB. For example, all logic signals must pass through the AND array where they encounter product terms which add a time delay as the signal progresses. Additional time delay may be encountered if the signal passes through a Fold-back NAND gate.

There are additional timing requirements such as setup and clock-to-output times involved with passing signals through a flip-flop. As the signals exit the flip-flops, they either pass to the outside world, through the I/O pins, or are fed back into the ZIA switch matrix for additional logic operations.

Design timing can be manually analyzed as separate signals, each having unique timing parameters that are easily calculated, However, the Xilinx development tools provide a detailed timing report that tallies and summarizes all paths specified by the designer. The timing report is based on the model described here and is a convenient text based mechanism for isolating and displaying timing relationships.

Timing Model

The timing model, shown in Figure 3, is used by the Xilinx development software which provides complete fitters for the CoolRunner XPLA3 family as well as timing models for simulation and detailed static timing reports.

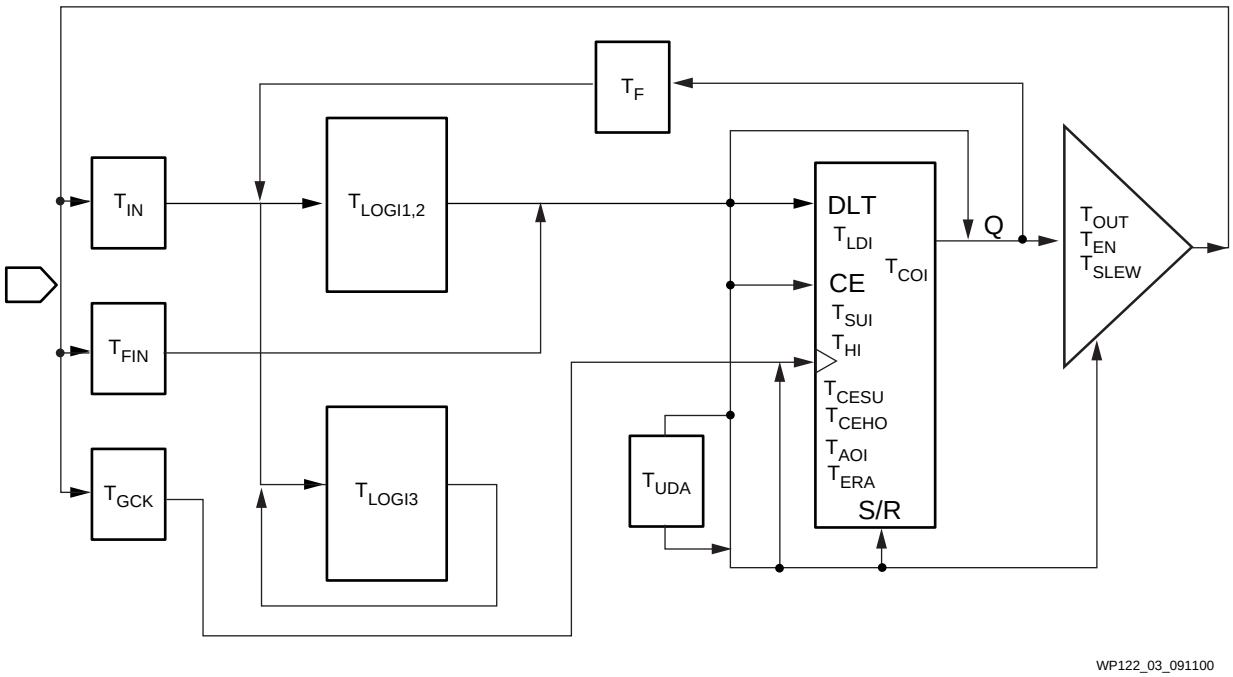

Figure 3: **XPLA3 Detailed Timing Model**

The timing model shown in Figure 3 resembles the XPLA3 macrocell with additional time delays included to account for the ZIA switch matrix and I/O buffers. As signals progress through an XPLA3 device, they encounter each of these delays which are tallied to arrive at a cumulative time delay for that signal. Table 1 provides a detailed definition of each parameter contained in Figure 3. The exact values for each device can be obtained from the specific data sheets.

Table 1: **XPLA3 Internal Timing Parameters**

Parameter	Description
Buffer Delays	
T_{IN}	Input buffer delay
T_{FIN}	Fast input buffer delay (input registers)
T_{GCK}	Global Clock buffer delay
T_{OUT}	Output buffer delay
T_{EN}	Output buffer enable / disable delay
Internal Register and Combinatorial Delays	
T_{LDI}	Latch transparent delay
T_{SUI}	Register setup time
T_{HI}	Register hold time
T_{CESUI}	Register clock enable setup time

Table 1: **XPLA3 Internal Timing Parameters *(Continued)***

Parameter	Description
T_{CEHO}	Register clock enable hold time
T_{COI}	Register clock to output delay
T_{AOI}	Register async. S/R to output delay
T_{ERA}	Register async. recovery
T_{LOGI1}	Internal logic delay (single p-term)
T_{LOGI2}	Internal logic delay (PLA OR term)
Feedback Delays	
T_F	ZIA delay
Time Delays	
T_{LOGI3}	Fold-back NAND delay
T_{UDA}	Universal delay
T_{SLEW}	Slew rate limited delay

External Timing Parameters

Table 2 shows how key external timing parameters are derived from the internal timing parameters.

Table 2: **Expressions for Key Timing Parameters Derived from Table 1**

Parameter	Description	Equation
T_{PD1}	Propagation delay time (single p-term)	$T_{IN} + T_{LOGI1} + T_{OUT}$
T_{PD2}	Propagation delay time (OR array)	$T_{IN} + T_{LOGI2} + T_{OUT}$
T_{CO}	Clock to output (global synchronous pin clock)	$T_{GCK} + T_{COI} + T_{OUT}$
T_{SUF}	Setup time fast	$T_{FIN} + T_{SUI} - T_{GCK}$
T_{SU1}	Setup time (Single product term)	$T_{IN} + T_{LOGI1*} + T_{SUI} - T_{GCK}$
T_{SU2}	Setup time (OR array)	$T_{IN} + T_{LOGI2*} + T_{SUI} - T_{GCK}$
T_H	Hold time	$T_{HI} + T_{GCK} - T_{IN} - T_{LOGI*}$
T_{OE}	OE to output enabled	$T_{UDA} + T_{IN} + T_{LOGI*} + T_{EN}$
T_{OD}	OE to output disabled	$T_{UDA} + T_{IN} + T_{LOGI*} + T_{EN}$
f_{SYSTEM}	Maximum system frequency	$1/(T_{SUI} + T_{COI} + T_F + T_{LOGI*})$
T_{PCO}	P-term clock to output	$T_{IN} + T_{LOGI*} + T_{COI} + T_{OUT}$
T_{PSU}	P-term clock setup time	$T_{IN} + T_{LOGI*} + T_{SUI} - (T_{IN} + T_{LOGI*})$
T_{PH}	P-term clock hold	$T_{HI} + (T_{IN} + T_{LOGI*}) - T_{IN} - T_{LOGI*}$
T_{POE}	P-term OE to output enabled	$T_{IN} + T_{LOGI*} + T_{EN}$
T_{POD}	P-term OE to output disabled	$T_{IN} + T_{LOGI*} + T_{EN}$
T_{PAO}	P-term set/reset to output valid	$T_{IN} + T_{LOGI*} + T_{AOI} + T_{OUT}$

where:

$T_{LOGI*} = T_{LOGI1}$ if a single PT is used.

$T_{LOGI*} = T_{LOGI2}$ if 2 to 48 PTs are used.

Please note that these times will change if multiple feedback passes (internal nodes) are used.

Timing Calculation Examples

This section gives a few examples of how the device timing is calculated. These calculations are automatically done for the user by software development tools but examples are provided here to help the user better understand how the software calculates device timing. Please note these examples do not cover every possible case.

Propagation Delay

For example, the T_{PD1} is the sum of the input buffer time delay (T_{IN}), the logic time delay (T_{LOGI1}), and the output buffer time delay (T_{OUT}), as shown in Figure 4. Note that the input buffer delay is combined with the ZIA time delay since the entering signal passes through the ZIA switch matrix.

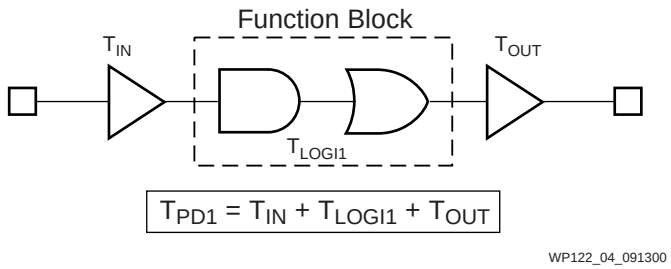

Figure 4: **T_{PD1} with a Single Product Term**

Figure 5 shows a variation on the simple T_{PD1} example with the addition of more product terms. The time delay from input A is slightly altered by replacing the value T_{PD1} with T_{PD2} which accounts for the additional product terms. The XPLA3 timing parameter, T_{PD2}, is the same regardless if 2 or up to 48 product terms are used.

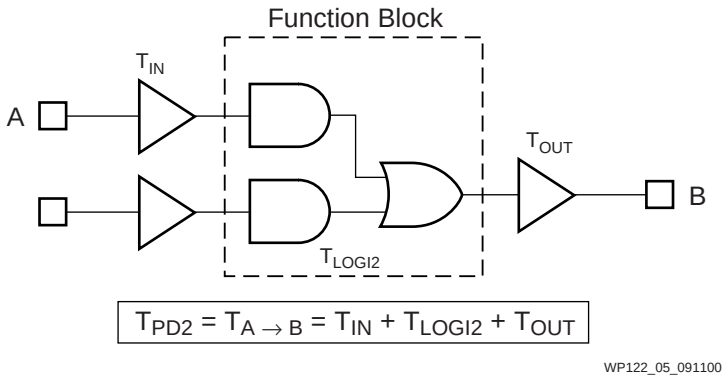

Figure 5: **T_{PD2} with Two to 48 Product Terms**

Figure 6 shows the result of supplementing single pass logic with an additional pass through another macrocell. In this case, there is a single pass through the input and

output buffers, a pass through the macrocell logic, a pass through the feedback path, and an additional pass through the macrocell logic.

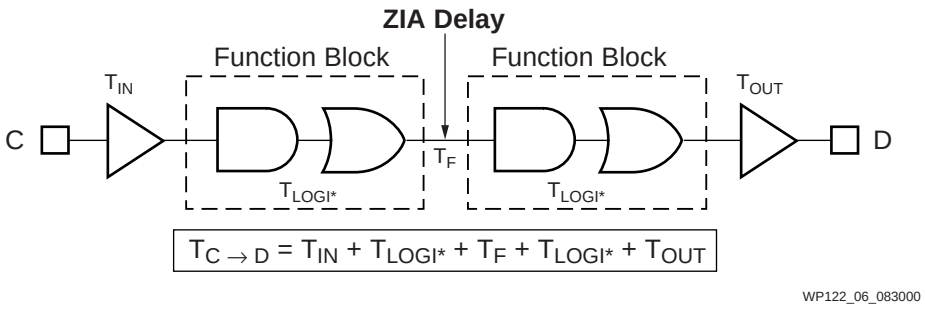

Figure 6: **T_{PD} with Two-Pass Logic**

Clocking

Figure 7 shows the situation for a simple flip-flop clocked by a Global Synchronous Clock signal (GCLK). The expressions for T_{CO}, T_H, and T_{SU1} or T_{SU2} in Figure 7 are valid for this arrangement.

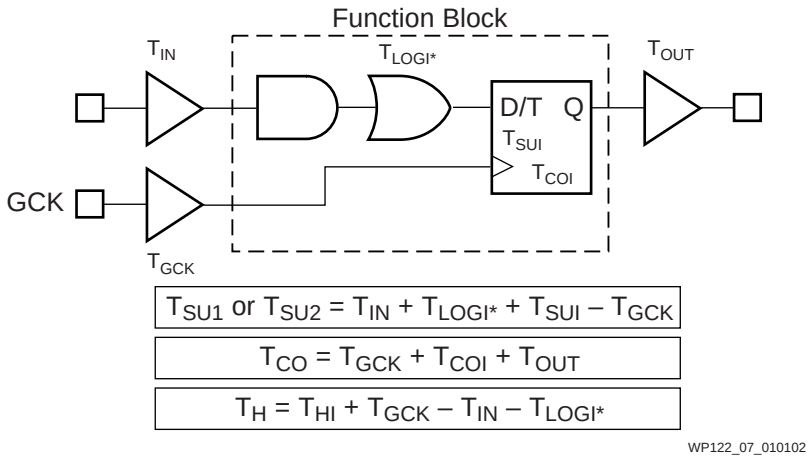

Figure 7: **Simple Flip-Flop Path**

Figure 8 shows the addition of another layer of macrocell logic into the situation described in Figure 7. The T_{CO} expression remains the same, but the T_{SU1} or T_{SU2} and T_H expressions are increased and decreased, respectively, by another $T_{LOGI*} + T_F$.

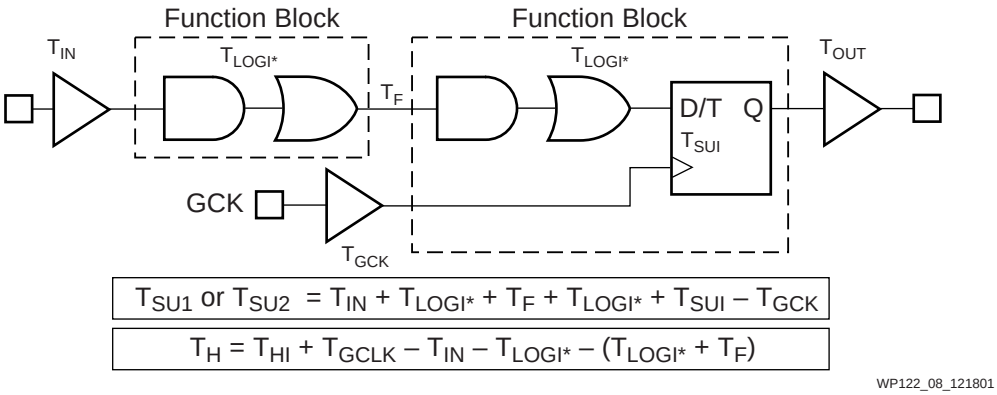

Figure 8: **Flip-Flop with Two-Pass Logic**

Figure 9 shows two flip-flops connected by a single level of logic, clocked by a global clock. The T_{SU1} or T_{SU2} and T_H for flip-flop A are identical to that of Figure 7.

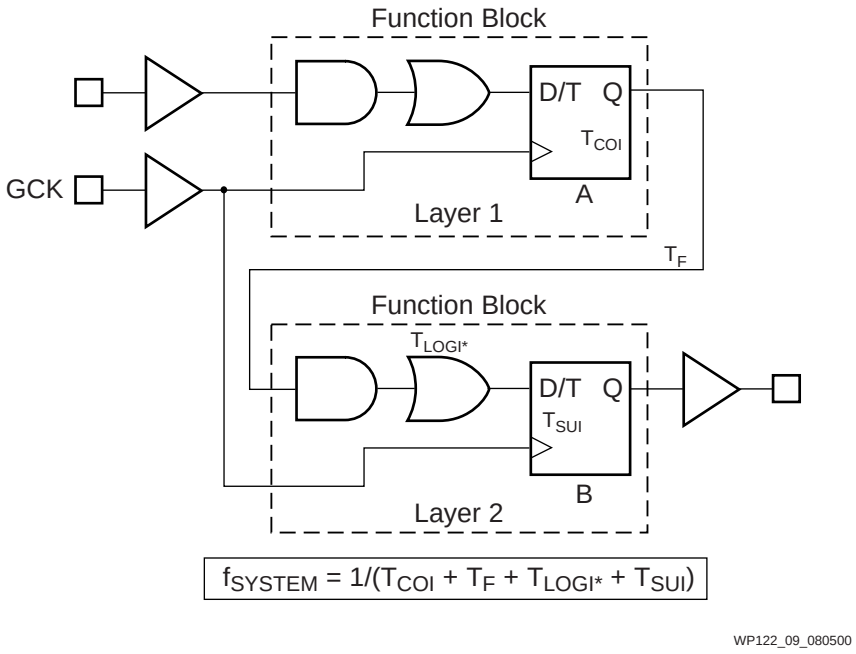

Figure 9: **Multiple Flip-Flops with Single Level Logic**

Figure 10 shows a single flip-flop with a product term clock. This arrangement differs from Figure 7 only in that the clock input comes from a product term clock. The entry

for T_{PCO} in Figure 10 reflects this variation. The timing for T_{PSU} and T_{PH} is calculated using the product term clock timing parameters.

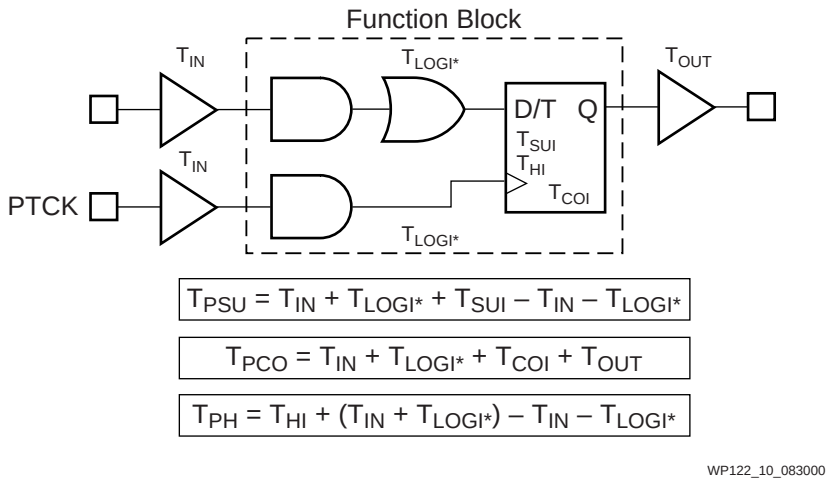

Figure 10: **Single Flip-Flop with Product Term Clock**

Clock Enable

XPLA3 CPLDs provide a flip-flop clock enable. CE has both setup (T_{CESU}) and hold (T_{CEHO}) time requirements.

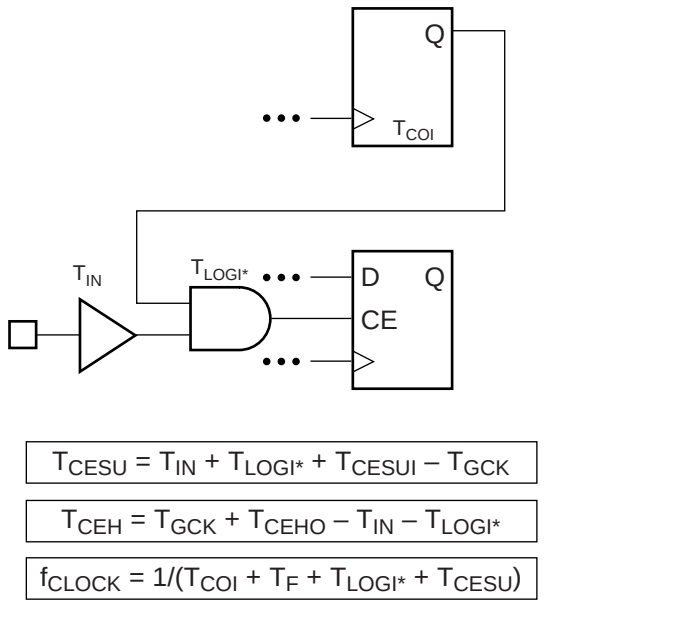

Figure 11: **Flip-Flop with Clock Enable**

Figure 12 shows how CE, which is driven by a product term, impacts f_{MAX}. Any additional feedback delays are added to the T_{SU1} or T_{SU2} and/or f_{CLOCK} calculations, which may impact system clock frequency.

Output Enable

Figure 12 shows the timing for driving valid data onto a bus with respect to a rising clock edge, a common configuration that occurs in high speed buses. This is sometimes called T_{VALID}.

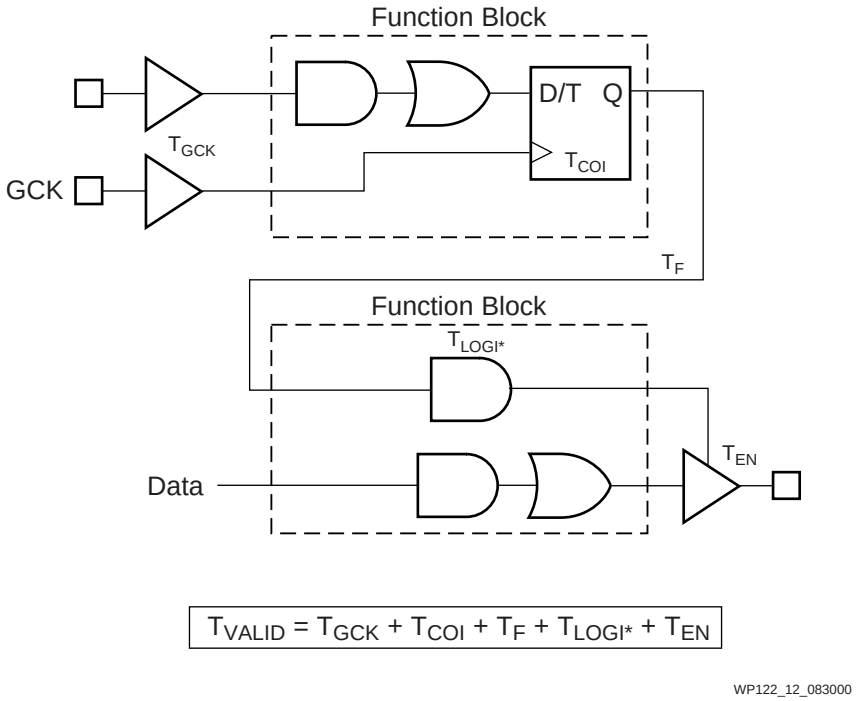

Figure 12: **Flip-Flop-Controlled Output Enable**

This set of examples should be sufficient to describe a large number of design configurations, and other examples can easily be derived from the timing model. For manual calculations, other timing delays such as T_{SLEW} and T_{LOGI3} are easily added to the overall timing as required.

Conclusion

After reading the white paper, the user should understand how the timing parameters are calculated from the CoolRunner XPLA3 timing model. This will allow the user a better understanding of how to maximize their system performance.

Revision History

The following table shows the revision history for this document.

Date	Version #	Revision
09/13/00	1.0	Initial Xilinx release.
01/07/02	1.1	Changed T_{SU} in Table 2 to T_{SU1} and added T_{SU2}, updated text and Figures 7 and 8. Updated format.