Metastability Recovery in Xilinx FPGAs

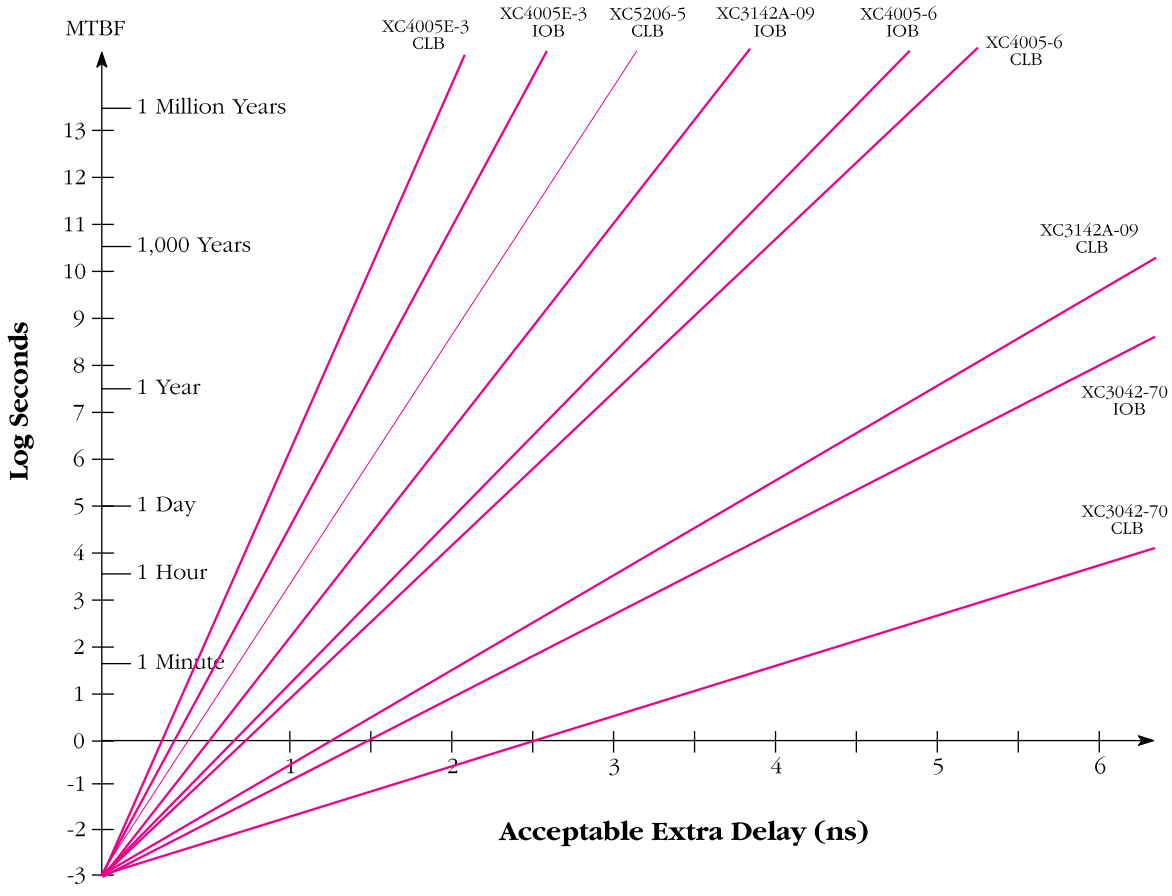
Whenever a clocked flip-flop synchronizes an asynchronous input, there is a small probability that the flip-flop output will exhibit an unpredictable delay. This happens when the input transition not only violates the setup and hold-time specifications, but actually occurs within the tiny timing window where the flip-flop accepts the new input. Under these circumstances, the flip-flop can enter a symmetrically-balanced transitory state, called a metastable state.

While the slightest deviation from perfect balance will cause the output to revert to one of its two stable states, the delay in doing so depends not only on the gain-bandwidth product of the circuit, but also on how perfect the balance was and on the noise level within the circuit; the delay can, therefore, only be described in statistical terms. The problem for the system designer is not the illegal logic level in the balanced state (it's easy enough to translate that arbitrarily to either a 0 or a 1), but the unpredictable timing of the final change to a valid logic state. If the metastable flip-flop drives two destinations with differing path delays, one destination might clock in the final data state while the other does not.

Metastability Measurements

Recently, the metastable delays of four different Xilinx FPGA devices were measured: two cutting-edge devices using 0.5 micron, 3-layer-metal technology, the

Figure: *Mean Time Between Failure for various IOB and CLB flip-flop outputs when synchronizing a 1 MHz asynchronous input with a 10 MHz clock.*



XC4005E-3 and the XC3142A-09; and, for comparison purposes, two older-technology devices, the XC4005-6 and the XC3042-70. In each device, two different implementations test the IOB and CLB flip-flops. The XC5200-5 CLB flip-flop was also tested. (There is no IOB flip-flop in XC5200 architecture.)

The XC4000E amd XC4000 devices showed little difference between IOB and CLB behavior, but in the XC3000-series devices, the IOB flip-flops showed dramatically better metastable performance than the CLB flip-flops. This difference can be traced to subtle differences in circuit design and layout and will guide us to further improvements in metastable performance of future designs.

Metastable measurement results are listed in the table and plotted in the figure. The results for XC4000E-3 IOB and CLB flip-flops, XC5200-5 CLB flip-flops and XC3100A-09 IOB flip-flops are outstanding, far superior to most metastability data published anywhere else. When granted 2 or 3 ns of extra settling delay, these devices come close to eliminating the problems caused by metastability, since their mean-time-between-failure exceeds millions of years. The older-technology devices are slightly less impressive, but still show very acceptable performance, especially the IOB input flip-flops that are normally used to synchronize asynchronous input signals.

Metastability Calculations

The Mean Time Between Failures (MTBF) can only be defined statistically. It is inversely proportional to the product of the two frequencies involved, the clock frequency and the average frequency of the asynchronous data changes, provided that these two frequencies are independent and have no correlation. The generally accepted equation for MTBF is

$$\mathbf{MTBF} = \frac{e^{K2 \times t}}{F1 \times F2 \times K1}$$

K2 is an exponent that describes the speed with which the metastable condition is being resolved.

K1 represents the metastability-catching setup time window that describes the likelihood of going metastable

F1 is the frequency of the asynchronous data input

F2 is the flip-flop clock frequency

t is the settling time

K2 is an indication of the gain-bandwidth product in the feedback path of the master latch in the flip-flop. A small decrease in the time constant 1/K2 results in an enormous improvement in MTBF.

With F1 = 1 MHz, F2 = 10 MHz and K1 = 0.1 ns,

$$\mathbf{MTBF\ (in\ seconds)} = 10^{-3} \times e^{K2 \times t}$$

The values of K2 under these conditions — expressed as 1/K2 in the table — were experimentally derived *(as described in the "1996 Programmable Logic Data Book," page 14-41).*

The MTBF under other operating conditions can be estimated using the data in the diagram. Simply divide the appropriate MTBF from the diagram by the product of the two relative frequencies. For example, for a 10 MHz asynchronous input synchronized by a 40 MHz clock, the MTBF is 40 times shorter than plotted, and for a 50 KHz signal and a 1 MHz clock, the MTBF is 200 times longer than plotted here. ◆

Metastability Measurement Results

Tested Flip-Flop		Value of 1/K2 in picoseconds
XC4005E-3	CLB	52
	IOB	62
XC4005-6	CLB	127
	IOB	118
XC3142A-09	CLB	208
	IOB	79
XC3042-70	CLB	385
	IOB	238
XC5200-5	CLB	73