"A Leap Forward"

Signaal Evaluates the Xilinx Alliance Series Software Tools

Hollandse Signaalapparaten B.V. (Signaal), a subsidiary of Thomson-CSF, recently performed an evaluation of the new Alliance Series software. The design was for an interface between an MC68360 CPU and a SHARC bus running at a clock frequency of 25 MHz, and was implemented in an XC4010E-4PQ208 FPGA. About 70% of the CLBs and 80% of the IOBs were used. All I/O pins were locked to enable concurrent design of the PCB layout.

The evaluation used the Synopsys FPGA Compiler for synthesis, and the Cadence Leapfrog simulator for behavioral (RTL), functional, and timing simulation. However, any synthesis tool and VITAL-compliant simulator could have been used because all interfaces are based on standard formats such as VHDL, SDF, and EDIF. *See "design flow" at right.*

The Customer Evaluation Report

Jaap Mol of Signaal wrote, "The new Alliance Series software is a leap forward; improvements have been made in all areas." His report included many other key insights:

Usability of the Software

"The usability has been improved by the new GUI. It is intuitive and allows for better control, which is especially important for the first time user of the tools."

Controllability of the Tools

"The controllability has been improved using the flow engine and user-definable templates. Design constraints can be specified during synthesis (netlist constraints) and during place and route (user and physical constraints). Constraint-driven place and route is essential for timing-critical, high-density designs."

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Version and Revision Control

"Version and revision control capability have proven to be very useful in performing design trade-offs. The best possible solution for the design can be selected from implemented versions and revisions. This is especially useful when using Xilinx FPGA technology to do rapid prototyping of a system. The Design Manager offers the capability for doing version and revision control on designs. In the Design Manager a design is referred to as a project. If there have been changes to a logic design (e.g. the netlist), this is referred to as a new version of the design. If the design is mapped into another device, package, or speed-grade, this can be referred to as a new revision. This way, the user can easily make trade-offs, without losing previous results."

Report Browsing

"During implementation of the design, many reports are generated. For instance, there are reports concerning timing, place and route, and pad assignments."

On-Line Help

"The on-line help is available from within the design manager. The help function is based on Windows Hyperhelp, has a search function, and is easy-to-use."

The Signaal Design Flow:

- A VHDL (RTL) model was verified using the VHDL simulator. This model also functioned as an input for logic synthesis.
- The synthesis tool translated the VHDL model to gates. (The required synthesis libraries are provided by Xilinx or the synthesis tool vendor.)
- An EDIF netlist was generated during synthesis, containing the connectivity between Xilinx primitives. This netlist was later transferred to the place and route software.
- Optionally, functional (pre-layout) simulation could be performed using the Xilinx VITAL library, to verify the correctness of the synthesis process before proceeding with place and route.
- The EDIF netlist was processed by the place and route software. After place and route was completed, a VHDL netlist and SDF timing information were generated. These were used for Timing Simulation, once again making use of the Xilinx VITAL library. In addition, static timing analysis was performed during synthesis and during place and route.

Interface Formats to Other Tools

"The interface to and from Xilinx tools is dramatically improved by the move to standard formats like EDIF, VHDL, and SDF. This was the major reason why the interfaces from the synthesizer and simulator did not cause any major problems. The availability of a

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VITAL-compliant VHDL library makes it possible to use one testbench, one simulator, and one language for simulation on any level of abstraction.

"Apart from the tools, which are called from the flow engine, the following functions are also available:

- "The **timing analyzer** provides a timing analysis of specific paths in the design, and helps to verify that the timing constraints are met by the place and route tools.
- "The **epic design editor** can be used to manually place and route any or all parts of the design.
- "The **hardware debugger** provides an interface to the XChecker cable, which can be used for reconfiguring an FPGA, while prototyping the system.
- "The **PROM file formatter** generates one or more PROM files in a suitable format for an EPROM programmer. It can merge multiple bitstreams into the resulting PROM files. Both serial and byte-wide PROMs are supported.

"It is quite visible that Xilinx has put a lot of effort into the development of this release. The new tools are intuitive, have good controllability, and support industry standards. The support of industry standards makes the interface to third-party EDA vendors easy and seamless. The tools helped cut down our design time significantly, which translates into reduced time-to-market. We hope Xilinx will continue investing resources in this direction." ◆