Designing With Large, Fast Programmable Logic Devices

The FPGA industry has achieved a major milestone with the availability of extremely large, high-performance devices. To successfully take advantage of the design opportunities presented by these new FPGAs, today's designers must be armed with the latest tools and techniques.

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Historically, application-specific chips comprised a relatively small portion of an electronic system. Standard function chips, such as bus interfaces, clock controllers, memory, device controllers, and microprocessors, made up the majority of the design. However, improvements in chip capacity, combined with the decreasing end-product form factor, is pushing us to much higher levels of integration.

Xilinx is a leading innovator in high-density, high-performance FPGAs. Customers have voiced a keen interest in the Virtex family of FPGAs, not only for their speed and density, but also for the new architectural features. On-board RAMs give you greater integration and the incentive to pull more of the system function onto the chip, while the wide variety of I/O types helps to integrate the chip into your system, eliminating external level translators.

Until recently, this integration capability was only available to ASIC designers. However, system-on-a-chip design opportunities have increased dramatically with the introduction of these affordable Virtex FPGAs possessing the density, architectural features, and software support you need.

Applications

Depending on your end application, you can plan to design-in these chips in a variety of ways. You can push the bulk of the system functionality onto a single chip, or divide the system according to flexibility requirements, split between an ASIC and an FPGA. For example, an ATM system may have a very complex 50K- to 100K-gate control logic requirement, prone to design error and specification change. This portion is best mapped into an FPGA.

Industries where standards are in flux are also prime candidates for high-density, high-performance FPGAs, where there is a need for last minute product customization. The bulk of the system (a consumer graphics product for example) can be realized in masked silicon, while an FPGA customizes it for a variety of different market segments, perhaps starting with PCI interfaces and moving to USB or AGP.

Design Techniques and Technologies

Silicon advances are not the only factor enabling systems-on-a-chip. Taking advantage of the increased chip capacity within the real world constraints of product market windows and performance specifications requires a whole host of supporting technologies, such as those available from Synopsys. Some key design techniques for high gate count, high-speed FPGA designs are:

- Hardware Design Languages (HDLs) and synthesis above 10,000 gates for productivity design re-use.
- Optimizing the full design flow, including FPGA place and route and requirements for compatibility with the ASIC design flow.
- Use of timing analysis to pinpoint critical timing issues early.
- Precise design methodologies and hierarchical synthesis support for team design.

Summary

The age of system-on-a-programmable-chip has become a reality, and the Virtex family from Xilinx is a leading architecture in that market. The Virtex architecture contains many powerful features, which lend themselves to smaller, faster systems. The Synopsys and Xilinx R&D teams continue to work closely together to develop a combined solution of powerful design tools, intellectual property, and high-density, high-performance FPGAs to bring you unprecedented opportunities. Σ

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