CPLD Fitter Shootout:

Xilinx 1.5 *versus* Altera 9.01

In a recent benchmark study we compared the "push button" results for Xilinx implementation technology v1.5 versus Altera MAX+PLUS II v9.01. Take a look for yourself; the results are quite compelling.

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Xilinx recently completed an in-depth study, comparing our latest v1.5 implementation tools with Altera's latest release (v9.01). The results prove that the Xilinx solution, along with the XC9500 and XC9500XL device families, is the obvious winner over Altera's MAX7000S/A/AE CPLD offering.

Synopsys FPGA Express v2.1.3 was used for design synthesis. Only defaults were used during the implementation phase; no additional "timing driven" options or constraints were applied. Two separate implementation runs were created per design with the Xilinx tools: one when optimizing for area, the other when optimizing for speed. This required us to select the "speed" or "area" template in the Xilinx tools. Altera does not provide implementation templates in their tools. The following implementation results were recorded for each design run:

- Device targeted (part, package, and speed grade are selected automatically by both the Xilinx and Altera tools for a specified device family).
- Number of macrocells used.
- Number of product terms used.
- Main system clock frequency (Tcyc), in megahertz (MHz).
- Propagation delay (Tpd), in nanoseconds (ns).

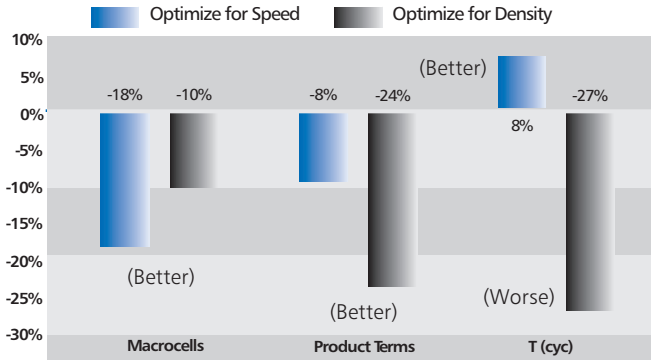
The entire process was performed twice: once to compare the results of targeting the 5V CPLD device families (XC9500 vs. MAX7000S), and again to compare the results of the 3.3V CPLD device families (XC9500XL vs. MAX7000A/AE).

Design Suite - The design suite consists of 50 HDL Designs, 25 of which are Verilog and the other 25 are VHDL. Six of the designs are control designs to test for explicit results while the remaining 44 designs are from customers. The size of the designs range from 10 to 250 macrocells in density, with the design size distribution evenly split above and below 70 macrocells.

Test Platform - Pentium 166MHz, 80MB RAM, Windows NT 4.0, Xilinx v1.5 software, Altera MAX+PLUS II V9.01 software.

Benchmark Results – 5V CPLDs

Xilinx XC9500 vs. Altera MAX 7000S Overall Results

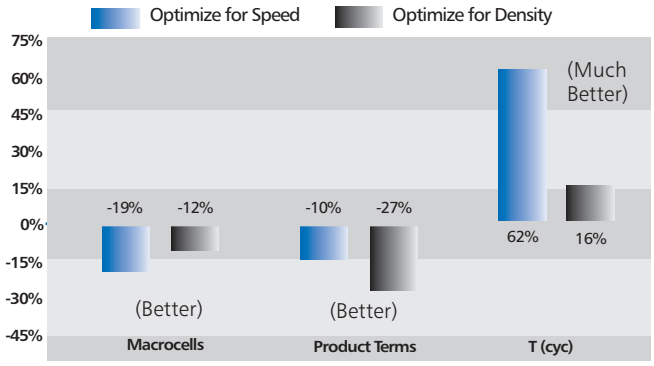


NOTES: Altera MAX+Plus II v9.01 vs. Xilinx v1.5
Percentage based on normalized Altera results.

Figure 1

Benchmark Results – 3.3V CPLDs

Xilinx XC9500XL vs. Altera MAX 7000A/AE Overall Results



NOTES: Altera MAX+Plus II v9.01 vs. Xilinx v1.5
Percentage based on normalized Altera results.

Figure 2

Results - As shown in **Figure 1**, XC9500 CPLDs use 18% fewer macrocells, 9% fewer product terms, and achieve an 8% faster clock frequency than Altera MAX7000S devices. As shown in **Figure 2**, XC9500XL CPLDs use 19% fewer macrocells and 10% fewer product terms, and achieve an impressive 62% faster system performance than Altera's MAX7000A/AE products.

Xilinx CPLD Implementation Technology for v1.5

The dramatic difference in performance demonstrated by these benchmark studies is the result of a number of important enhancements to the Xilinx Alliance Series™ and Foundation Series™ 1.5 software that improve CPLD design entry and implementation capabilities.

Design Entry Enhancements include:

- **Automatic Device Selection:** V1.5 now allows automatic CPLD device selection via either the Alliance Series Design Manager or the Foundation Series Project Manager. Both options will choose an implementation based on device, package, speed grade, or any combination. By default, the CPLD implementation tools will choose the smallest die and the smallest package with the fastest speed grade available.
- **Implementation Templates**: Both the Alliance and Foundation Series Implementation tools will allow you to use pre-defined Implementation Templates. These templates, "Optimize for Speed" and "Optimize for Density," give you an easy way of targeting your design to best suit your application.

When you first invoke the implementation tools, the default option is set to "Optimize for Speed." This template will attempt to fit a design with a bias towards the fastest system clock speed. As always, if a specific clock frequency is desired, it is best to attach a specific "timespec" to the design. This can be accomplished several ways: using the new Constraints Editor, a user constraints file (UCF), schematic symbol or attribute, or through various entry mechanisms within third-party Synthesis tools, such as Synopsys Express, Synplicity Synplify, and Exemplar Leonardo.

Fitter Enhancements Since v1.4 Software

The fitter is the backend software that places and routes your design, and then converts your design to the information and control signals that are necessary for downloading a CPLD programming file. Enhancements include:

- **35% Runtime Reduction** - The v1.5 CPLD implementation tools are now averaging 35% faster speeds than the previous v1.4 tools. This is best represented in designs that are over 108 macrocells. Smaller designs below 72 macrocells improved anywhere from 10% to 50%, depending on logic complexity.
- **15% Average Improvement in Silicon Performance through Software** - System clock speeds have improved 10% to 20% for designs placed in the same device speed grade.
- **Algorithmic Enhancements** - Improvements were made to the multi-level logic optimization algorithm, which improves logic timing and density. Xilinx also introduced a product term collapsing look-ahead feature that significantly reduces the number of product terms required for a given logic function, thus achieving higher system clock frequencies, lower logic level delays, and faster runtimes.

Summary

The results are clear. The combination of the Xilinx version 1.5 implementation technology along with the XC9000 series FPGAs produce superior results over Altera. The Xilinx software consistently uses fewer device resources, chooses a smaller device, and produces devices with shorter delays.