HOTLINE Q&A

by The Xilinx Hotline Staff

Q: Can the TAP (JTAG) pins of a Virtex device be set to SelectI/O standards other than LVTTL?

The TAP pins of a Virtex device cannot be changed. They always use the LVTTL SelectI/O standard.

Q: Can the TAP pins of a Virtex device be used as regular I/O?

The TAP pins of a Virtex device are fully dedicated boundary-scan pins. They cannot be used as regular I/O.

Q: When performing a functional simulation of a Virtex BlockRAM with VerilogXL, the following timing violation is reported by VerilogXL on the BlockRAM. What does this timing violation mean?

```
xxx: Timing violation in top.U1
 $recovery(posedge CLKB: 800, posedge CLKA: 800,
 1.0: 10);
```

The UNISIM Virtex BlockRAM Verilog model in Alliance Series 1.5i incorrectly models the relationship between the BlockRAM clocks. It does not allow both clocks on a BlockRAM to change at the same time. This is not accurate behavior in the case of a read.

There are two workarounds to this problem. The first workaround is to not let both clocks of the BlockRAM change at the same time, in functional simulation. This has the benefit of detecting a possible simultaneous write from both ports. Another workaround is to remove the $recovery directive from the UNISIM BlockRAM Verilog simulation model. This workaround is potentially dangerous because the illegal operation of performing a simultaneous write to the same location will not be flagged. This incorrect behavior will be fixed in an upcoming patch of the 1.5 software.

Q: How do you turn on the Virtex boundary-scan feature? Is there a Virtex boundary-scan symbol that must be instantiated?

The Virtex boundary-scan feature is always active. Nothing needs to be done to turn this feature on.

Q: What does the following error message mean if a Virtex design is compiled with FPGA Compiler I?

```
The target library does not contain all required gates.
Either a NOR, or an AND and an OR gate(two-input)
 is required for mapping. (OPT-102)
```

This message means that the replace_fpga command was used to compile a Virtex design with FPGA Compiler I. The command replace_fpga does not apply when compiling a Virtex design with FPGA Compiler I.

Q: What are the restrictions in using the MUXF6 in Virtex?

The data inputs of the MUXF6 must be connected to the output of MUXF5s.

Q: How do you place an external clock on one of the Virtex global clock nets?

Connect the top-level port in your HDL design to the input of an IBUFG. Next, connect the output of the IBUFG to a BUFG. The output of the BUFG will use the Virtex dedicated clock resources.

Q: Can A TNM be applied to a Virtex shift register LUT?

A TNM can be applied to a Virtex shift register LUT (SRL). Additionally, a Virtex shift register LUT is considered a part of the FFS timegroup. This means that if a constraint file has a TNM that applies to all FFSs in a design that the TNM will apply to all flip-flops and shift register LUTs. The **TNM=FFS:designregisters** attribute would place the TNM 'designregisters' on all flip-flops and shift register LUTs.