Third-Party Developers Deliver First Cores for Virtex FPGAs

by Mike Seither, Director of Public Relations, Xilinx, mike.seither@xilinx.com

New Virtex system-level architecture yields an immediate boost in performance.

Xilinx recently announced the availability of the first wave of third-party software cores that support the new Virtex FPGA family. The cores are available today from partners in the Xilinx AllianceCORE® program and include predefined networking, communications, encryption, and microprocessor peripheral functions.

"The Virtex family is enjoying tremendous market acceptance," said Dennis Segers, vice president of FPGA development and general manager of the High End FPGA Business Unit at Xilinx. "For the first time, customers have access to FPGAs with system-level features and up to one million system gates. This is fueling the demand for cores, which play a critical part in the success of large designs. More of our AllianceCORE partners are recognizing this opportunity, and they are choosing the Virtex family as the primary platform for developing new intellectual property."

AllianceCORE partners report that cores previously designed for Xilinx XC4000 FPGA devices operate 25 to 30 percent faster when converted to run on Virtex devices. All of the new Virtex FPGA cores have been certified to ensure that they work within the Xilinx software design flow.

"The results we are seeing on Virtex FPGAs are nothing short of extraordinary," said James Doherty, managing director of Integrated Silicon Systems (ISS). "Our first run of the ISS-designed DVB Reed-Solomon cores in Virtex devices resulted in an immediate performance improvement of about 28 percent. We expect to see even greater gains in performance by better leveraging some of the system-level features available in Virtex FPGAs."

"The Virtex family features a revolutionary FPGA architecture that is unmatched in the industry," said Timothy Smith, managing director of Memec Design Services of Mesa, Arizona (www.memecdesign.com). "It allows us to consider the development of FPGA cores that were not possible before."

The new cores for Virtex FPGAs available now from AllianceCORE partners include:

- **CAST, Inc**. of Pomona, New York, (www.cast-inc.com) is supplying the C2910A micro-program controller, the C2901 bit-slice unit, the C_UART compact universal asynchronous receiver-transmitter (UART), and the C8259A programmable interrupt controller. New from CAST is the X-DES cryptoprocessor core.
- **CoreEl MicroSystems** of Fremont, California, (www.coreel.com) is supplying a new UTOPIA slave interface and a 10/100 Ethernet media access controller (MAC) core.
- **Integrated Silicon Systems** of Belfast, Northern Ireland, (www.iss-dsp.com) is supplying Reed Solomon encoder and decoder cores.
- **Memec Design Services** is supplying their Reed Solomon encoder core, a new IIC master and slave interface, and Reed Solomon decoder cores.
- **Virtual IP Group** of Santa Clara, California, (www.virtualipgroup.com) is supplying the M8254 timer/counter and M8255 programmable peripheral interface cores.

Virtex Architecture Improves Core Performance

The Virtex family was developed to address system-level design on an FPGA. As a result, the combination of the device architecture and development software greatly simplify the process of designing and using cores. Third-party core providers experience improved performance with less need to optimize for the FPGA architecture. "The Virtex architecture is a natural for implementing IP," said Newton Abdalla, president of CAST, Inc. "The capabilities it provides to support system-on-a-FPGA design are beyond anything that is available in the market today."

All cores are available for purchase today directly from the AllianceCORE partners in either Xilinx optimized netlist or source code formats. Datasheets for each core can be found on the Xilinx website at www.xilinx.com. Σ