

Competitive Overview

Virtex Series FPGA Competitive Cross Reference



Virtex™-E - 1.8V Virtex Series Key Features: Density/Performance, SelectRAM+™, SelectI/O™, DLLs, SelectLINK™

Devices	Package	Package I/O	Logic Gates	Typical Gate Range	Flip-Flops*	Output Drive (mA)	Maximum RAM Bits	Maximum Device I/O	Logic Cells
XCV50E	CS144	94	21K	20K-56K	2064	2/24	80K	176	1728
	PQ240	158							
	FG256	176							
EP20K60E							32K	204	2560
XCV100E	CS144	94	32K	30K-95K	2988	2/24	80K	176	2700
	PQ240	158							
	FG256	176							
EP20K100E							53K	252	4160
XCV200E	CS144	94	64K	60K-200K	5556	2/24	128K	284	5292
	PQ240	158							
	FG256	176							
	FG456	284							
EP20K160E							81K	316	6400
XCV300E	PQ240	158	83K	80K-400K	7116	2/24	224K	316	6912
	FG256	176							
	BG432	316							
	FG456	312							
EP20K200E							106K	382	8320
XCV400E	PQ240	158	130K	130K-560K	10812	2/24	310K	404	10800
	BG432	316							
	FG676	404							
EP20K300E							147K	408	11520
XCV600E	HQ240	158	187K	185K-980K	15360	2/24	504K	512	15552
	BG432	316							
	FG676	444							
	FG800	512							
EP20K400E							212K	502	16640
EP20K600E							311K	624	24320
XCV1000E	HQ240	158	332K	330K-1.5M	26556	2/24	768K	660	27648
	BG560	404							
	BG680	512							
	FG860	660							
	FG900	660							
	FG1156	660							
BG560	404								
XCV1600E	BG680	512	420K	420K-2M	33276	2/24	1062K	724	34992
	FG860	660							
	FG900	700							
	FG1156	724							
EP20K1000E							327K	716	38400
XCV2000E	BG560	404	518K	520K-2.5M	40812	2/24	1240K	804	43200
	FG680	512							
	FG860	660							
	FG1156	804							
EP20K1500E							456K	858	54720
XCV2600E	BG560	404	685K	600K-3.2M	53196	2/24	1525K	804	57132
	FG680	512							
	FG860	660							
	FG1156	804							
	BG560	404							
XCV3200E	FG680	512	876K	800K-4M	67308	2/24	1846K	804	73008
	FG860	660							
	FG1156	804							

Virtex™ - 2.5V Virtex Series Key Features: Density/Performance, SelectRAM+™, SelectI/O™, DLLs

Devices	Package	Package I/O	Logic Gates	Typical Gate Range	Flip-Flops*	Output Drive (mA)	Maximum RAM Bits	Maximum Device I/O	Logic Cells
XCV50	CS144	94	21K	34K-58K	1536	2/24	56K	180	1728
	PQ240	166							
	TQ144	98							
	BG256	180							
EPF10K30E							24K	220	1728
XCV100	CS144	94	32K	72K-109K	2400	2/24	78K	196	2700
	PQ240	166							
	TQ144	98							
	BG256	180							
EPF10K50E							40K	254	2880
XCV150	PQ240	166	47K	93K-165K	3456	2/24	102K	260	3888
	BG256	180							
	BG352	260							
	FG256	176							
EP20K100							52K	250	4160
EPF10K100B/E							25K	338	4992
XCV200	PQ240	166	64K	146K-237K	4704	2/24	130K	284	5292
	BG256	180							
	BG352	260							
	FG256	176							
EPF10K130E							65K	413	6656
XCV300	PQ240	166	83K	176K-323K	6144	2/24	160K	324	6912
	BG352	260							
	BG342	316							
	FG456	312							
EP20K200							104K	320	8320
EPF10K200E							98K	470	9984
XCV400	HQ240	166	130K	282K-468K	9600	2/24	230K	404	10800
	BG432	316							
	BG560	404							
XCV600	FG676	404	187K	365K-661K	13824	2/24	312K	512	15552
	HQ240	166							
	BG432	316							
	BG560	404							
	FG676	444							
	FG680	512							
EP20K400							208K	496	16640
XCV800	HQ240	166	254K	511K-888K	18816	2/24	406K	556	21168
	BG432	316							
	BG560	404							
	FG676	444							
	FG680	512							
	FG680	512							
XCV1000	BG560	404	332K	622K-1,124K	24576	2/24	512K	660	27648
	FG680	512							
	FG680	512							

* I/O Flip-Flops not counted.

High End FPGA Products & Benefits Snapshot	
<p>Virtex-E</p> <ul style="list-style-type: none"> System-level integrated FPGA up to 3.2 million gates and 311MHz Differential signaling: LVPECL, LVDS, Bus LVDS 36 I/O pairs at 622 MHz Up to 832K bits of True Dual-Port(™) Block RAM Up to 1014K bits of Distributed RAM Delivers Terabit memory bandwidth 8 DLLs. Supports Double Data Rate Memory and backplane applications 1.8V operation 	<p>Virtex</p> <ul style="list-style-type: none"> System-level integrated FPGA up to 1M gates and 200MHz Up to 128K bits True Dual-Port RAM Up to 384K bits Distributed RAM 4 DLLs. Supports Double Data Rate Memory and backplane applications Optimized for synthesis and IP-based design methodology 2.5V operation
Total Solution	
<p>Software & Cores</p> <ul style="list-style-type: none"> 50% faster compile times, increased performance, Internet-based design features. Array of fully verified, predictable and parameterizable cores. 	

Competitive Overview

Virtex Series FPGA Competitive Cross Reference

Competitive Feature Comparison

Device	Timing Generation	5 Volt Tolerant I/O	I/O Standards Supported												Differential Signaling			
			LVTTTL	LVC MOS	PCI33	PCI66	GTL/GTL+	SSTL2	SSTL3	AGP	HSTL Class I	HSTL Class III	HSTL Class IV	CTT	LVDS	Bus LVCS	LVPECL	
Virtex-E	8 DLL	✓*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Virtex	4 DLL	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
APEX 20K	1 PLL		✓	✓	✓													
APEX 20KE	4 PLL		✓	✓	✓	✓	✓	✓	✓	✓	✓						✓	

* Requires 100 ohm external resistor

Competitive Feature Comparison

Device	Memory Access								
	Internal			External					
	Block	CAM	Distributed	SRAM	SSRAM	SGRAM	SDRAM	DDR	ZBT
Virtex-E	✓	**	✓	✓	✓	✓	✓	✓	✓
Virtex	✓	**	✓	✓	✓	✓	✓	✓	✓
APEX 20K	✓								
APEX 20KE	✓	✓		✓	✓	✓	✓		

** Supported with existing memory resources (see Application Notes on SPW)

Virtex-E is the Superior Programmable Solution

Superior Virtex-E LVDS Support

- Altera's APEX E LVDS only provides for 32 I/Os. Virtex-E supports LVDS, Bus LVDS, and LVPECL for up to 344 I/O pairs. Virtex-E Select I/O+ technology offers complete flexibility of choosing which standard is used on any given pin.
- Altera claims 622 MHz, but only for 16 inputs and 16 outputs, which is 10 Gbps. Virtex-E offers 36 pairs at 622 Mbps and delivers significantly higher LVDS Bandwidth by offering 344 I/O pairs at 311MHz per pair, which is a 107 Gbps (Gigabits per second) data rate.
- APEX E does not support backplane applications with Bus LVDS. Virtex-E offers Bus LVDS for all densities and speeds.
- APEX E does not support LVPECL. Virtex-E offers LVDS and LVPECL up to 622MHz for all densities. LVPECL is the industry standard for transmission of on-board clocks at greater than 100MHz.

Superior Virtex Clock Management

- Altera's analog PLLs do not support precise clock management. Designers can achieve an exact 50/50 duty cycle using Virtex DLLs, which is crucial for Double Data Rate (DDR) applications. APEX PLLs can not offer this precision.
- Superior Virtex-E logic and RAM offering**
 - Virtex-E offers 3.2 million gate densities in Q2/00 and up to 832K bits of Block RAM, plus distributed RAM. Compare that to Altera's 2.5 million gates in the middle of Y2000 with only 456K Block RAM bits.
 - APEX provides only block RAM and an interface to external RAM. Virtex offers more RAM and more types of RAM.
 - Virtex interfaces to the industry's highest performance memories, including:
 - 200 MHz ZBT SRAM
 - 266 MHz Double Data Rate (DDR) memory
 - Altera claims the dedicated CAM in APEX E, but the Virtex and Virtex-E offers CAM built from either distributed RAM or Block RAM at equivalent densities to those offered in APEX E. Most designs will require higher CAM densities than those offered with on-board dedicated CAM from Altera. In those cases, Virtex-E offers a faster external memory interface than APEX's.