How To *Create* an MP3 Player
Using Spartan-II FPGAs.

Spartan-II FPGAs are used to implement complex MP3 system-level glue logic.

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MP3 is rapidly becoming the defacto standard for the delivery of high quality music on the Internet. This technology has been well received as evidenced by the over five million MP3 software plug ins that have been downloaded to date. This is a testament to the future potential of the MP3 technology considering the relatively limited marketing it has received to date.

MP3 is an abbreviation for MPEG 1 layer 3, which is a compressed digital audio format that keeps the file size small without losing the quality of the original audio. MP3 allows audio files to be compressed to approximately $1/11^{th}$ of the original size. For example, a typical music CD consumes 650MB; using MP3 the same audio only takes 55MB! This has allowed music to be stored on the PCs hard drive, allowing users to effortlessly create and customize music play lists.

The compression achieved by MP3 makes it practical to construct a solid state portable audio player based upon FLASH memory as the storage medium. This article explores the development of a portable MP3 player using the Spartan-II FPGA family.

Design Overview

The MP3 player discussed in this application contains advanced user interface features, such as the ability to store contact information, record memos, and other functions typically found in Personal Digital Assistants (PDAs). The design uses an IDT RC32364 RISC processor to decode the MP3 data and implement the graphical user interface. The Xilinx Spartan-II FPGA is used to implement the complex MP3 system-level glue logic required to interface and manage the memory and I/O devices.

Figure 1 shows a block diagram of the design. The key features are:

• 128 x 128 pixel graphical touch screen.

• USB interface for music downloads and network connectivity.

• IRDA-compliant infrared interface for exchanging data with other units.
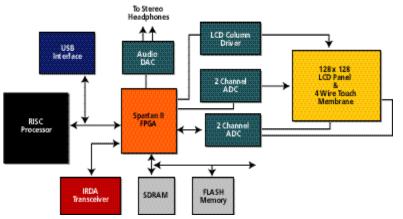
• 32 MB of on board FLASH storage.

Figure 1: MP3 system block diagram.

- CompactFlash interface for storage expansion using CompactFlash cards or MicroDrive hard drives.

Use of ASSPs

The design uses Application Specific Standard Products (ASSPs) to implement much of the complex logic. Typically, these ASSPs are not designed to communicate with each other. The Xilinx Spartan-II FPGA is used to provide the complex glue logic for the interface between the ASSPs and the RC32364 RISC processor from IDT.

The Digital-to-Analog converter is the Crystal CS4343 from Cirrus Logic. The CS4343 provides the analog stereo headphone interface; a serial port is used to transfer digital audio data streams, while an I^2C control port is used to configure the device features such as volume, muting, equalization, and power management.

The USB interface is the USBN9602 from National Semiconductor. This device supports full speed USB and includes an integrated USB transceiver. The system interface for the USBN9602 is an 8-bit microprocessor bus that can be configured to operate in a multiplexed or non-multiplexed mode. To reduce the number of pins, the multiplexed mode was used.

The FLASH memory is the Samsung KM29U64000T 8M x 8 device based on NAND FLASH technology. This memory is very popular in MP3 players due to its high density and low cost per bit. However, this FLASH memory contains two characteristics that present significant design challenges:

- The KM29U64000T uses a highly multiplexed 8-bit-wide port for both address and data access.

- Error detection and correction is needed to ensure system integrity.

The second and most challenging issue, data integrity, is common with NAND-based FLASH technology. The FLASH memory contains a range of valid memory blocks (N_{VB}). For the KM29U64000T the typical N_{VB} is 1020, the minimum is 1014, and the maximum is 1024. While the first block is guaranteed to be good, bad blocks can occur at any other location within the memory array. Invalid blocks are marked at the factory by storing a "0" value at location "0" in either the first or second block of the page. The design must keep a record of good blocks resulting in a non-contiguous memory map. A further issue is that the FLASH memory may experience additional block failures during the memories operational life.

Glue Logic Architecture

Figure 2 shows an overview of the architecture implemented in the Spartan-II FPGA.

The architecture consists of the following functional blocks:

- IP Bus Controller.
- CPU interface.
- LCD controller.
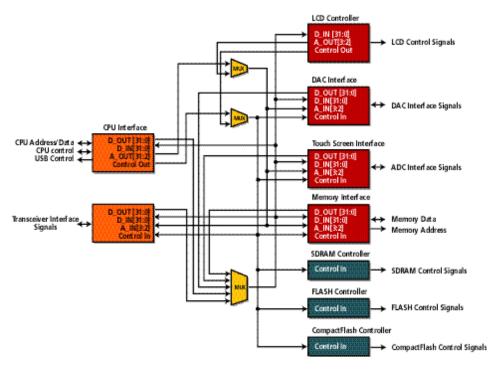- Memory Interface.
- SDRAM controller.

Figure 2: Spartan-II block diagram.

- FLASH Controller.
- CompactFlash Controller.
- IRDA Controller.
- Audio DAC Interface.
- Touch Screen Interface.

A simple non-multiplexed, multi-master address data bus called the IP bus, interconnects the blocks. Having the FLASH, SDRAM, and the CompactFlash RAM share a common address and data bus allows a reduction in pin count.

The IP Bus has two masters, the CPU interface and the LCD controller. Multiplexers are used for gating data into the internal datapaths, eliminating the need for 3-state drivers.

The CPU Interface performs the CPU initialization, the protocol conversion (to and from the CPU bus, USB interface, and the IP bus), and the address de-multiplexing.

The LCD Controller is responsible for refreshing the screen with the image stored in the SDRAM. The LCD controller can obtain the data for screen refresh independent of the CPU activities.

The Memory Interface block implements the data path required to map the 8- and 16-bit memory devices to the 32-bit IP bus. Although the RC32364 is capable of obtaining instructions and data from devices with varying bus widths, using the Spartan-II to implement this function reduces the CPU bus cycles and hence, increases performance and reduces power consumption.

The SDRAM controller is based on the design developed by Xilinx in application note XAPP134: Virtex Synthesizable High Performance SDRAM Controller There are two changes made to this design:

- The host interface is adapted from a multiplexed address data bus to a non-multiplexed data bus.
- A 16-bit wide SDRAM memory configuration is needed in place of the 32-bit wide memory datapath.

The FLASH Controller copies the executable image from the FLASH memory to the SDRAM at boot time, to overcome the FLASH random access latency and maximize system performance. This method also allows the NAND FLASH error code correction to be implemented in software, resulting in an efficient use of the FLASH memory.

The CompactFlash Controller provides the interface to allow the MP3 music files to be stored in to the CompactFlash memory via the USB serial link. The control signals required to retrieve the MP3 music file for playback are also contained in this block.

The IRDA Controller is essentially a specialized, fixed function UART. Separate, 2-word receive and transmit FIFOs are used to reduce the interrupt overhead associated with data transmission. The IR transceiver can support a data rate of 115 Kb/s resulting in a CPU interrupt every 557 ms.

The Audio DAC Interface provides the dedicated hardware needed to implement the transfer protocol for delivering an uninterrupted audio stream. This hardware consists of two, 4-word FIFOs, one for each audio channel and a state machine to manage the FIFOs and sequence the interface signals. The audio DAC interface also contains a 2-bit I/O port that uses software to implement the I^2C protocol used for accessing the control and status registers in the DAC.

The Touch Screen Interface is an I/O port that allows the processor to read the data returned by the two-channel analog-to-digital converter. This allows the system software to determine the X and Y touch screen coordinates.

Spartan Device Selection

Spartan-II devices are available in a wide range of densities and packages. The following criteria were used to select the device:

- I/O Pins. The design requires a total of 137 I/O pins.
- Voltage. The design operates at 3.3V.
- Density. The estimated size of the design is 83,000 gates.
- Performance. The highest clock speed used in this application is 64 MHz; this is used to clock the SDRAM controller. The remaining logic operates at sub multiples of this clock.
- Packaging. The size constraints imposed on most modern designs dictates a high-density surface mount package.

Based on these criteria the device selected for this design is the XC2S100. This device offers 100K gate density, 3.3V operation, 176 user I/Os, and is packaged in a FG256 BGA package. The cost of this device, in 100K quantities, is $12.95.

Conclusion

This design illustrates how Spartan-II FPGAs can be used to provide time-to-market advantages in high volume consumer applications. In this application, the Spartan-II FPGA is used as a cost-effective device to maximize the CPU performance and reduce system power consumption by providing some dedicated functions as well as the glue logic required to interface to the ASSPs. Using a Spartan-II FPGA also allows field upgrade flexibility, in a market where standards and protocols are still evolving. ∑