Xilinx Development Systems

Where Productivity & Creativity Meet

Xilinx Software R&D delivers new version 3.1i software tools that empower you to maximize your productivity, while leveraging your creativity.

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Programmable logic design has entered an era where device densities are measured in the millions of gates, and system performance is measured in hundreds of MegaHertz. Given these new system complexities, the critical success factor in the creation of a design is your productivity. Version 3.1i of the Xilinx development systems were created with your goals in mind-harnessing your creative engineering talent to the greatest extent possible.

Maximizing Productivity - Keeping Your Weekends Free

Creating your programmable logic design is probably only part of your job. You may also have to complete the board design, verify the design in the lab, or help create your product demonstration. We understand that Xilinx can contribute to your success by ensuring that the Xilinx design flow is as productive as possible. The 3.1i tools include the following improvements, making it easier than ever to finish your programmable logic design on time:

- Faster runtimes (2x).
- Faster clock Speeds (2x).
- Advanced HDL synthesis and optimization.
- Improved timing analysis and error navigation.
- Integrated logic analysis.

Runtimes

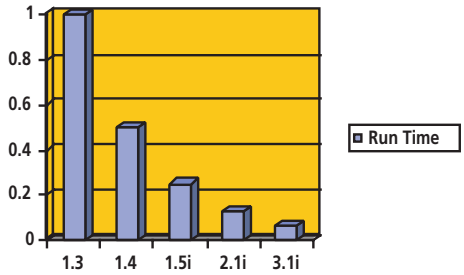
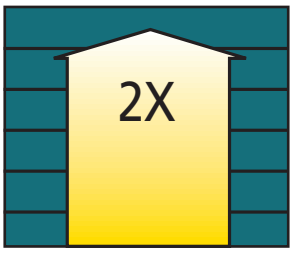


Figure 1 - Runtime improvements over consecutive releases.

The 3.1i release of Xilinx development systems deliver run time improvements that once again cut place and route runtimes in half. This is the fourth consecutive software release with 50% runtimes reductions, which means that the Xilinx solution is completing designs 16X faster than 4 years ago, as shown in Figure 1. It is important to note that these runtime improvements are independent of computing platform, and achieved even when placing and routing today's more complex devices. Improvements like these are why Xilinx is able to help keep you productive even when you are designing with a multi-million gate Virtex device.

Quality of results



To be most productive, you also need place and route tools that reliably converge on your design's timing requirements. Xilinx invented Timing Driven Place and Route for programmable logic

in 1992, and through our continued algorithmic innovations, we remain the leader in delivering superior quality results. In the 3.1i release, you can achieve 2x performance improvements when compared with designs created using the fastest speed grades that were available at the time of the previous 2.1i release. The industry's most advanced timing driven place and route tools, coupled with fastest devices, allow you to meet even the most challenging timing requirements using Xilinx programmable logic.

Advanced HDL Synthesis and Optimization

Xilinx 3.1i Foundation Series products include a new Block Level Incremental Synthesis (BLIS) capability that enables you to rapidly converge on your design's timing requirements. Synopsys has built this capability exclusively for Xilinx. BLIS is based on the concept of focussing the optimization of HDL on a module by module basis, localizing the changes within a module, and therefore improving the efficiency of guided design. BLIS is yet another design methodology that Xilinx is delivering to help you complete your design more efficiently.

Error Navigation and Timing Analysis

Having thorough and informative reports on the processing of your design also increases your efficiency. Furthermore, presenting this information in an intuitive and efficient format is also important; reviewing the reports is now easier than ever:

- **Error Navigation** - For warnings and errors that may arise during design compilation, Xilinx provides a direct link to a wealth of Solution Records that exist on our website (www.support.xilinx.com). These Solution Records provide answers to problems as simple as "incorrect pin connections" as well as more complicated problems like "how to obtain better clock rates using digital Delay Lock Loops".
- **Timing Reports** - For information on your designs timing, the Xilinx Interactive Timing Analyzer includes a new and improved hierarchical browsing capability. The new Timing Analyzer also includes a powerful "what if" analysis feature that allows for immediate analysis of your design when targeting different device speed grades, or using different timing constraints. Furthermore, Xilinx has rewritten its timing analysis algorithms so it requires substantially less memory and processes designs far faster. The combination of these improvements means it is easier to quickly analyze the performance of your design.

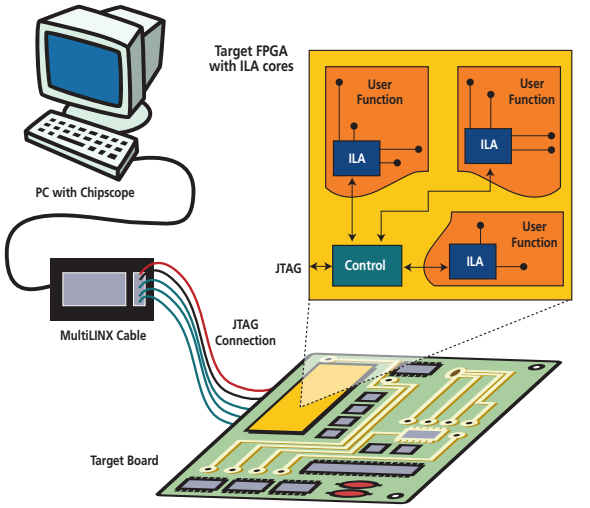


Figure 2 - Integrated logic analysis.

Integrated Logic Analysis

Your job isn't done until after your design has been incorporated into the production system as illustrated in Figure 2. To assist you in verifying your programmable logic device's behavior within the system, Xilinx now provides ChipScopeTM ILA, the Integrated Logic Analyzer. With ChipScope ILA you can perform complex system analysis on the behavior of your design as it works in real-time, within the system. The Integrated Logic Analyzer allows you to capture the waveforms of control signals, data buses, or any general logic within your Xilinx FPGA, and easily analyze their timing and functionality using ChipScope's easy-to-use graphical user interface. Helping you detect problems in the functionality or timing of your design within your system is another example of how Xilinx helps support you in becoming successful. (See the companion article on page 19.)

Emphasizing Creativity - How Good Designs Become Great

Mainstream design flows enable you to enter your design's functional and timing requirements and then "hand them off" to the layout tools to complete the job. Xilinx development systems are engineered to simplify the process of communicating your expert knowledge to our advanced design algorithms.

The 3.1i release includes new and improved versions of the following implementation tools:

- Xilinx Core Generator.
- Xilinx Constraints Editor.
- Xilinx High Level Floorplanner.

This powerful collection of tools will help make the process of creating your next programmable logic design the most efficient and productive yet.

Core Generator

By allowing you to easily reuse Intellectual Property, built elsewhere within your organization or by a 3rd party provider, the Xilinx Core Generator allows you to focus your creative energies on creating the unique aspects of your design, ensuring your products' success in the marketplace. The 3.1i release of the Core Generator delivers improvements in the graphical user interface, design flows, plus there is a host of new cores. See the IP Center http://www.xilinx.com/ipcenter/index.htm to learn about the Intellectual Property that is available for your use.

High Level Floorplanner

In the 3.1i release, the Xilinx Floorplanner has been enhanced to deliver the benefits of true modular design. The 3.1i floorplanner may be used in conjunction with the Xilinx Modular Design tools to enable the independent Timing Driven layout of functional modules of a design. Another benefit of the new Floorplanner is the new pin layout capability, which makes it simple to assign your design's I/O signals to the desired device pins.

Xilinx Constraints Editor

The 3.1i Xilinx Constraints Editor is another huge step forward in timing driven place and route efficiency. It simplifies the art of defining your circuits timing specifications, taking advantage of the industry's most robust timing constraint language—TimeSpecs™. In 3.1i, the Constraints Editor also supports the definition of timing constraints on a hierarchical basis, thus supporting modular design.

Furthering the art of logic design

The Xilinx 3.1i release has already been heralded as the industry's best programmable logic design tool. In the future, you will enjoy even more productivity because the Xilinx Software R&D team is already hard at work inventing tomorrow's break-through design techniques. While many of these inventions won't be available for mainstream use until our next major software release, some of these advancements will be included within our regular quarterly software updates. Please stay tuned for further announcements about your state-of-the-art programmable logic design system.

Conclusion

By focussing our resources on the challenges of productivity, Xilinx enables you to spend more time on the creative aspects of your design. This helps you get to market faster, and deliver a more robust product to your customers. The Xilinx 3.1i development systems deliver superior push-button, interactive, and state-of-the-art design methods. The 3.1i release will begin shipping to all registered, in-maintenance customers this spring. To learn more, please visit the Xilinx web site www.xilinx.com.