Intel XScale Microarchitecture Reference Design Features a Spartan-II Companion Chip

Xilinx XPERT and Alliance Reference Design partner, ADI Engineering Inc., has developed a high-performance reference design and evaluation platform for the Intel 80200.

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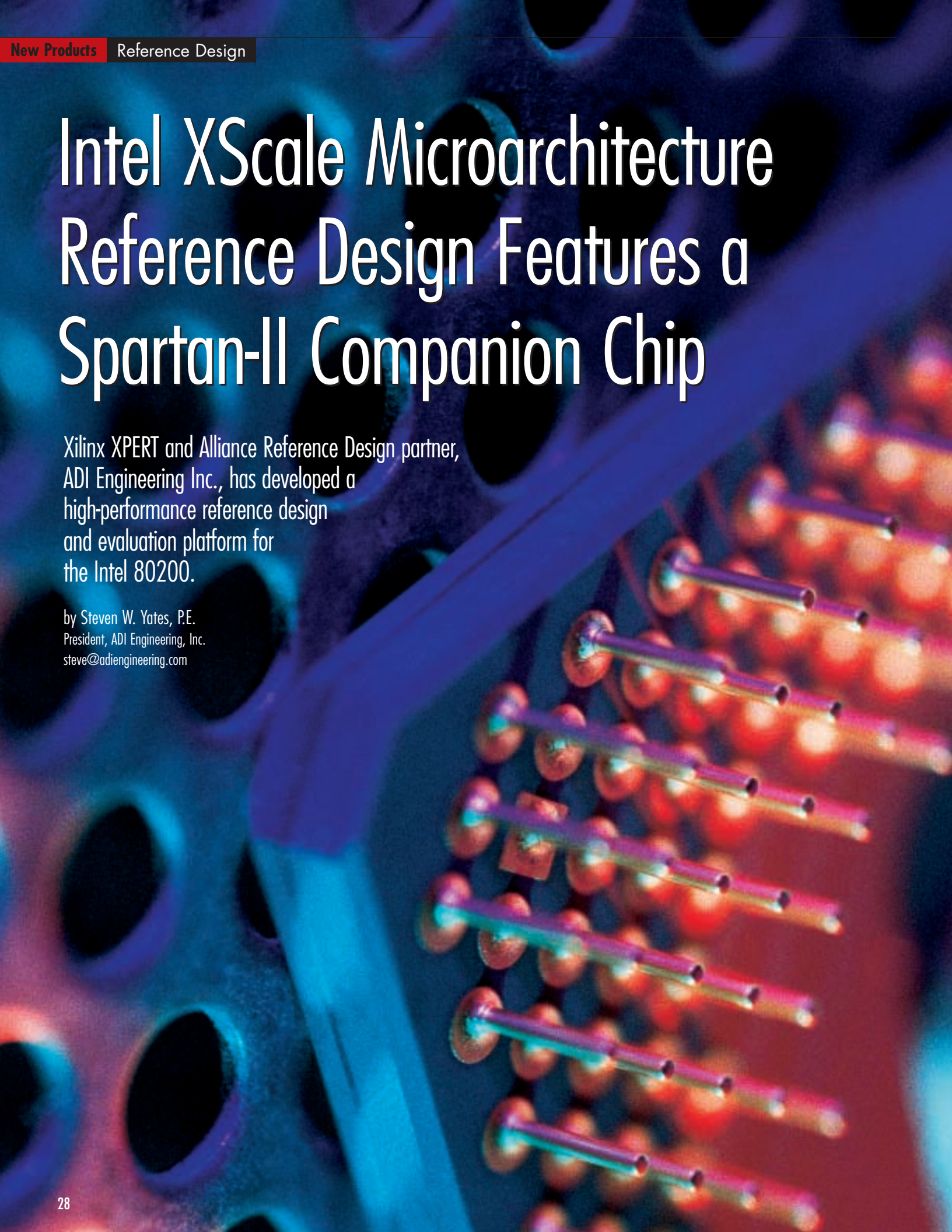

The Intel 80200 is the first processor based on the Intel® XScale™ microarchitecture: It integrates an external bus controller and an interrupt controller around the ARM™-compliant processor core. The 80200EVB reference design features a Xilinx XC2S150 Spartan-II™-based 80200 FPGA Companion Chip (80200FCC), providing 80200-optimized SDRAM control, a peripheral bus interface, and a 64-bit, 33 MHz PCI 2.2 interface.

The Intel XScale Microarchitecture

The Intel XScale microarchitecture represents a major advancement in high-performance, ultra-low power, embedded computing for applications including Internet appliances, handheld devices, networking and wireless equipment, and remote access servers. With its unique power-optimized, performance-oriented design, this microarchitecture offers highly scalable power and performance – from 125 MIPS at 10mW to 1,000 MIPS at less than 1W – to fit a wide range of applications.

As the successor to the popular StrongARM™ architecture, the Intel XScale microarchitecture features an ARM v.5TE instruction-set-compliant execution core with a wide array of performance enhancing and power saving technologies. Performance and power are scalable not only to suit the requirements of specific end applications, they can be adapted on the fly to match specific content as well.

The 80200EVB Reference Design

ADI Engineering's 80200EVB enables you to evaluate the Intel XScale microarchitecture, and to leverage the proven 80200FCC and board-level designs to accelerate your time to market.

Design Overview

The 80200EVB is a complete reference design for the Intel 80200 processor. Major features of the 80200EVB are:

- Intel 80200 processor running at up to 733 MHz
- Spartan-II 80200FCC companion chip implementing a high-performance SDRAM controller, 8-bit peripheral bus interface, and future 64-bit, 33 MHz PCI 2.2 interface
- 32 MB PC100 SDRAM, expandable to 128 MB
- 1 MB flash memory, expandable to 4 MB
- JTAG debugger interface
- RS-232 port
- Seven-segment LED display
- On-board power supply, operates from a single 9 - 15 VDC input.

A block diagram of the 80200EVB is shown in Figure 1.

80200 Bus Interface

The 80200 processor's external bus interface is deeply pipelined to hide external memory latency. This works well with pipelined memory technologies such as SDRAM.

The 80200 external bus interface is split into separate request and data buses, both of which are synchronous with respect to the 100 MHz memory clock. Requests for data read and write cycles are issued to the 80200FCC memory controller by the 80200 (or other bus masters) on the request bus. Up to four requests can be pending at a time.

Some time after a request is made on the request bus, data must be transferred for that request on the data bus. Each request has a corresponding transaction of one or more data cycles. Data bus transactions must occur in the same order as the requests were made but the request and data buses are otherwise independent. The data bus consists of a 32-bit or 64-bit wide data path and associated data check bits for use with ECC memory.

For burst read accesses, the 80200 supports a Critical Word First (CWF) protocol, which allows the data to be returned starting with the requested DWORD instead of starting at the beginning of the block of data. The 80200FCC supports the CWF protocol for SDRAM and peripherals on the peripheral bus.

80200FCC Memory Controller

The 80200FCC memory controller is a full-featured, high-performance SDRAM controller designed from the ground up to take advantage of the 80200's pipelined

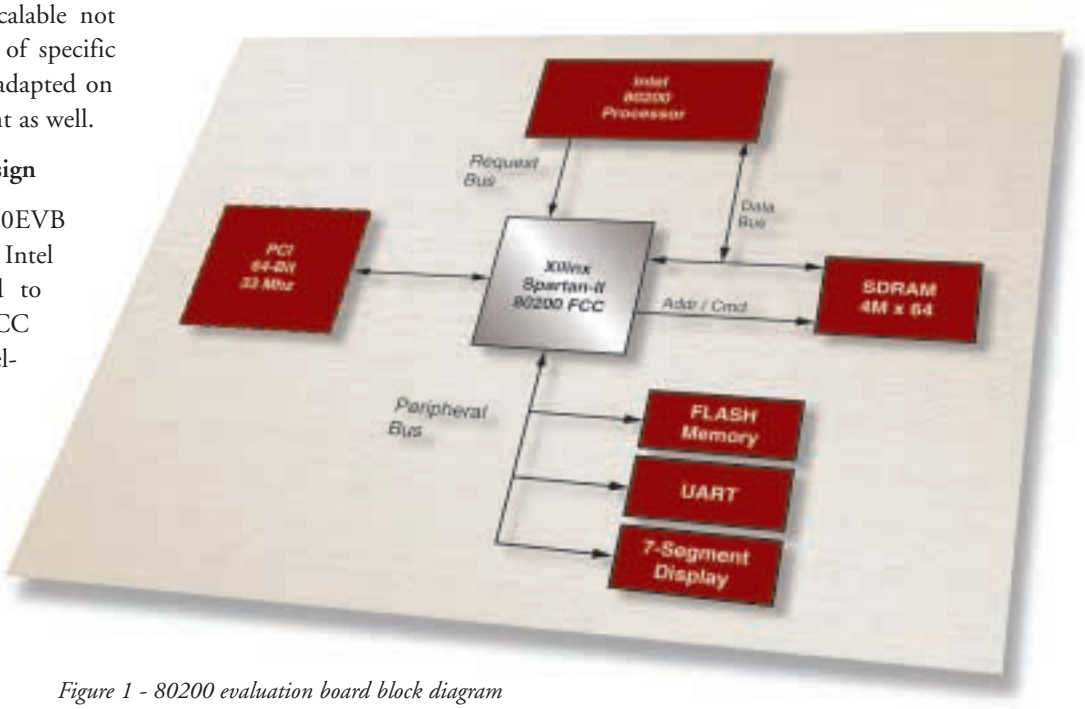

Figure 1 - 80200 evaluation board block diagram

external bus. Sequences of 80200 requests are examined and tracked by the 80200FCC memory controller as they enter into and propagate through its internal request queue. This enables the 80200FCC memory controller to look ahead at requested SDRAM transactions to determine how best to fulfill the requests while keeping the 80200 external bus operating at peak efficiency.

Major features of the 80200FCC memory controller include:

- Automatic SDRAM initialization
- Maintains row state for each SDRAM bank, closing rows only when necessary
- Automatically guarantees SDRAM command sequence timing
- Manages 80200 data bus by automatically inserting bus turnaround cycles when required
- Queues up to four pending 80200 requests
- Implements a two-level SDRAM refresh request priority scheme to minimize refresh overhead, queuing up to eight refresh cycles for burst execution
- Pipelines SDRAM commands to keep data bus fully utilized
- Supports Critical Word First protocol for SDRAM and peripherals
- Aborts illegal bus requests
- Provides a separate 8-bit peripheral bus, minimizing SDRAM performance impact
- Provides single stage write posting to the peripheral bus
- Achieves a sustained SDRAM bandwidth of 800 MB/s at 100 MHz.

The 100 MHz operation of the 80200FCC is made possible by the many performance-enhancing architectural features of the Xilinx Spartan-II family, including on-chip DLLs, I/O cell flip-flops, configurable I/O drivers, internal three-state buffers, and low-skew global routing resources. The Spartan-II family is able to provide these critical performance-enhancing features yet still maintain a low cost point.

To match the performance of the memory controller to a variety of SDRAM devices, many SDRAM timing parameters such as CAS latency, RAS precharge, RAS to CAS delay, and others are configurable. Configurable timing parameters may be

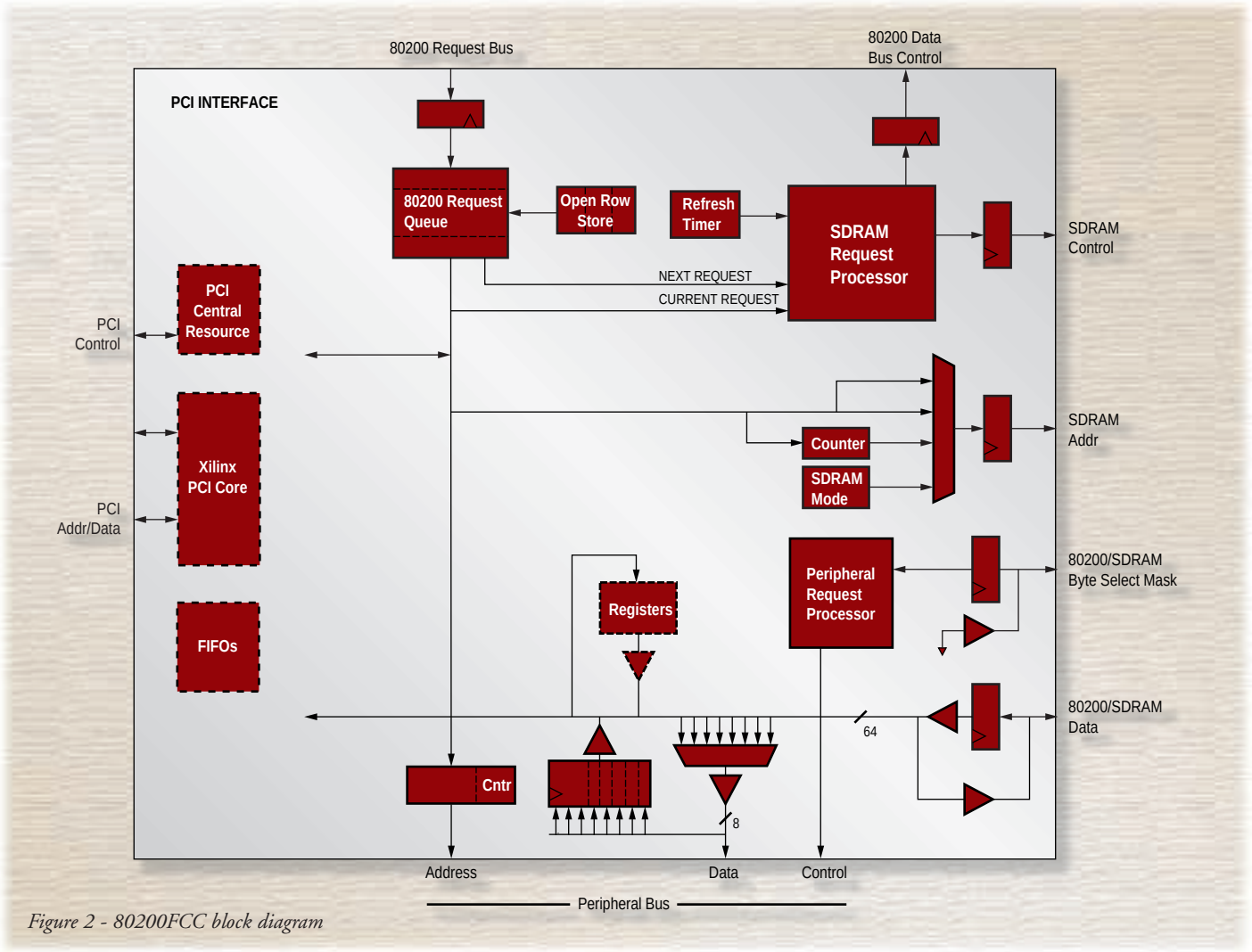

Figure 2 - 80200FCC block diagram

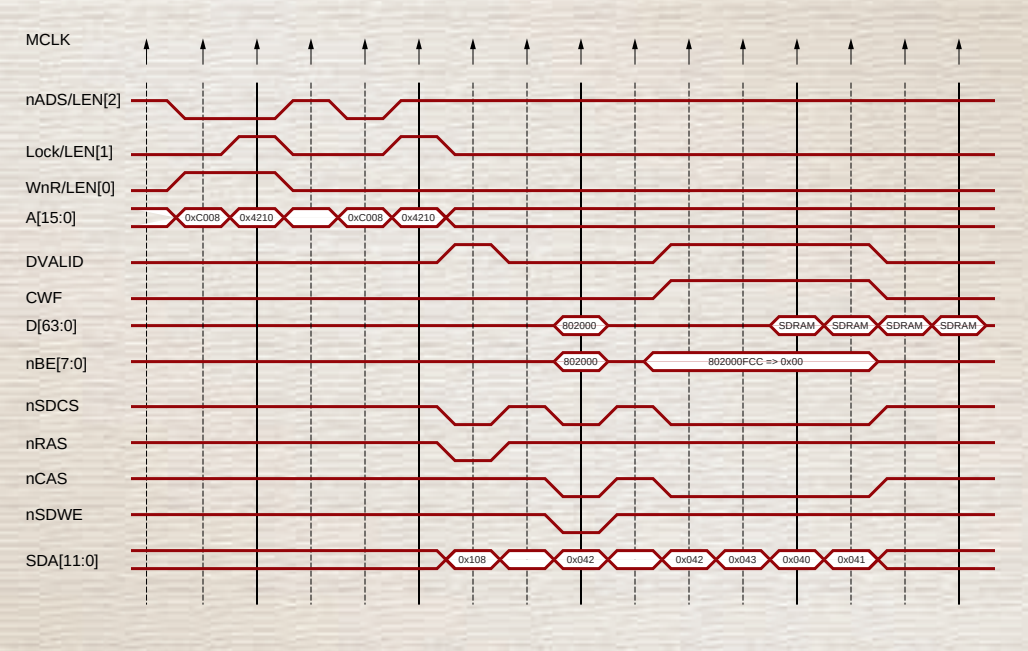

Figure 3 - Typical 80200 SDRAM access (write to idle SDRAM bank followed by a 32-byte read)

modified by changing VHDL constants and re-synthesizing the design.

A block diagram of the 80200FCC is shown in Figure 2.

A typical sequence of 80200 requests and corresponding SDRAM cycles is illustrated in Figure 3, which shows a write to an idle SDRAM bank followed by a 32-byte read.

PCI Interface

The 80200EVB board design supports one 64-bit, 33 MHz PCI 2.2 slot, although the initial 80200FCC release does not support PCI. ADI Engineering is currently adding PCI functionality to the 80200FCC.

The Xilinx LogiCORE™ PCI64 interface for Spartan-II devices will provide the basis for the 80200FCC PCI interface. This Xilinx IP enables the 80200EVB to leverage the Spartan-II XC2S150 to provide a low-cost integrated PCI interface while still providing ample spare CLBs for future enhancements and customization.

Peripheral Bus

A lower speed peripheral bus, separate from the 80200 100 MHz data bus, is provided by the 80200FCC for connection of flash memory and other peripherals. Because of the many different peripherals that could be connected to this bus, it is highly configurable. On the 80200EVB, the peripheral bus consists of an 8-bit data bus, four chip selects, read and write strobes, and 22 bits of address for 4 MB of address space per chip select. Peripheral bus data width, number of chip selects, wait state delays, and address space size are all configurable by modifying VHDL constants and re-synthesizing the design.

The 80200FCC performs data conversion between the 80200 processor and peripheral devices by steering data between the 8-bit peripheral bus and one of the eight byte lanes of the 80200 data bus, as shown in Figure 2. Byte lane selection is determined by the length and address of the peripheral bus request.

The 80200FCC peripheral bus interface handles any length 80200 read request (including 32-byte burst reads) by executing multiple peripheral accesses. Data are assembled in up to eight byte lane latches and returned in a single 80200 data cycle. For multi-byte reads, the peripheral bus address is incremented by a counter inside the 80200FCC. This counter supports the 80200 CWF protocol.

Conclusion

The ADI Engineering 80200EVB is a high-performance reference design and evaluation platform for the Intel 80200 processor. The Xilinx Spartan-II family plays a key role by providing a high performance yet low cost solution for the 80200FCC companion chip, and the Xilinx LogiCORE PCI64 interface will further leverage the low cost 80200FCC to provide an integrated PCI interface.

Design collateral for the 80200EVB and the 80200FCC is available free of charge to accelerate the time to market of custom 80200-based designs. You may obtain 80200EVB board schematic diagrams, 80200FCC VHDL source code, parts lists, and user documentation free of charge from Intel and ADI Engineering. Also, 80200EVB evaluation boards and custom design services are available from ADI Engineering.

Ordering Information

80200EVB evaluation boards may be ordered directly from ADI Engineering at 804-978-2888, ext. 1, or sales@adiengineering.com. Design collateral for the 80200EVB and the 80200FCC are available online at www.adiengineering.com.

ADI Engineering also is available to provide support and design services to develop custom solutions based on the Intel XScale microarchitecture. Additional information on the Intel XScale microarchitecture is available online at http://developer.intel.com /design/intelxscale/.