Software Solutions Version 3 Development Systems Quick Reference Guide

Xilinx development systems give you the speed you need. With the initial release of our version 3 solutions, Xilinx place-and-route times are as fast as two minutes for our 200,000-gate XC2S200 Spartan™-II device, and 30 minutes for our one-million-gate, system-level XCV1000E Virtex™-E device. That makes Xilinx development systems the fastest in the industry for the design of programmable logic devices (PLDs).

And with the push of a button, our timing-driven tools are creating designs that support I/O speeds in excess of 800 Mbps and internal clock frequencies in excess of 300 MHz.

The newest devices in the Virtex series, the Virtex-II family, are fully supported by the Xilinx development systems. Advanced design flows, including modular and incremental design, are now available for use in the designing of Virtex-II FPGAs

Xilinx desktop design solutions combine powerful technology with an easy to use interface to help you achieve the best possible designs within your project schedule, regardless of your experience level. For more information on any Xilinx product, visit www.xilinx.com.

Alliance Series™ Solutions:
The Alliance Series solutions contain powerful open systems implementation tools that are engineered to plug and play within your existing design flow. This combination of advanced features delivers high performance results on the toughest designs.

Xilinx Foundation Series™ ISE Solutions:
The Xilinx Foundation Integrated Synthesis Environment (ISE) is our next-generation, complete, ready-to-use design environment, optimized to deliver the benefits of an HDL methodology. Foundation ISE is packed with advanced technologies, in addition to Xilinx Alliance design entry tools, helping you bring your product to market faster.

Xilinx Web-based design solutions give you the ability to engage in digital design activities online using Xilinx application servers, or download design and implementation software modules for use in your own design environment. These applications include:

WebFITTER™:
The WebFITTER is a free Web-based design tool that allows you to evaluate your designs using Xilinx XC9500™ series CPLDs and CoolRunner™ series CPLDs.

WebPACK™ ISE:
The WebPACK ISE is a collection of free downloadable software modules, including ABEL v7.3, VHDL, and Verilog synthesis, design implementation tools, and device programming software.

WebPACK ISE now includes support for all Xilinx CPLD families (XC9500 series and CoolRunner series) and the entire Spartan-II FPGA family, as well as the 300,000-system-gate Virtex XCV300E FPGA.

WebFITTER URL:
www.xilinx.com/sxpresso/webfitter.htm

WebPACK ISE URL:
www.xilinx.com/sxpresso/webpack.htm

Version 3 Development Systems

Feature Comparison Guide

Design Entry	Alliance	Foundation	Foundation ISE	WebPACK
Schematic		●	●	●
VHDL, Veriolog HDL, ABEL, HDL		●	●	●
State Diagram Editor		●	●(1)	●(1)
Floorplanner	●	●	●	●
CORE Generator	●	●	●	●
Timing Constraint	●	●	●	●
Modular Design	(Optional)		(Optional)	
Design Synthesis	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Xilinx Synthesis Technology (XST)			●	●
FPGA Express / Incremental Synthesis		●(5)	●	
Design Verification	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Timing Simulation	●	●	●	●
Gate Level Simulator		●	●(2)	●
HDL Simulator	●(1)	●(1)	●(1)	●(1)
HDL Testbench Generator			●(1)	●(1)
Integrated Logic Analysis (ChipScope ILA)	(Optional)	(Optional)	(Optional)	
Static Timing Analysis	●	●	●	●
Design Implementation	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Constraints Editor	●	●	●	●
CPLD ChipViewer	●	●	●	●
FPGA Editor	●	●	●	●
Error Navigation to Xilinx Web			●	●
Command Line Operation	●		●	●
HTML Timing Reports	●	●	●	●
Data Book I/O Timing	●	●	●	●
Timing-Driven Place-and-Route	●	●	●	●
Multipass Place-and-Route	●	●	●	
Project Archiving	●	●	●	●
System Interfaces	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
EDIF In	●	●		CPLD Only
PROM File Generator	●	●	●	●
JTAG Download Software	●	●	●	●
IBIS	●	●	●	●
STAMP	●	●	●	●
VHDL, Verilog Out	●	●	●	●
HDL Simulation Libraries	●	●	●	●
Environment	**Alliance**	**Foundation**	**Foundation ISE**	**WebPACK**
Operating System	PC / UNIX	PC	PC	PC

Device Comparison Guide

Elite	Standard/Express	Base/Base Express	WebPACK ISE
All Virtex-II Family	Virtex-II Family up to XC2V1000	Virtex-II Family up to XC2V80	Virtex XCV300E only
All Virtex-E Family	Virtex-E Family up to XCV1000E	Virtex-E XCV50E only	All Spartan-II Family
All Virtex Family	All Virtex Family	Virtex XCV50 only	All CoolRunner Series(4)
All Spartan Series	All Spartan Series	All Spartan Series	All XC9500 Series
All XC9500 Series	All XC9500 Series	All XC9500 Series	
All XC4000E/L/EX	All XC4000E/L	All XC4000E/L	
All XC4000XL/XLA	All XC4000XL/XLA/EX/XV(3)	XC4000XL/XLA up to XC4020	
All XC3000(3)	All XC3000(3)	All XC30003	
All XC5200(3)	All XC5200(3)	All XC52003	

1. Evaluation functionality available through the Xilinx ALLSTAR program. For more information on the ALLSTAR program, go to www.xilinx.com.
2. Functional and timing simulation is performed using a HDL simulator in the ISE product.
3. XC3000, XC5200, and XC4000XV devices are not supported in the Foundation Series ISE configurations.
4. CoolRunner series is only available in WebFITTER and WebPACK tools at this time.
5. Foundation Base does not include a license for FPGA Express.