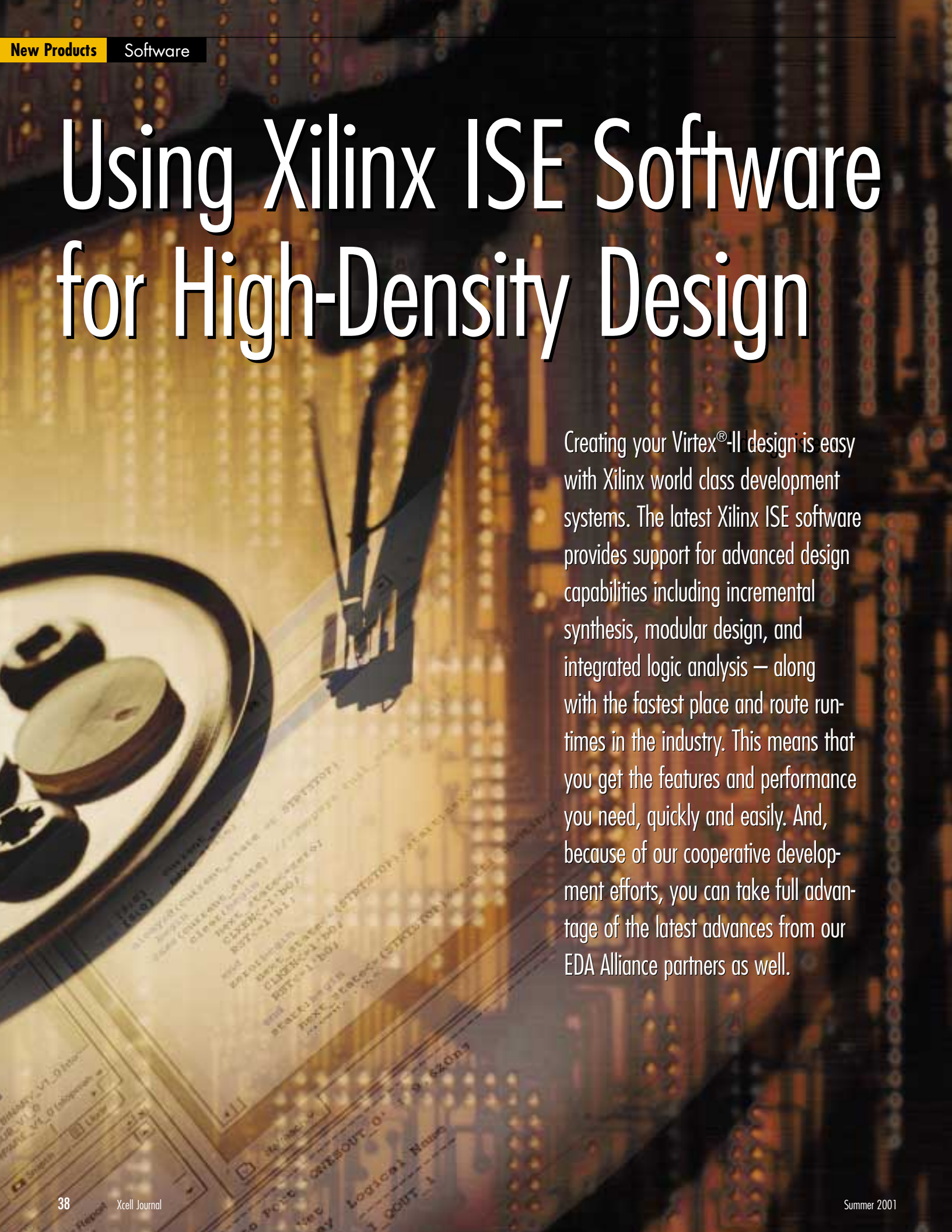
Using Xilinx ISE Software for High-Density Design



Creating your Virtex®-II design is easy with Xilinx world class development systems. The latest Xilinx ISE software provides support for advanced design capabilities including incremental synthesis, modular design, and integrated logic analysis – along with the fastest place and route run-times in the industry. This means that you get the features and performance you need, quickly and easily. And, because of our cooperative development efforts, you can take full advantage of the latest advances from our EDA Alliance partners as well.

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ISE Overview

With the Virtex®-II family and the Platform FPGA initiative, programmable logic has matured well beyond its original use as simple glue logic. Programmable devices are now the central components in many advanced system designs because of their high performance, extreme density, and advanced features. To take full advantage of these advanced devices, you need advanced, high performance development tools as well; and that's what you get with the Xilinx ISE software.

The Xilinx ISE (Integrated Synthesis Environment) provides everything you need in a single, tightly integrated package. The ISE software includes:

- A full design management and implementation environment
- Integration for the most widely used synthesis engines in programmable design including Synopsys, Synplicity, and Exemplar.
- Fast and easy design realization
- Simulation integration with ModelSim
- The fastest place and route technology available for logic implementation
- EDA partner integration for your existing design software flow.

Partitioning

To make your design process more manageable, first partition your design into hierarchical, functional modules. By partitioning your design correctly, you can accelerate timing closure by keeping critical gates and paths together, and you can simplify your design by reducing the number of interface ports between modules and minimizing intermodule delay paths.

Many factors will determine how these modules should be defined:

- What are the skills and strengths of the available designers?
- Where in the device can prior design work be utilized?
- How many functions can be implemented through cores or purchased IP blocks?
- Which areas of the design will require unique or intensive design work and re-work?

Use the Xilinx High-Level Floorplanner to partition your design, as shown in Figure 1. This will constrain the hierarchical modules to specific physical areas of the device. If I/O signals are known, the design manager can also map them, or reserve I/O blocks for future use.

Floorplanning at the beginning of the design process serves three main purposes:

- Floorplanning divides your design into manageable sub-modules. After floorplanning, the design manager can create black-box definitions to define the HDL modules. This allows each designer to receive the correct design definitions of their respective module – and the design manager can still perform analysis functions at any time from the top block of the device without requiring all the modules to be complete.
- During floorplanning, the engineering manager can create module boundary definitions to initially describe the HDL module entities. This allows designers to receive the correct design definitions for their respective modules – and the engineering manager can later perform analysis functions without requiring all modules to be complete.
- Floorplanning helps to accelerate implementation times.

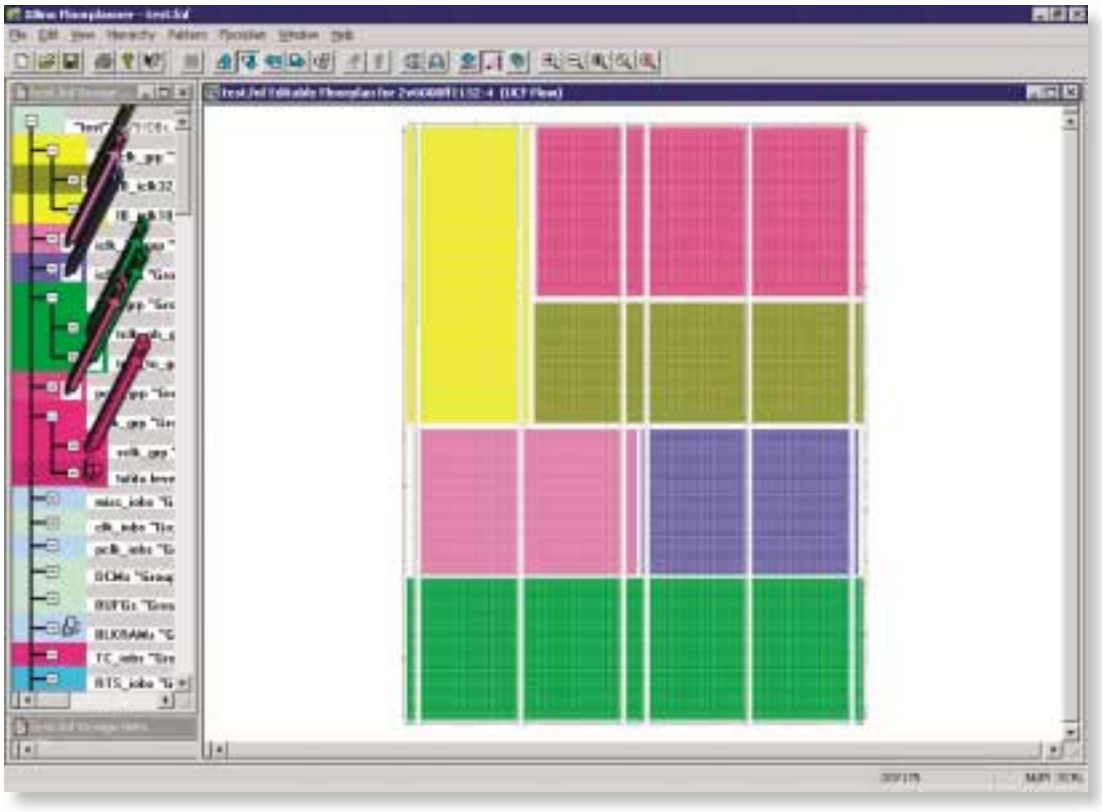

Figure 1 - Floorplanner

Design Creation

The ISE software offers a wide range of alternatives for creating your design.

VHDL and Verilog Design Entry

The most common method of design entry today is through either VHDL or Verilog language text entry, using a standard text editor, or context-sensitive language editors. These editors allow you to enter complete language statements through simple keystrokes and easily analyze syntax for missing language structures.

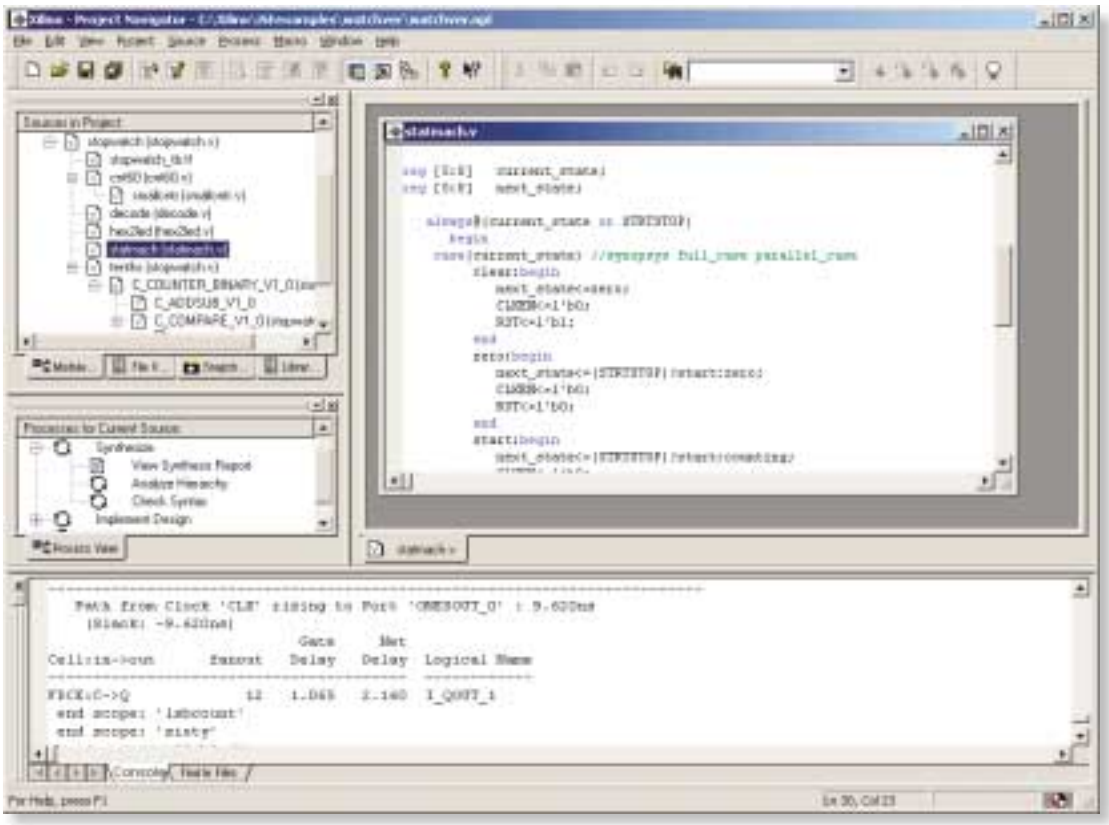

Figure 2 - Project Navigator

The ISE Project Navigator, shown in Figure 2, is where you drive design entry; it contains a complete VHDL/Verilog language editing environment, with context-sensitive help and language templates to help you quickly enter your code.

Graphic Design Entry

Graphic design entry is experiencing a resurgence in high-density design. In the late 1980s graphic entry became a popular design method, but as device density grew, it proved too cumbersome. Coupled with the use of Xilinx Modular Design, graphic entry is making a strong comeback as design work concentrates on implementation of smaller modules, not the overall device.

With our recent purchase of VSS (Visual Software Solutions), StateCAD is now tightly integrated into the Xilinx standard design tools. StateCAD offers state-diagram, finite state machine, truth table, and flowchart logic entry that can you can then output as VHDL or Verilog code.

These graphic entry methods also help you to document your design, in a very readable and easily understood format; they are the preferred method of entry for a growing number of design engineers, depending on the size of the target module.

Using Intellectual Property

To meet strict deadlines, you increasingly need reliable, affordable, pre-engineered designs that can be easily modified for your specific application. That's why the fastest growing design option for high-density design is IP, or Intellectual Property, which includes free and purchased cores, and the re-use of your own captured and verified code.

The very nature of the FPGA device fabric, allows IP to give you quick product turnaround in a reliable, repeatable format. The commercially available cores have already been verified for use in specific device families, eliminating the need for silicon verification, which thus reduces your overall design time. There are a wide range of fully verified, complex cores from which to choose, which frees you to concentrate on other critical design areas.

Through the Xilinx LogiCORE™ program, hundreds of standard IP functions are available. These include cores such as multipliers, filters, FIFOs, error correction, Ethernet MACs, ATM functions, HDLC controllers, and video blocks. The AllianceCORE™ program expands this offering to include some of the best third-party IP available. And the Reference Design program offers free advice and design applications from certified design centers throughout the world. Xilinx has bundled this information together, and makes it available through the Xilinx IP Center (www.xilinx.com/ipcenter). Here, you'll find everything you need to design with IP, including the recently announced MicroBlaze™ soft processor core.

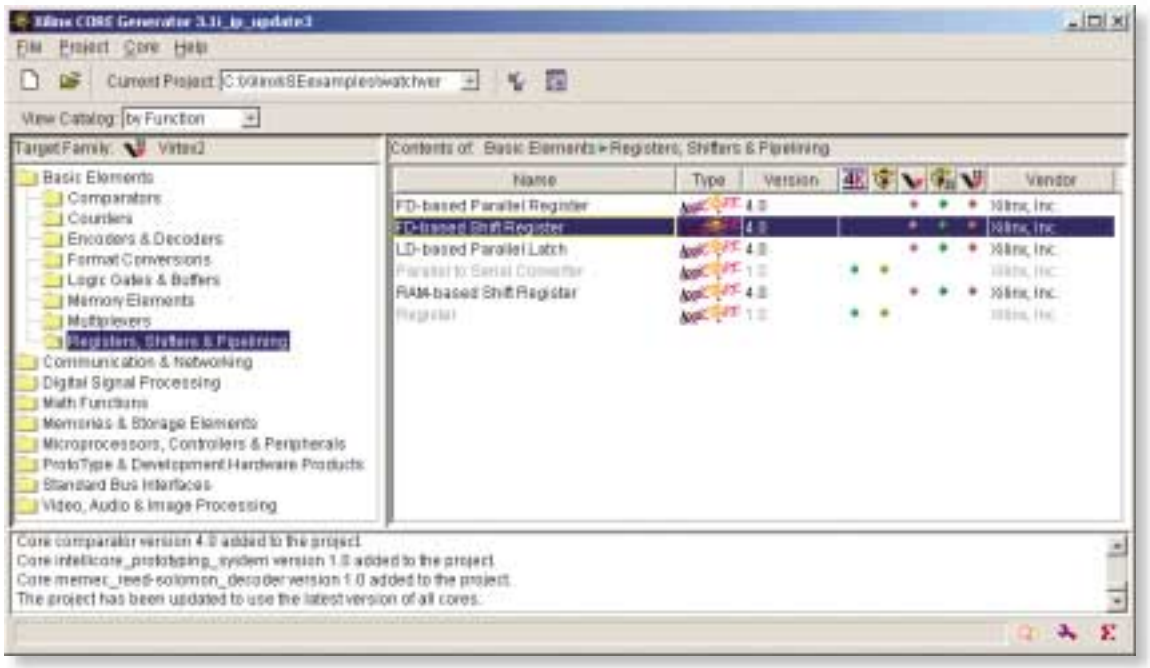

Figure 3 - CORE Generator

Using the CORE Generator

Most cores are customizable, allowing you to modify them for your specific needs. To manage this process, Xilinx provides the CORE Generator as shown in Figure 3. The available cores are displayed in a library interface, so you can easily choose the appropriate core for your needs. The cores are adjustable for the parameters you want to customize, and the area/speed trade-offs appropriate to your specific design. You can also link the CORE Generator to the Xilinx IP Center and receive regular core updates.

Internet Capture for IP is also integrated into the Core Generator to facilitate design reuse. You can capture your corporate-developed IP as standardized cores and use the CORE Generator as a cataloging and delivery vehicle. Your cores then appear in the library interface for later selection and use.

Using Standard I/O Functions

Using a core to solve a critical design challenge is only a part of the overall solution; you also have to interface that function to the outside world. A key feature of the Virtex-II family is high speed connectivity; interfacing the internal logic to external systems such as memories, network fabric, PC peripherals, and other ASSPs. To implement these I/O functions you can use standard cores such as PCI, PCI-X, RapidIO™, POS-PHY, Flexbus, SDRAM controllers, UTOPIA and so on. You don't need to spend time recreating common interface functions, or worry about spending time translating bus logic.

Using DSP Functions

Xilinx FPGAs offer the highest performance DSP processing power you can get anywhere, with speeds beyond 600 billion MACs; even mainstream, dedicated digital signal processors cannot match our performance.

To help you make full use of this power, Xilinx launched the XtremeDSP™ initiative, which provides all the cores, the development tools, and the support you need. Cores such as advanced DSP filters, Reed-Solomon filters, modulators, transforms, math building blocks, video and imaging algorithms, and wireless cores are all available today. And through our collaboration with The Mathworks, Xilinx provides seamlessly integrated MATLAB/Simulink and System Generator software, bridging the gap between the system design domain, and direct implementation in the FPGA.

Design Management

With the Xilinx ISE software you can utilize many different tools and design methods. To help you manage these options and drive your design to a smooth completion, we provide the Project Navigator, as shown in Figure 2.

For each module of your design, the Project Navigator launches the correct tool for a given process, and tracks the module from creation through final implementation. Context sensitive design flows provide pushbutton processes to correctly implement a module, and you can easily see the status of all processes. You can also take snapshots of the running processes to enable revision control; then you can easily restore your design at any point, allowing you to easily try different design ideas without losing any of your work.

The Project Navigator also provides a status window feedback that is Web-enabled so error messages can be passed to the Xilinx Solution Center where solutions are kept constantly up-to-date. This gives you the most direct and accurate answers, eliminating the time spent browsing help files and documentation to find the correct answer.

Modular Design

By starting with floorplaning, you can now leverage a new technology Xilinx has pioneered to make high-density design even faster – Modular Design.

Xilinx Modular Design is a productivity option that works in addition to the ISE

design software. With Modular Design, you can use all Xilinx implementation tools independently and completely on each module of your design; enabling design teams to work in parallel to complete their individual modules.

Modular Design delivers speed and productivity in high-density designs by offering a true team design environment that allows parallel implementation of the partitioned design modules. But more important, Modular Design treats each module as a separate design by completing and then locking down implementation results on a module-by-module basis. A change to one module does not affect the implementation or timing of completed modules. With Modular Design, high-density designs are finished much faster than in a traditional serial design flow.

Using Timing Constraints

With Modular Design, you can work on smaller design modules, and each of those modules can be implemented separately. Therefore, using timing constraints for synthesis is very similar to the general synthesis rules for small to moderate designs. However, there are a few key factors that will affect high-density implementation results.

Be careful not to over-constrain your design. Many designers operate under the mistaken belief that by over-constraining a module they will guarantee timing. However, over-constraining can force the synthesis tool to introduce extra gates into the finished module. One method to consider is to begin implementation by synthesizing without timing constraints. Let the synthesis tool work for the best design, and point out to you the areas that will cause problems; then you can go back and constrain only those portions of the module that need better timing.

Use Good Coding Practices

Timing can also be seriously affected by how well your design code can be synthesized. Xilinx recently announced the 1.0 coding style guide for the Synopsys LEDA (Library of Efficient Data Types and Algorithms) tool language checkers. The LEDA tools can verify your module against standard good coding practices. This reduces the chance of problems during implementation (due to bad coding styles, such as introducing unnecessary latches into the finished module, which may cause timing analysis mistakes). The LEDA tools are also flexible for use with customized coding styles, to assure that your design meets your own specific corporate coding standards.

Physical Synthesis

The two most time-intensive steps in implementation are place-and-route and synthesis. These two critical design phases are usually loops of multiple iterations where you spend most of your design effort modifying your design and re-running the software, attempting to meet the timing requirements for a module. Xilinx has pioneered a new technology, physical synthesis, to help shorten this design cycle and make the implementation loop much more intelligent.

With physical synthesis for FPGAs, the synthesis step can now make intelligent decisions to help speed the overall design results because it has some knowledge of your floorplan, the physical device configuration, and any early placement information. The place-and-route process can also pass timing information back to the synthesis tool once critical delays have been identified. Therefore, the number of iterations is reduced, and device performance is increased.

Physical synthesis works with our place-and-route tools, our partners' synthesis tools (Synplicity and Exemplar), and our own XST synthesis software.

Xilinx XST

Xilinx Synthesis Technology (XST) is included with the ISE software, and is focused on optimizing your designs for the specific Xilinx device technology you are using. XST was developed to help remove programmable device implementation barriers and then pass those technology solutions onto the synthesis engines provided by our partners, such as Synplicity, Synopsys, and Exemplar.

If your design is running below your performance requirements, try running an implementation pass through XST. You may get better speeds, and eliminate several design iterations.

Conclusion

The Virtex-II Platform FPGA family will continue to increase in density, performance, and features, and the Xilinx ISE software will continue to make your design flows productive. By combining the latest software technologies from Xilinx and our partners, you get the fastest and most productive development platform ever, and it just keeps getting better.

For more information on Xilinx ISE software go to: www.xilinx.com/xlnx/xil_prodcat_landingpage.jsp?title=Design+Tools.