Discontinuity at the Gate – A New Era in FPGA Design

The Xilinx vision in programmable logic will change how you do digital design. Mentor Graphics has recognized this and is committed to the FPGA market.

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What happens when you give the design community a field-programmable hardware platform that contains 10 million system gates, 300+ MHz internal clock speeds, gigabit serial I/O performance, and IP immersion technology? You create an opportunity for an entirely new complex design methodology. By providing such robust capabilities in a programmable format, you create a discontinuity in the industry that removes previous cost and technology barriers from the product development process. The Xilinx Virtex-II Platform FPGA family embodies this emerging technology, and has provided the catalyst to change our current design methodologies.

Today it is estimated that there are 20,000 custom or semi-custom chip designers, and this number is growing very slowly, as shown in Figure 1. Under the current structure, issues including design styles, verification methodologies, NRE charges, risk, and software development inhibit how many circuits can be attempted each year. Creating a standard platform for development removes these limitations, and allows the number of potential designers to grow by an order of magnitude, to 200,000. This massive influx of potential designers creates a new brain pool for innovation.

FPGAs Coming of Age

The path to harmony between design tools and actual silicon is extremely challenging. For example, as shown in Figure 2, in the ASIC world it took 15 years to merge the silicon process with a solid design methodology based on reliable and functional EDA software. ASIC technology became the driving force in the industry. The process that began surrounding this technology created an effective solution for the electronics industry, which led to growth and innovation. But the ASIC process has matured to the point where it is applicable more for extremely high-end design, and it is slowly moving out of reach for the mass market.

In contrast, FPGA technology has taken only five years to get to the same level of functionality as ASICs. FPGA technology has uniquely solved the same problems the ASIC methodology addressed, but along the way it also minimized the NRE, risk, and manufacturing issues involved as illustrated in Figure 3. Today, the Xilinx Virtex-II technology is a legitimate ASIC replacement. When combined with leading-edge EDA software, Virtex-II FPGAs provide the electronics industry with a new, exciting path for growth and innovation. FPGAs are now the key vehicle driving the state-of-the-art for new electronic systems.

The Xilinx platform-based FPGA technology brings programmability to the System-on-Chip (SoC) methodology. Using a 0.15µ, 8-layer metal process with 0.12µ high-speed transistors, Virtex-II FPGAs provide designers with the performance and density they need to create an SOC design. With features like digital clock management, select I/O ultra technology, and active interconnect, designers can spend more time on functional verification, knowing that the main silicon issues and problems have already been solved. In addition, with IP immersion technology, FPGA designers can now work at a much higher level of abstraction and move the "gates per day" metric to a level where silicon utilization is maximized.

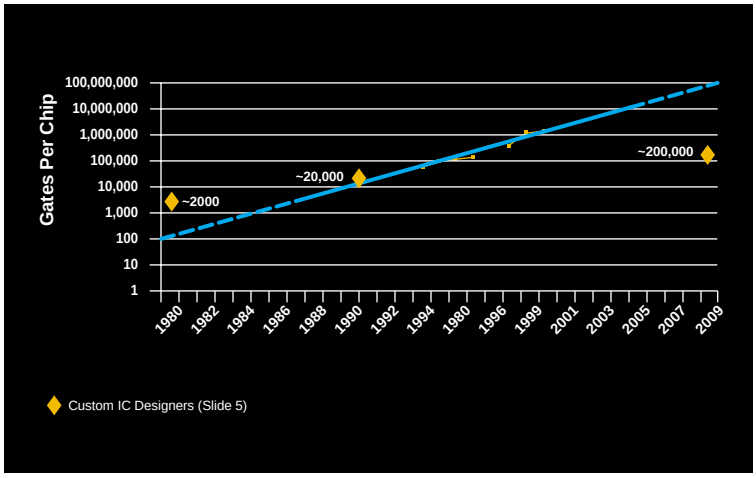

Figure 1 - Gate-to-designer ratio

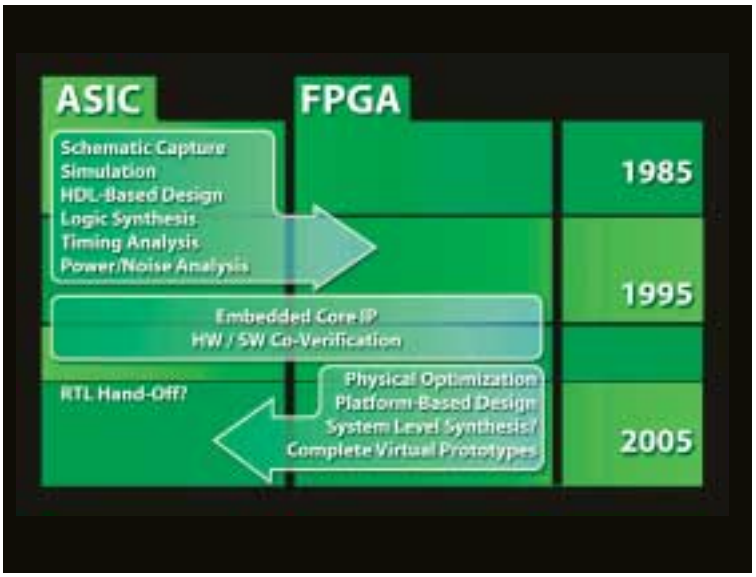

Figure 2. Evolution of ASIC and FPGA design methodologies

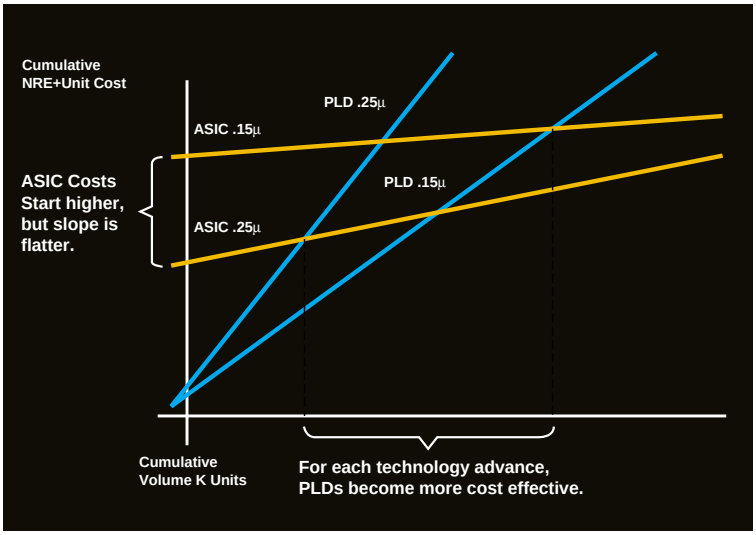

Figure 3. FPGA to ASIC crossover improves with process

Platform-Based FPGAs – The Value of History

Creating standards and putting boundary conditions on a design process can accelerate circuit development and shorten time to market. The ASIC SOC development process in place today is an open-ended approach to design with almost an infinite degree of freedom. This freedom provides flexibility and has enabled the creation of extremely complicated circuits, but it has also created a high risk methodology with a steep learning curve.

In contrast, platform-based FPGAs provide a structured approach to design. From the designer's point of view, the beauty of creating an FPGA is that the FPGA vendors worry about all the issues of the design process (silicon, methodology, and software).

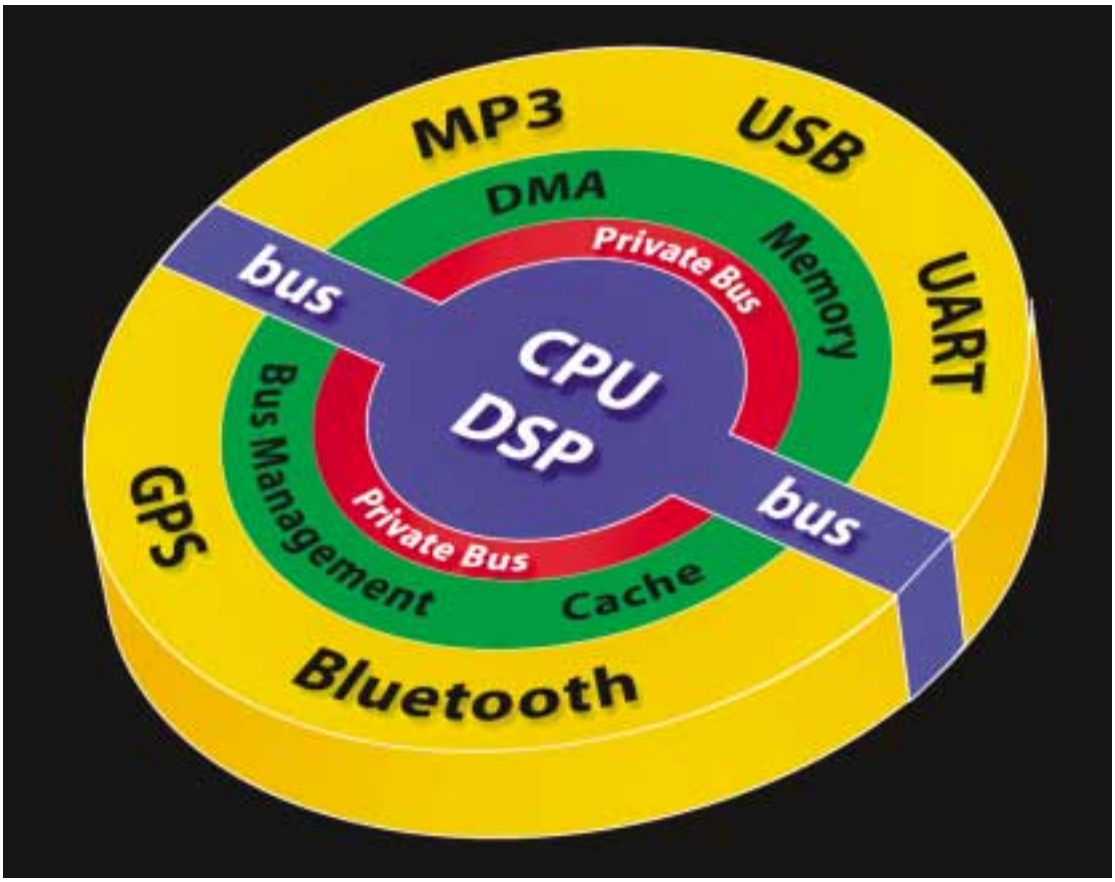

Figure 4 - Platform-based FPGAs integrate IP to user-defined logic

From the FPGA vendor's point of view, they need to provide their customers with a solution that enables high-quality, repeatable results.

Platform-based FPGAs have taken the problems found by previous ASIC SoC designers and minimized them by providing a proven, recommended path for success. In the history of electronic design, innovation and productivity are at their peak when proven methodologies permeate the industry.

IP Immersion

Designing an ASIC SoC requires a highly experienced team of engineers from multiple disciplines. This team must learn how to use a processor, develop software on it, and connect IP into the system. These learning curves are long and riddled with mistakes. And, because all design blocks come from different places, integration rarely works on the first try.

Platform-based FPGAs solve some of the big issues that limit the development of ASIC SoCs by addressing IP integration issues, as shown in Figure 4. The Xilinx IP immersion technology maximizes performance and density by providing a fixed and proven structure to integrate hard and soft IP into the silicon architecture.

Platform-based FPGAs using embedded processors will be the next key technology that will push FPGA design forward. By limiting support to only certain CPU architectures, all integration information is predefined for functions such as control signals, clocks, and data buses. Soft IP is pre-engineered to work with these predefined buses, so the designer just needs to connect these fixed IP objects to the buses. For the user-defined section of the chip, the design has been made easier because its boundary conditions are known.

To take advantage of these fixed-CPU platform-based FPGAs, designers will look for new applications and uses. Since the cost of implementation will be in everyone's reach, we should see a resurgence of the garage-shop mentality and new out-of-the-box thinking.

Enabling Innovation Together

At Mentor Graphics, we enjoy collaborating with a partner that looks at the big picture and asks, "How do I change the future?" The Xilinx vision in programmable logic will change how we do digital design. Mentor has recognized this and is committed to the FPGA market. We continue to develop point tools and solutions to solve the tough design problems. Mentor realizes that dedicated FPGA flows, tested and integrated tightly with the vendor software, will provide the technology that will "Enable Innovation" for the future of the electronic industry.

> TODAY, THE XILINX VIRTEX-II TECHNOLOGY IS A LEGITIMATE ASIC REPLACEMENT. WHEN COMBINED WITH LEADING-EDGE EDA SOFTWARE, VIRTEX-II FPGAS PROVIDE THE ELECTRONICS INDUSTRY WITH A NEW, EXCITING PATH FOR GROWTH AND INNOVATION.
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> — WALDEN C. RHINES, CHAIRMAN AND CEO, MENTOR GRAPHICS