The Virtex-II DCM – Digital Clock Manager

Higher system bandwidth requires higher data rates between devices, and advanced clock management.

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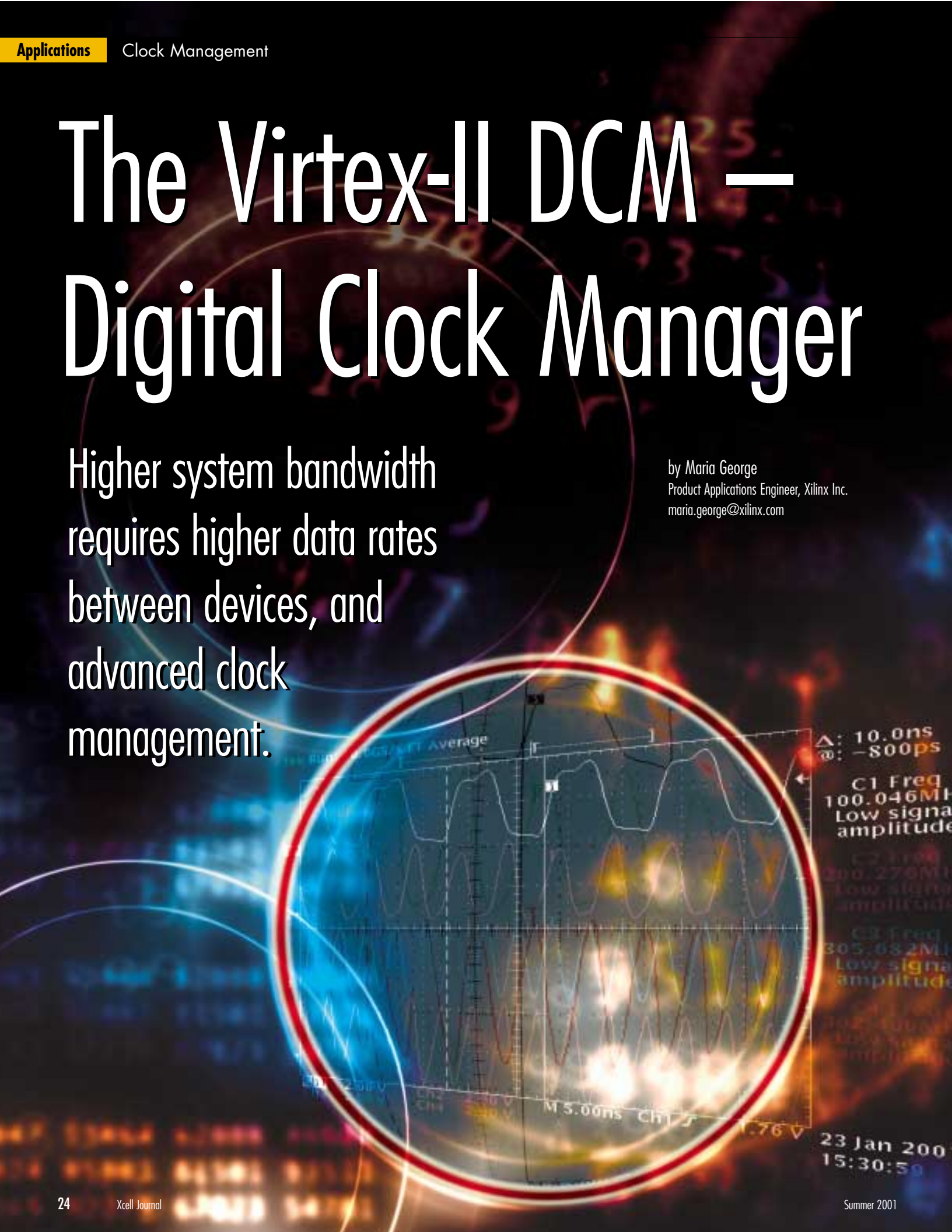

Efficient clock management is one of the keys to creating robust high-performance designs. When you have precise control of your clocks, your design is much easier to create and it is much more reliable. The Digital Clock Manager (DCM) in Virtex®-II FPGAs is the most advanced clocking technology available today, and it helps you create complex designs, quickly and easily.

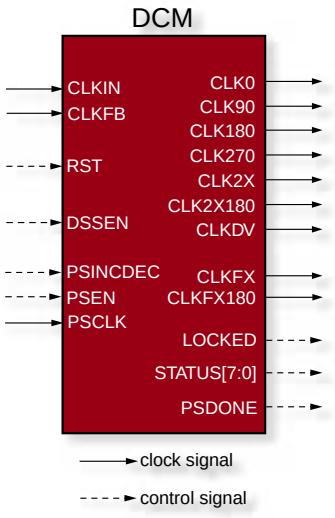

Figure 1 - DCM Block Diagram

The DCM uses digital delay lines for robust, high-precision control of clock phase and frequency. Up to four DCM clock outputs can drive global clock buffer inputs simultaneously, and all DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers. In addition, you can use the DCM outputs to generate board-level clocks, off-chip.

DCM Signal Description

Figure 1 shows all of the inputs and outputs of the DCM including control/status signals. The DCM has the following I/O signals:

- CLKIN input pin – Clock Input to DCM
- CLKFB input pin – Clock Feedback Input required to provide delay compensated output
- RST input pin – Resets the entire DCM
- DSSEN input pin – Enables the Digital Spread Spectrum (DSS) circuitry
- PSINCDEC input pin – Increments (when High) or decrements (when Low) the Phase Shift Factor
- PSEN input pin – Phase Shift Enable used in conjunction with PSINCDEC
- PSCLK input pin – Phase Shift Clock sourced by either CLKIN or any other clock source
- CLK0 output pin – Delay-compensated version of CLKIN
- CLK90 output pin – 90° out of phase with CLK0
- CLK180 output pin – 180° out of phase with CLK0
- CLK270 output pin – 270° out of phase with CLK0
- CLK2X output pin – Twice the frequency of CLKIN and in phase with CLK0
- CLK2X180 output pin – Twice the frequency of CLKIN and 180° out of phase with CLK0
- CLKDV output pin – Divided version of CLKIN
- CLKFX output pin – Frequency synthesized clock output (M/D * CLKIN)
- CLKFX180 output pin – 180° phase shifted version of CLKFX
- LOCKED output pin – Asserted High when all enabled DCM circuits have locked
- STATUS output pins – Indicates loss of the input clock, CLKIN
- PSDONE output pin – Indicates completion of requested Phase Shift

The FPGA configuration DONE output signal indicates the completion of configuration of the Virtex-II device. The DONE signal can be delayed until after the DCM has achieved lock, such as when all the DCM outputs have stabilized. This delay guarantees that the chip does not begin operating until the system clocks generated by the DCM have stabilized. This delay is accomplished by selecting the appropriate configuration option.

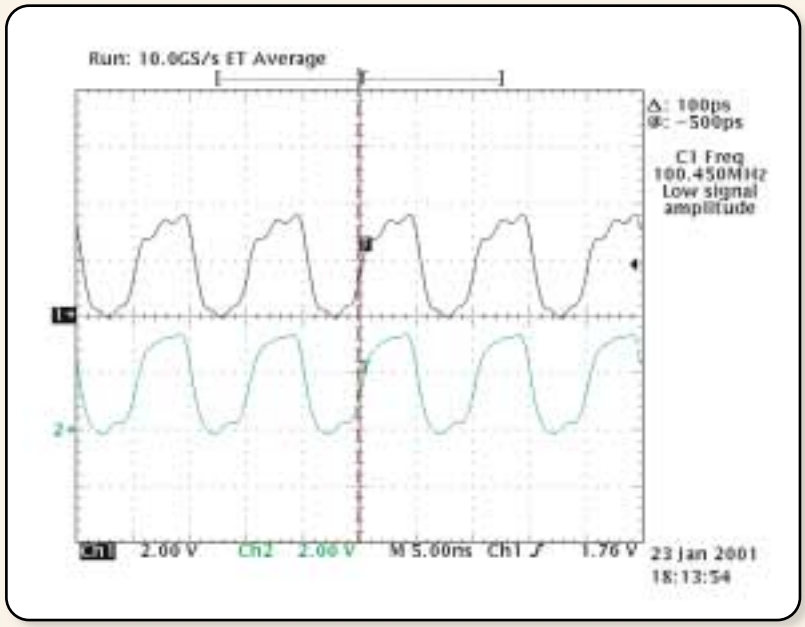

Figure 2 - DCM de-skewed outputs -Trace 1 is CLKIN (clock input to DCM), Trace 2 is CLK0 (delay-compensated DCM output

This diagram illustrates the phase alignment or lack of skew between the CLKIN input and the CLK0 output of the DCM.

DCM Features

The Virtex-II DCM provides a complete on-chip and off-chip clock generator, with powerful clock management features:

- **Clock De-Skew** – The DCM generates new system clocks (either internally or externally to the FPGA) that are phase-aligned to the input clock.
- **Frequency Synthesis** – The DCM can generate a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting** – The DCM can provide both coarse and fine phase shifting with dynamic phase shift control to compensate for voltage and temperature drift.

Clock De-Skew

Synchronous systems depend on precise clock distribution to achieve high performance and to avoid violating hold-time requirements. The Xilinx architecture, clock buffers, and so on, ensure low-skew clock signal distribution both within the Virtex-II device (using the clock distribution network) and externally on a system/board level. The well-buffered global clock distribution network minimizes clock skew, regardless of loading differences.

The Virtex-II DCM provides a fully digital, dedicated on-chip de-skew circuit with zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. The de-skew circuitry has an input frequency range of 24 MHz to 420 MHz, and an output frequency range of 1.5 MHz to 420 MHz. The de-skew circuitry can tolerate up to 1 ns of skew, cycle to cycle.

By monitoring a sample of the output clock (CLK0 or CLK2X), the de-skew circuit automatically compensates for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device. By taking advantage of the de-skew circuit to remove on-chip clock delay, you can greatly simplify and improve system-level design involving high-fanout, high-performance clocks. Figure 2 shows the waveforms of the de-skew outputs with an input clock frequency of 100 MHz.

The de-skew feature can also act as a clock mirror. By driving the CLK0 or CLK2X output off chip and then back in again, the de-skew feature can be used to de-skew a board-level clock serving multiple devices.

Frequency Synthesis

To avoid high-frequency clock distribution on printed circuit boards (PCBs), system-clock multiplication and division are required. Frequency synthesis in the DCM gives you the flexibility to choose multiplication and division factors that are integers (whose ranges are specified in the data sheets). This feature can help reduce the number of high-speed system-level clocks in your design. Frequency synthesis enables you to use a single system-level clock to generate any frequency within the operating range.

Besides the flexible frequency synthesis described above, the DCM also offers basic frequency synthesis. For example, clock multiplication by 2 (CLK2X, CLK2X180), and clock division (CLKDV) of the user source clock by up to 16. Any one of the following numbers can divide the clock input to the DCM: 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, or 16.

Clock multiplication gives you a number of design alternatives. For example, a 100-MHz source clock on your PCB, doubled on-chip by the DCM, can drive an FPGA design operating at 200 MHz. This technique simplifies board design because the clock path on the board can be slower, giving you better signal integrity.

With a multiplied clock you can also do time-domain-multiplexing – using one circuit twice per clock cycle, which con-

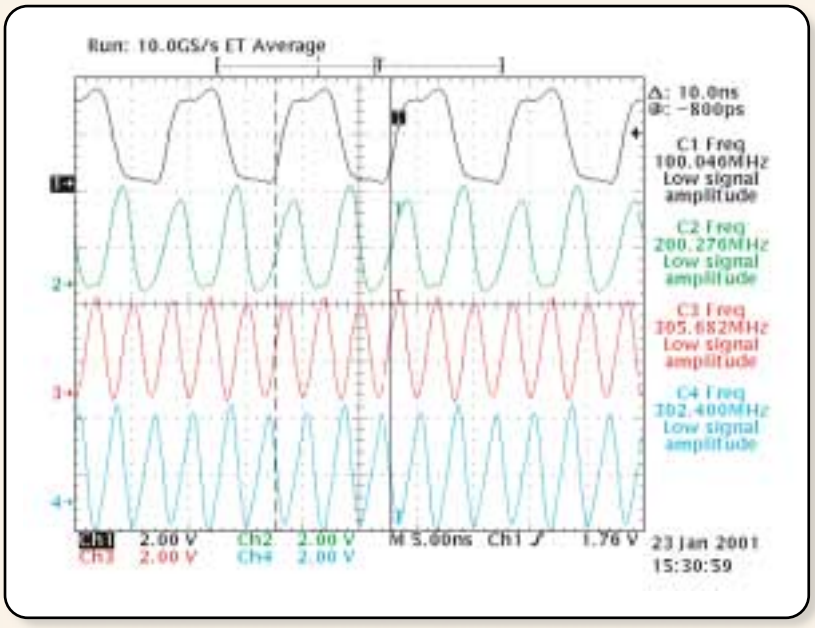

Figure 3 - DCM frequency synthesized outputs – Trace 1 is CLK0 (delay-compensated DCM output), Trace 2 is CLK2X (twice the frequency of CLK0 and phase alligned with CLK0), Trace 3 is CLKFX (frequency synthesis output with M=3, D=1 and phase alligned with CLK0), Trace 4 is CLKFX180 (180° out of phase with CLKFX).

This diagram shows the frequency synthesizer generating a clock output that is 3X the frequency of input clock, CLKIN.

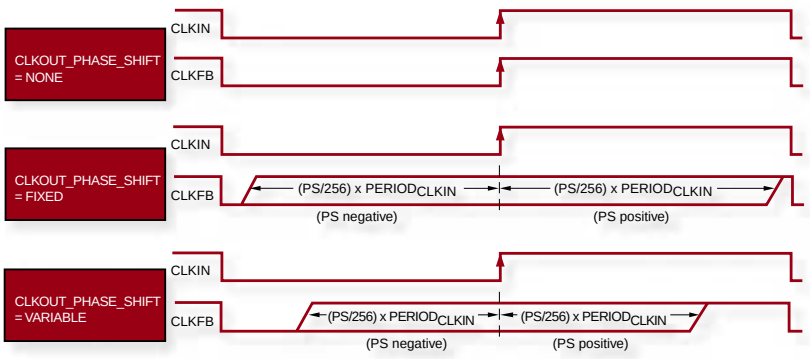

Figure 4 - Phase shift effects

sumes less resources than two copies of the same circuit.

Flexible Frequency Synthesis is implemented by using the CLKFX and CLKFX180 outputs. The frequency of these clocks equals the input clock frequency (F) multiplied by M/D. M, the numerator, is the multiplication factor and D, the denominator, is the division factor. These two counter-phase frequency-synthesized outputs can drive global clock routing networks within the device; they are well-buffered to minimize clock skew due to differences in distance or loading. To de-skew these outputs, a feedback signal must be provided to the CLKFB input of the DCM (either CLK0 or CLK180).

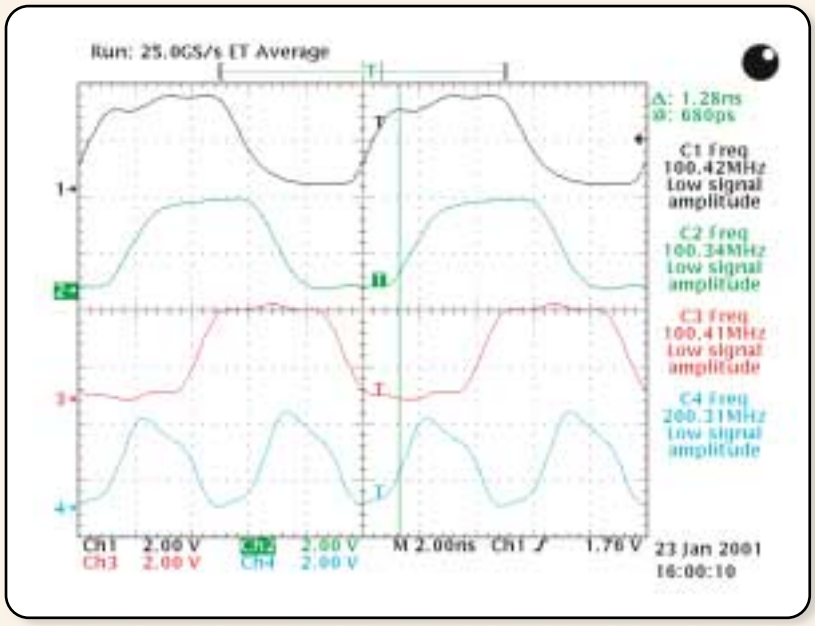

Figure 5 - DCM phase shifted outputs – Trace 1 is CLKIN (100 MHz clock input to DCM), Trace 2 is CLK0 (delay-compensated DCM output with a fine phase shift of 1.3ns with respect to CLKIN), Trace 3 is CLK90 (90° out of phase with CLK0), and Trace 4 is CLX2X (twice the frequency of CLKIN and in phase with CLK0).

This diagram shows the fine phase shift feature of the DCM with the phase shift value set to 33 [(33 x 10 ns)/256 = 1.3 ns]. All the DCM outputs shown are 1.3 ns phase offset with respect to CLKIN.

As an example, if the input frequency F = 50 MHz, M = 333, and D = 100, the generated output frequency is correctly 166.50 MHz, even though both (333 x 50 MHz = 1.665 GHz), and (50 MHz/100 = 500 kHz), are far outside the range of the frequency output. (Note that M and D values have no common factors and therefore cannot be reduced).

Figure 3 shows the waveforms of the frequency synthesized outputs with M = 3, D =1 and F = 100 MHz.

Phase Shifting

The DCM also allows you to shift the phase of clock signals, so you can adjust the setup and hold times of I/O signals. High-resolution phase shifting has the following characteristics:

- The DCM provides quadrature phases of the source clock (CLK0, CLK90, CLK180, and CLK270) which can be used simultaneously.
- A phase shifted output with a resolution of 50ps or 1/256th of the input clock period can be created; fine phase shifting affects all the outputs of the DCM.
- The phase shift can be fixed (established by configuration) or dynamically adjusted after configuration.
- The dynamic phase adjustment feature can be used to optimize clock-to-out by adjusting the set-up and hold times while the system is running.

The equation for the phase shift is:

CLKIN_CLKFB_skew=(Phase_Shift_Value/256) x PERIOD CLKIN

Figure 4 shows the phase shift effects in the fixed and variable modes of operation.

The phase shift is a fraction of the clock period (N/256). The phase shift granularity is the greater of the two limiting factors: the minimum delay line step size (≅ 50 ps), and the minimum phase shift step size (1/256 x input clock period). The maximum phase shifting range is the lesser of the two limiting factors: the maximum delay line range (≅ 10ns for FIXED mode and ≅ 5 ns for VARIABLE mode), and the maximum

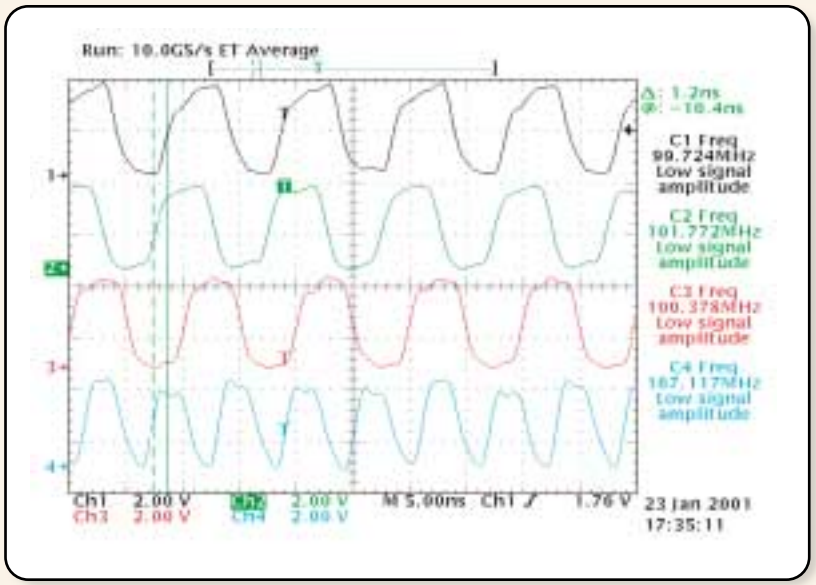

Figure 6 - DCM Phase Shift and Frequency Synthesis Outputs – Trace 1 is CLKIN (100 MHz DCM clock input), Trace 2 is CLK0 (delay-compensated DCM output with a negative fine phase shift of 1.2ns with respect to CLKIN), Trace 3 is CLK90 (90° out of phase with CLK0), and Trace 4 is CLKFX (frequency synthesis output with M=5, D=3 and phase alligned with CLK0).

This diagram shows both the fine phase shift and the frequency synthesis feature being used simultaneously in the same DCM. The phase shift value is set to -30 [(30 x 10 ns)/256 = 1.2 ns]. The transitions on all the DCM outputs shown occur 1.2 ns before the transition on CLKIN due to the negative phase value.

phase shift range (255/256 ≅ 1 clock period).

Figure 5 shows the phase shift in the DCM de-skew outputs with a phase shift value of 33: (33 x 10ns)/256 = 1.3 ns where 10 ns is the clock period.

Figure 6 shows the waveforms of the DCM outputs with both the phase shift and the frequency synthesis feature being used simultaneously. In Figure 6, the phase shift value is -30, or 1.2ns: (30/256)x10ns = 1.2 ns, where 10 ns is the clock period, M = 5, and D = 3.

The dynamic high-resolution phase shifting feature of the DCM makes Virtex-II devices the only FPGAs in the industry to offer a superior clock management solution. The smaller density Virtex-II devices could justifiably be used just for the DCM alone, replacing devices such as the Cypress RoboClock, or the IDT TurboClock.

Table 1 is a comparison of the Virtex-II DCM with Cypress RoboClock.

DCM Applications

The advanced frequency synthesis feature can be used to generate frequencies in key applications, such as:

- 10b/8b (10 bit to 8 bit encoding), with 100 MHz input and 125 MHz output
- FEC code rates, such as 528/512, and 8/7

The phase shifter high-resolution phase adjustment feature can be used for:

- Modifying clock-to-out timing
- Maximizing setup and hold time margins
- Clock and data recovery for OC-3 applications
- Master/slave, hot/standby switching

All of these features can be accessed simultaneously in a single DCM.

Conclusion

The Virtex-II DCM is the most reliable and easy to use clock management technology available. The DCM is a digital signal processor, processing phase information every clock cycle with completely predictable results. When operating within the specified environmental limits, the DCM is not affected by voltage and temperature changes, and unlike a PLL, the DCM does not require special power and ground pins or external networks on the PCB.

	VIRTEX-II DCM	CYPRESS Roboclock+ CY7B9911V
Maximum Frequency	420 MHz	110 MHz
Output Skew Range	+/- 360° (Full Period)	18 ns
Skew Resolution	Period/256	≅ 1 ns/step
In-System Adjust	Yes	No
Device Integration	Up to 12 DCMs Integrated On-Chip	32-pin PLCC
Customer Value	Higher Performance Increased Flexibility Higher Integration	

Table1 - Comparison of Virtex-II DCM and Cypress RoboClock