Video Demonstration Board

A glimpse at broadcast video router/mixer functions inside a Virtex-II Platform FPGA

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Virtex-II FPGAs are the ideal platform for developing video applications. No other FPGA can provide the combination of 18x18 2's complement signed block multipliers, Digital Clock Managers (DCM), glitch-free global clock multiplexers, Bus LVDS I/O, and DDR I/O, which are all essential for the pixel-rate math and the high bandwidth needed for managing and manipulating video data streams.

To demonstrate the many video-friendly features and the video IP (application module software) of the Virtex-II FPGA family, we've developed a demonstration board that provides a Virtex-II FPGA interfaced to the essential video support functions such as:

- Large, fast, frame buffer memories
- Video inputs (4 NTSC or PAL, CCIR 601/656 4:2:2 format)
- Video outputs (1 NTSC or PAL, CCIR 601/656 4:2:2 format)
- Video outputs (1 RGB, 24 bit format)
- Network connection
- System configuration devices.

There are many routing/mixing functions currently available as intellectual property for the demonstration board, with room for future exploration of more advanced video algorithms. This board can also be used as a convenient video IP development and experimentation system.

Brief Description

The Virtex-II video demonstration board is a simple version of a video router/mixer. The board allows conversion of several, high bandwidth video streams from various video sources, into a common format and color space. Then, using high-speed, pixel-rate, pipelined math, you can manipulate and merge the video streams. The Virtex-II FPGA provides high bandwidth access to devices and large memories, high data rate arithmetic, and the necessary control logic.

The Virtex-II architectural features highlighted by the demonstration board include:

- 18x18 2's complement, signed block multipliers which provide the high speed math capability
- Digital Clock Managers (DCM) which provide clock de-skew, frequency synthesis, clock phase shifting, and EMI reduction logic
- Global clock multiplexer buffers which provide clock multiplexing, clock buffering, and distribution
- A Network connection to a Local Area Network (LAN) and the Internet so you can remotely update the Virtex-II internal algorithms
- Configuration from compact flash memory providing a way to update and store future changes to the programming bit stream of the Virtex-II device.

Supported Effects

Using the Video Demonstration board, you can mix video streams, from many different sources, in interesting ways. For example, you can easily perform the all-too-familiar video fade or alpha blend from one scene to another, where the current video stream (such as a basketball game live feed from a satellite), slowly disappears and a new scene appears (such as a commercial).To accomplish this, the pixels in one scene are multiplied by a fraction (alpha) while the pixels in the other scenes are multiplied by "one minus the fraction" (1-alpha). Varying the fraction from zero to one produces the blending effect.

The master controller or technician viewing the different video input streams and the resulting video output executes video commands to manipulate the input streams. Thus, just as in a typical video production, the master controller queues up an effect, such as "going to a commercial" and the FPGA executes the mathematics behind the command.

The types of broadcast video effects currently supported are:

- Fade to/from black
- Fade through black
- Dissolve
- Horizontal wipe
- Vertical wipe.

Over time, more effects will be available. These expanded effects will appear on the Xilinx website as video application notes.

Board-Level Block Diagrams

The video demonstration board has a number of input sources of live video and a number of separate frame buffers to support the increased amount of storage and bandwidth needed by the extra live streams. An audio codec is supported for embedded audio as well as supporting potential audio algorithm updates from a network connection. The board can also drive a TV monitor. A block diagram is shown in Figure 1.

Board Features

- Four sources of live video input (either NTSC or PAL)
- Composite and S-Video inputs (from a camcorder)
- Separate fixed graphic image loaded from Compact Flash memory
- Real-time video output (XVGA touch-screen and/or NTSC/PAL output)
- Composite and S-Video NTSC/PAL video and RGB output
- Video effects (fades, dissolves, wipes, and so on)
- Compact Flash FPGA configuration
- Touch-screen-selected video source and effects. The touch screen is enabled by RS232 port; video source selection and effects are also pushbutton enabled
- Audio switching
- 10 Base-T and 100 Base-TX Ethernet support
- XC2V6000FF1517 Platform FPGA support
- Universal power supply module.

Verilog Modules

The following list of functions, written initially in Verilog, are available for use with the Virtex-II Video Demonstration Board:

- User Interface – Push button scan affects what is seen on the output screen
- ZBT memory interface controllers – Drives data to and from the FPGA and ZBT RAM
- XVGA controller – Outputs data to a regular computer monitor (self adapts for NTSC or PAL). The module will work with any resolution given the right amount of memory; the 4-channel version will support 1024 x 768, the 1-channel version runs at 800 x600
- Clock generation – Generates four different clock rates, supporting various video functions, the audio codec at 25.576MHz (if the DCM will work with the required ratios), and 25MHz for Ethernet
- Line-field decoder – Assists in identifying frame and field parameters
- I^2C serial interface standard – Loads initialization parameters from the FPGA to the video peripheral chips
- On chip line buffers – Allowing algorithm pixels to be processed vertically
- Interlace fields to non-interlace frames conversion
- Color space conversion
- 4:2:2 to 4:4:4 format conversion
- Up/down scaling of thumbnails
- Blend and fade between frames (video processing).

Check the Video Applications website for the latest new functions. Future algorithms may include compression of video data, detection and enhancement of video imagery via DSP functions, and additional flexibility to support the constantly emerging video standards.

Conclusion

The advanced system-level features and the growing list of video-related Intellectual Property make the Virtex-II FPGA family an ideal choice for video applications. And now, the Virtex-II Video Demonstration Board gives you everything you need to quickly and easily explore video applications. For more information on the demonstration board, visit the Xilinx website at: www.xilinx.com.

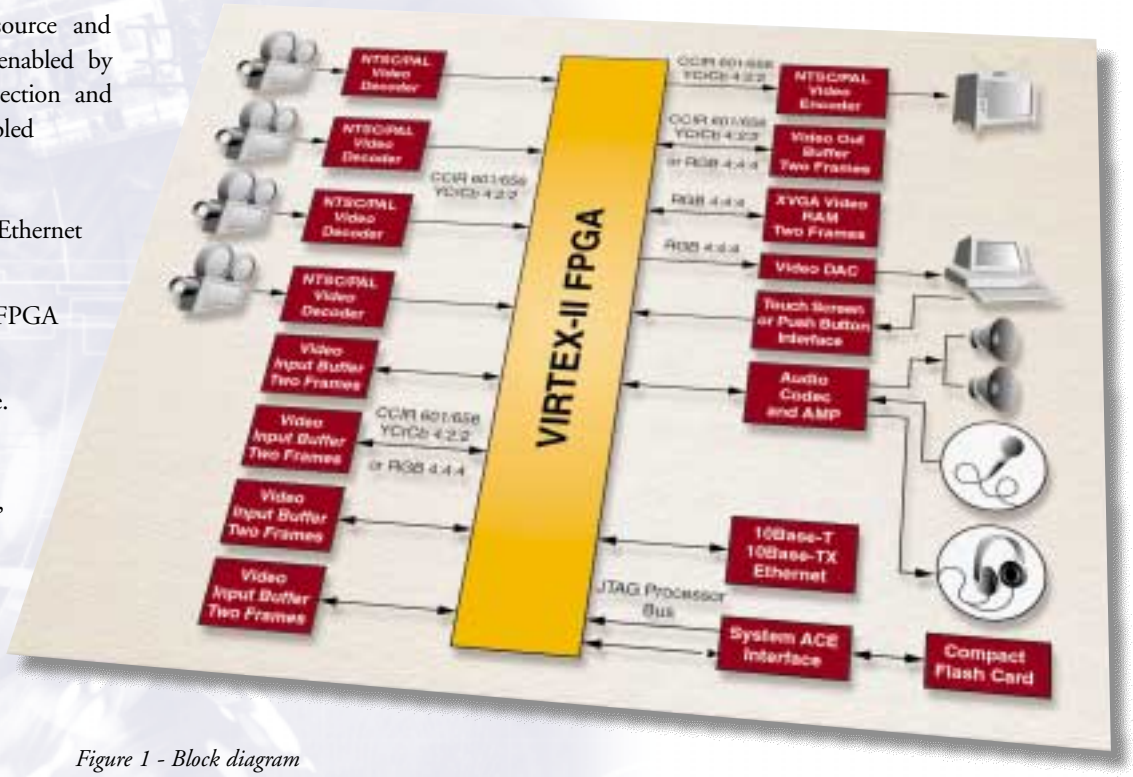

Figure 1 - Block diagram