IBM's New PowerPC Strategy Roadmap

It's exactly what you'd expect from IBM.

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It is not by accident that ideal targets for IBM PowerPC™ technology include wired and wireless networking, storage, and pervasive computing applications. It's all part of a master strategy to focus both today's and tomorrow's industry leading technology on PowerPC products – to meet the performance, power, and price needs of these ever-dynamic and diverse applications.

The focus of IBM's strategy centers upon both technology and design expertise. Underlying this focus is a strong and long-term commitment to leveraging the PowerPC architecture and designing with standard interfaces, such as RapidIO™, PCI/X, and Ethernet. The goal of this strategy is to assure the continuation of a product portfolio heritage of being core-based, power-efficient, scaleable, and software transparent.

The melding of IBM's advanced technology, PowerPC products, and SoC capability will establish a hallmark in the battle for mindshare and marketshare. As market opportunities evolve for higher performance and/or lower power devices, IBM will be poised to address these seemingly insatiable needs.

THE RAPIDIO INTERCONNECT ARCHITECTURE, DESIGNED TO BE COMPATIBLE WITH MOST POPULAR INTEGRATED COMMUNICATION PROCESSORS, HOST PROCESSORS, AND NETWORKING DIGITAL SIGNAL PROCESSORS, IS A HIGH PERFORMANCE, PACKET-SWITCHED, INTERCONNECT TECHNOLOGY. IT ADDRESSES THE HIGH-PERFORMANCE EMBEDDED INDUSTRY'S NEED FOR RELIABILITY, INCREASED BANDWIDTH, AND FASTER BUS SPEEDS IN AN INTRA-SYSTEM INTERCONNECT. THE RAPIDIO INTERCONNECT ALLOWS CHIP-TO-CHIP AND BOARD-TO-BOARD COMMUNICATIONS AT PERFORMANCE LEVELS SCALING TO TEN GIGABITS PER SECOND AND BEYOND.

IBM's PowerPC cores, microprocessors, and integrated products meet the unique needs of an increasingly diverse marketplace. PowerPC chips offer state of the art

technology in a variety of configurations to provide the optimal mix of performance, power, functionality, and size. And because of our core-based design philosophy, IBM customers can quickly and easily differentiate their products in the marketplace, and still maintain flexibility and software transparency across generations of devices.

IBM has been a leader in awarded patents for many years, largely as a result of IBM Microelectronics contributions. Among the more recent of these contributions are several dozen patents directly related to three chip breakthroughs – silicon germanium (SiGe), silicin-on-insulator (SOI), and Low-K Dielectric.

Just as IBM led the industry with its copper process technology, these new process technologies will be the catalyst for even greater performance and low-power advances in the semiconductor industry.

Key to enabling a high level of flexibility is the IBM CoreConnect™ on-chip bus architecture, which is becoming a defacto industry standard. CoreConnect provides a standardized method for assembling pieces of chip designs from diverse suppliers to facilitate an open SoC design process that encourages the development of reusable IP. Currently, this bus structure is licensed by over 40 IP providers, and is the basis for numerous IBM standard, application specific, and custom devices. Forthcoming enhancements include higher bandwidth and crossbar functionality, which will marry well with our next-generation CPU cores and our planned addition of performance-enhancing IP like RapidIO and high-speed serial ports.

Enhancing IBM's strategy is a commitment to the PowerPC architecture. The latest enhanced version, called PowerPC Book E, has been refined to provide 64-bit capabilities, increase flexibility, and address the unique demands posed by embedded systems. Book E is a new definition of the PowerPC architecture, one that maintains compatibility with applications developed for the original PowerPC architecture.

What's technology got to do with it?

Almost everything. It's what boosts performance... throttles power consumption... and enables smaller devices. In a nutshell, technology is a key ingredient to the ever-elusive faster, smaller, and cheaper semiconductor solution.

Today's copper process, silicon-on-insulator, and Low-K Dielectric technologies have fostered higher levels of performance and lower power dissipation than were previously attainable. This elevation of performance is currently being realized in IBM's highest performance servers and workstations for data processing and electronic commerce through IBM's stand-alone and system-on-chip (SoC) processors.

The application of new process technologies is crucial to the development of processor engines that will meet the performance and power needs of next-generation applications. And nowhere will the infusion of new technology be more appreciated than in the relatively new "pervasive computing." This includes handheld and embedded products such as smart phones and Internet appliances for business professionals and consumers. In this arena, both "high performance" and "low power consumption" are of utmost importance. To continue meeting this challenge, IBM is focusing its technology resources on PowerPC embedded processors that will distinguish themselves by their enviable power/performance ratios as well as their high integration of critical IP.

Conclusion

As a chief architect of the PowerPC Architecture, IBM has been at the forefront in the evolution of microprocessor design, semiconductor technology, and SoC advances in the industry. IBM likes its position as a pioneer and industry leader – and has no desire to relinquish its position. You are invited to meet IBM at any of its milestones, as it advances toward an ultrascalar, 2+ GHz-processor engine. It's exactly what you would expect from IBM.