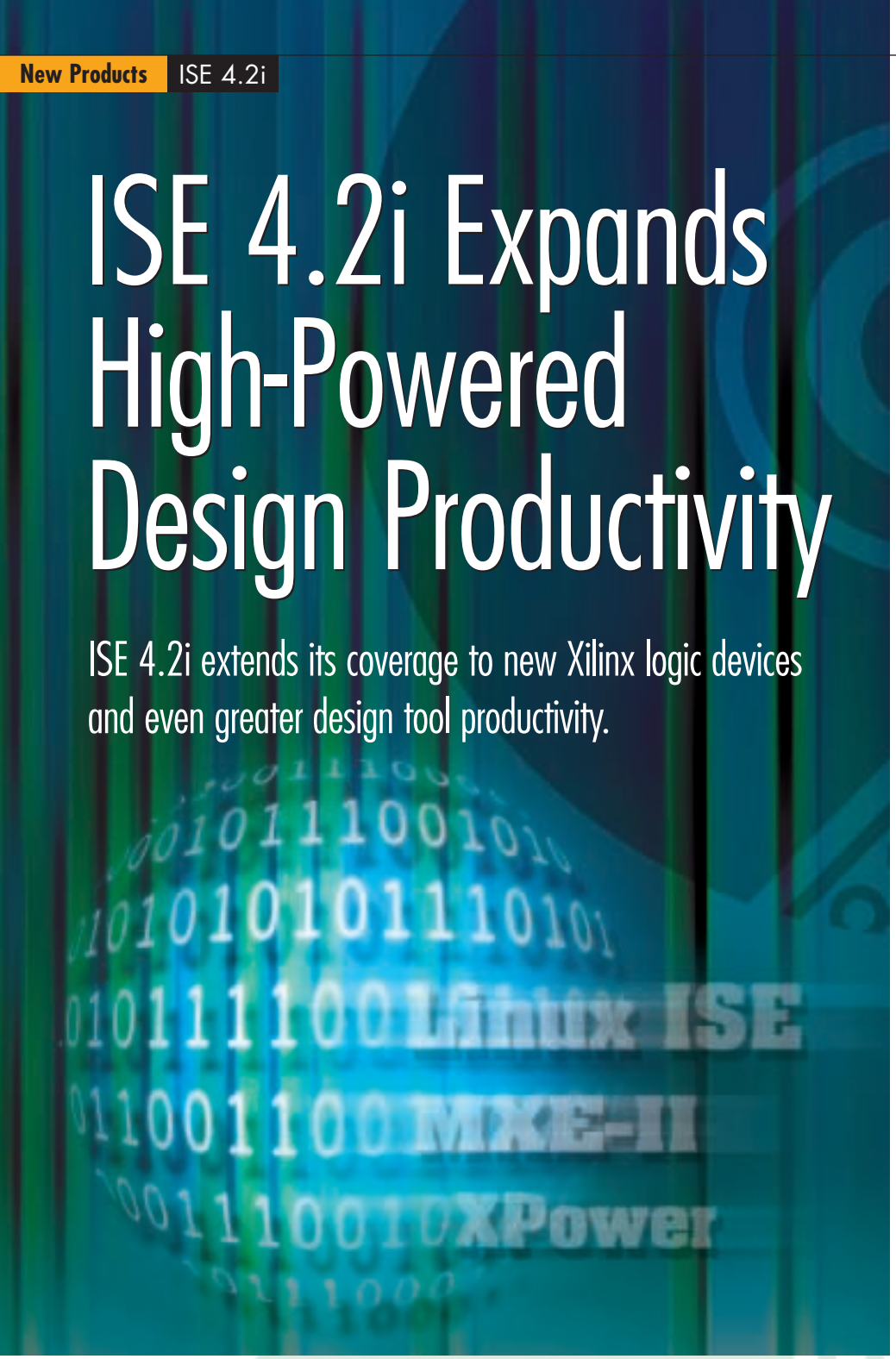
ISE 4.2i Expands High-Powered Design Productivity

ISE 4.2i extends its coverage to new Xilinx logic devices and even greater design tool productivity.



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In February, Xilinx released Integrated Software Environment version 4.2i logic design software. ISE 4.2i delivers several new capabilities that make it the most complete package available for programmable logic design. Building on the advances of ISE 4.1i, released this past August, version 4.2i offers several advantages in particular to designers looking at embedded logic systems and high-speed signal challenges:

- Linux ISE
- Expanded device support
- High-speed design support
- Partial reconfigurability
- Streamlining XPower performance
- MXE-II

Linux ISE

ISE version 4.2i is the first version of Xilinx design software to run on the Linux operating system. Now, you can run Xilinx implementation tools on Linux Red Hat version 7.2, including the Wine windows application layer. With the addition of the Linux operating system, you now have one of the widest choices possible in design system platforms and implementation tools for programmable logic design.

Expanded Device Support

ISE 4.2i includes the latest device support for all of the Xilinx families, including the new Virtex-II PRO™ product line.

- The Virtex-II PRO Platform FPGA is the only programmable device available with 3.125 Gbps serial I/O – and anywhere from zero to four IBM PowerPC™ 405 microprocessors embedded in the device fabric.
- ISE 4.2i comes ready to implement Virtex-II PRO functions, as well as those available in the recently announced CoolRunner™-II and Spartan™-IIE device families.
- ISE 4.2i also includes the new "-6" speed grade for the industry's fastest Virtex-II FPGAs.
- By delivering FPGA and CPLD device support from a single design product line, ISE gives you an easy way to move up or down device families without having to load or relearn new software.

High-Speed Design Support

With Virtex-II PRO Platform FPGAs, you can now drive design I/O at speeds up to 3.125 Gigabits per second – a first in programmable logic. And ISE 4.2i comes ready to help you realize that high-speed I/O potential quickly and easily. All of the implementation tools, the pin planner, and timing and constraints editors in ISE 4.2i have been enhanced to simplify the implementation of the high-speed I/O of the Virtex-II PRO devices. And the synthesis tools can optimize the paths to and from the multi-gigabit transceivers

(MGTs), a capability unique to ISE 4.2i design software.

The ISE 4.2i libraries also support instantiation of 1, 2, and 4-byte flavors of the high-speed I/O protocols supported by Xilinx.

Xilinx and Cadence Design Systems have jointly developed high-speed design kits. These kits include software components and design aids to help you use the Virtex-II PRO multi-gigabit transceivers. The kits also contain HSpice compatible models for analyzing PCB electrical trace effects coming off the high-speed Virtex-II PRO I/O pins. By combining the new HSpice models for the Virtex-II PRO MGTs, IBIS models for all our FPGA device families and SWIFT models describing the behavior of the PowerPC™ microprocessor and multi-gigabit transceivers, Xilinx provides support for analyzing your FPGA, even after it's been programmed and ready for the board.

Partial Reconfigurability

Continuing its long string of firsts in the programmable logic industry, Xilinx has added a new capability to both the ISE software family, as well as the Virtex-E and Virtex-II product lines – Partial Reconfigurability. Introduced in ISE 4.2i, Partial Reconfigurability allows either a Virtex-II or Virtex-E FPGA to be partitioned so that part of the device can be reprogrammed, while the remainder of the FPGA continues to run.

Partial Reconfigurability works through the Modular Design option for ISE. Using Modular Design, the overall design can be partitioned into sub-modules that can be implemented independently of each other. Once a module is completed, its timing and performance are locked down while the remaining modules are being finished, delivering faster overall design completion.

With the addition of Partial Reconfigurability, the device can also be partitioned where electronic functions make the most sense. Then later on in the field, one partition can be reprogrammed while the remainder of the FPGA continues to run. Products can be updated for new functionality while still in the field, and the product doesn't have to be taken offline while new functionality is loaded.

Streamlining XPower Performance

XPower, an ISE feature that estimates the power consumption of FPGAs and CPLDs, has also been streamlined for better performance. VCD simulation files now read in much faster than previous versions, allowing for quick and accurate setup of input signal activity. And XPower now supports the new CoolRunner-II family of CPLDs.

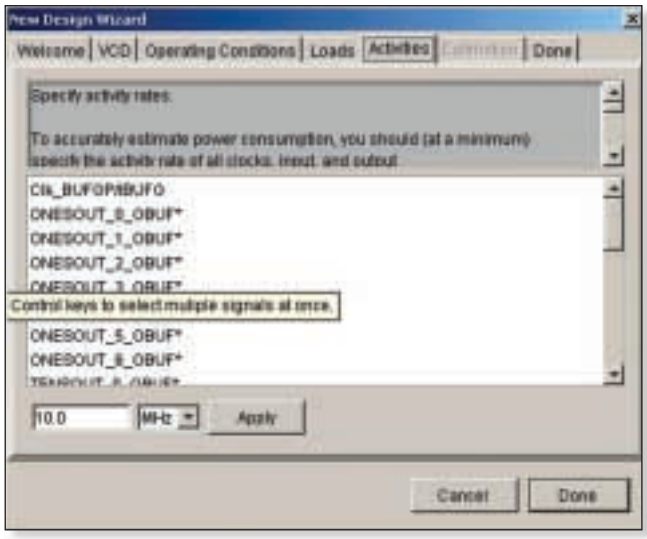

Figure 1 - XPower New Design Wizard

XPower New Design Wizard

Most important, in the ISE 4.2i version of XPower you will also find the "XPower New Design Wizard," shown in Figure 1. The wizard helps XPower users read in design data, input VCD files if available, set default parameters, and identify and then set specific input activity rates – all in a tab-delineated form that's easy and intuitive to use. This new wizard helps you get more accurate thermal estimates faster.

MXE-II Simulation Software

ModelSim™ Xilinx Edition II (MXE-II) simulation and debug software is now available to all ISE customers. Based on Model Technology's ModelSim 5.5e software, MXE-II delivers the additional simulation capacity and performance needed to verify the ever-increasing repertoire of faster and denser programmable devices. These additional capabilities are user-transparent, requiring no time-consuming learning curves. In fact, MXE-II simulation software requires less from the end user because of the integration with ISE's HDL Bencher™ graphical test bench generation environment. HDL Bencher waveforms are automatically translated into VHDL or Verilog, simulated with MXE-II, and the expected results can be back-annotated into the original waveforms. Discrepancies between expected and actual results are also highlighted, expediting dynamic verification.

Moreover, MXE-II includes optimized libraries that deliver faster simulation runtimes than competing technologies for post-route non-timing/timing simulation. These libraries are available for all the device families supported in ISE. These enhancements – coupled with a new, fully automated licensing process – significantly expand MXE-II's usefulness to a broader set of PC-based customers.

MXE-II performs 33% better than its predecessors. That, plus the doubling of MXE-II's capacity, makes it ideal for the verification of all types of Xilinx devices, including the CoolRunner-II, Spartan-IIE, and Virtex-II families.

Conclusion

ISE 4.2i continues to deliver the speed you need – from the simplest designs in the smallest device families to the most demanding high-speed, embedded system designs. Upgrade today to get the most leading edge capabilities available for your programmable logic products. You can find out more about ISE 4.2i at *www.xilinx.com/ise/42i*. For a recorded e-learning lecture on ISE 4.2i, go to *www.xilinx.com/support/training/north-america-home-page.htm*.