Speed Up Your Design Verification

You can develop complete, timing-constrained HDL and Verilog test benches in minutes with the HDL Bencher component of Xilinx ISE 4.1i.

by Ricky Escoto
Manager, Product Line Marketing
ricky.escoto@xilinx.com

The HDL Bencher™ testbench generator delivers shorter time to market and increased engineering productivity. Using this automated testbench development tool, you get fast verification of HDL-based FPGA and CPLD designs. The new HDL Bencher generator is fully integrated with the Xilinx Integrated Software Environment (ISE) 4.1i family of design tools. HDL Bencher software is so easy to use that you don't have to know anything about hardware description languages to develop testbenches.

HDL Bencher Overview

With the HDL Bencher software, you can generate complete, self-checking VHDL or Verilog™ testbenches in just minutes. All you have to do is input a VHDL or Verilog design, along with the timing parameters that must be met by synthesis. You then describe the stimulus and expected behavior using the built-in pattern generator, the waveform editor, and the spreadsheet-based graphical user interface (GUI). The output is a simulation-ready testbench with library declarations, stimulus and check statements, and error reporting routines.

What's New in This Version

The HDL Bencher testbench generator has been enhanced to improve the overall testing process. This version features an improved user interface, faster testbench specification, and compressed testbench output.

Interactive Debug and Simulation

The HDL Bencher tool now includes automatic simulation through the Xilinx ISE framework. Simply draw the stimulus, then generate the expected results, and export a self-checking testbench automatically, as shown in Figure 1. Use the domain knowledge inherent in the HDL source, and in your head, to quickly produce regression level test cases. Mismatches between expected and actual values are highlighted automatically.

ISE Integration and Enhanced File Support

The HDL Bencher tool has been completely integrated with ISE 4.1i software. Integration includes automatic launching of the HDL Bencher software from ISE 4.1i, automatically adding waveform and testbench sources, and verification of large, multi-source file designs.

Faster and Better Performance

We've reduced File Open time by 20% and improved graphics display by 300%. The major effect of these speed enhancements is a faster, crisper application – ideal for large FPGA testbenches.

Faster Simulation

To improve regression run times, we've modified testbench output in a number of ways, resulting in testbenches typically 90% smaller than those generated by the previous version of HDL Bencher software:

- The clock process has been separated from assignments and assertions (clocked designs) to minimize code size.
- The delays between output assertions and input assignments have been packed to reduce code size.

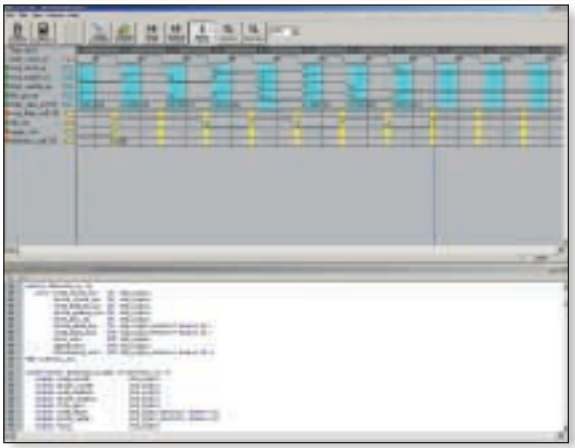

Figure 1 - The HDL Bencher 2.0 GUI

All-Level Verification

ISE 4.1i now features a waveform-based test environment. The same behavioral waveform file created in the HDL Bencher software is automatically updated to verify post-route and post-synthesis designs. Signal types are automatically remapped, and port definitions are resolved automatically.

Conclusion

The HDL Bencher testbench generator for ISE 4.1i supports integrated output simulation through ModelSim™ software, thereby closing the loop on its mission to provide seamless and fast testbench generation for Xilinx ISE applications

The HDL Bencher testbench generator is available at no charge to all Xilinx customers. It is fully integrated into Foundation™, BaseX, and WebPACK™ ISE 4.1i software. For more information on the ISE family of products, log on to *www.xilinx.com/ise/xcell/*.