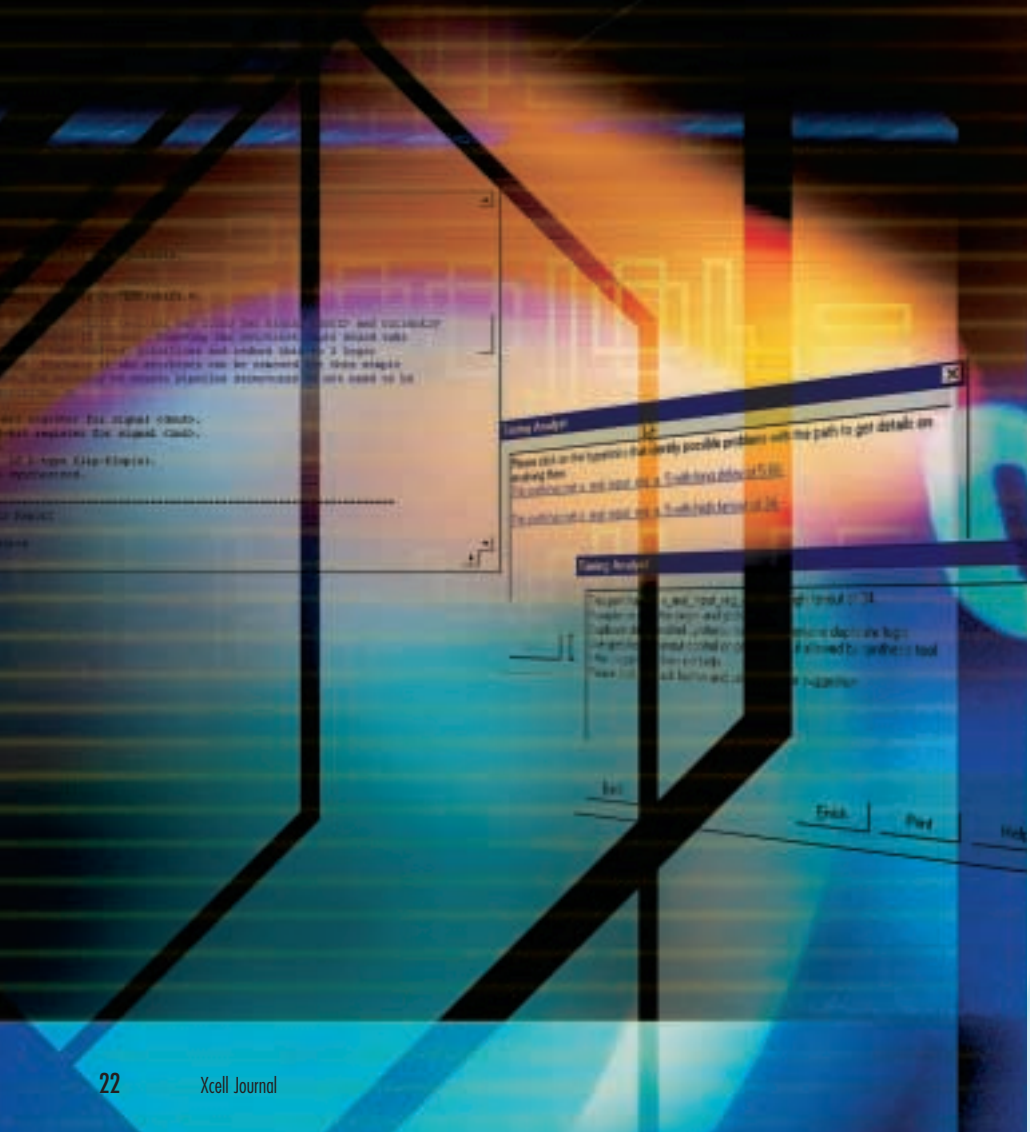
ProActive Timing Closure Delivers up to 133% Better Device Performance

Take a look under the hood at one of the technology innovations embedded in ISE 4.1i and learn how it can meet your need for speed.



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As network and bandwidth capabilities continue to increase, the demands placed on design performance rise incrementally. These design pressures are leading to changes in programmable logic design tools – and Xilinx is leading the way with a new set of timing technologies, collectively known as ProActive Timing Closure.

Introduced in all configurations of the new release of Xilinx Integrated Software Environment (ISE) 4.1i, ProActive Timing Closure is setting new benchmark standards reaching design speeds up to 133% faster than ISE 3.1i. Furthermore, our internal benchmarks have shown that ProActive Timing Closure in ISE 4.1i can process on average as many as 100,000 gates per minute. That equates to millions of gates per hour for high-density designs.

Advanced Place-and-Route Algorithms

At the heart of ProActive Timing Closure are enhancements to the place-and-route algorithms. Placement now begins by scanning your design for critical data paths and attempting to place those data paths first – thus, improving timing for the critical portions of the design first, and improving overall timing.

Extra-Effort Routing Mode

The place-and-route tools now also include a new "extra-effort" mode. In this mode, the routing tool analyzes the design for nets that did and did not meet timing. Then the extra-effort mode automatically requests a new placement for areas that didn't meet timing. The router then attempts to route these newly re-placed areas – an operation that is transparent to the user.

The new place-and-route algorithm can result in fewer iterations, and more successful place-and-route passes earlier in the design cycle. Some customers are reporting they can use this advanced timing technology to generate several successful layouts of a particular design in the time it used to take to do one pass.

Directed Routing for IP

As IP has grown in speed and complexity, the need for more visibility into place-and-route directions for IP has grown accordingly. Today's POS-PHY and optical interface designs contain many critical data paths. And marrying your favorite synthesis tool to the increasingly complex and capable Xilinx device fabrics only increases the challenge.

The Directed Routing component of PTC is designed to help solve that challenge. Directed Routing brings a new level of visibility into the configurable logic blocks (CLBs) in the Xilinx device. Directed Routing describes in detail the placement and routing that should be used to achieve successful and repeatable IP implementation.

Physical Synthesis for FPGAs

Last year, Xilinx announced the first physical synthesis integration for FPGA design. ISE 4.1i continues the expansion of FPGA physical synthesis. With PTC, both Synplicity®'s Amplify™ and Exemplar Logic®'s TimeCloser™ physical synthesis tools now have more knowledge of the floorplan and early placement information. Thus, these tools make better place-and-route decisions that lead to better performance.

Also enhanced in ISE 4.1i, Synplicity customers can use the new Total Optimization Physical Synthesis (TOPS™) technology as part of the Amplify Physical Optimizer™ software to perfect their FPGA designs. Amplify physical optimizer software and the new incremental benefits from the TOPS technology are leading customers to better quality of results (QoR). [See "Understanding Physical Synthesis and Timing Closure" in this issue of *Xcell* for more information on ISE physical synthesis.]

HDL and Timing Interaction

Using traditional design techniques, much of a designer's time is spent trying to reach timing closure. It, therefore, stands to reason that improving timing-driven compilation – the timing results with more information and more interaction – will go a long way to help logic designers be more productive.

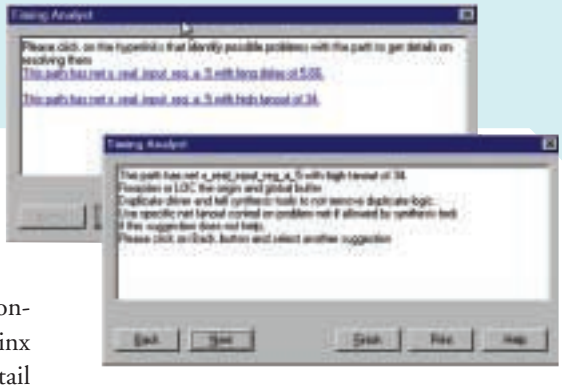

Figure 1 - ISE 4.1i Timing Wizard

Interactive Timing Wizard

ProActive Timing Closure includes a new interactive timing wizard, as shown in Figure 1. By selecting highlighted problem and warning areas in the timing report, the wizard suggests design changes and improvements that can help solve the timing problem and speed up the debug process.

HDL Analysis

Timing can be seriously affected by the "synthesizability" of the design code. In December last year, Xilinx announced the 1.0 coding style guide for Synopsys® Inc.'s LEDA™ HDL language checkers. In ISE 4.1i, customers can now use Synopsys' LEDA family of tools on their FPGA designs. The LEDA set of tools can verify your module against standard, good coding practices. This reduces the chance for problems cropping up during implementation due to bad coding (like introducing unnecessary latches into the finished module that cause timing analysis mistakes). The programmable LEDA tools are flexible to support corporate design techniques, to assure your source code meets your own specific standards.

As shown in Figure 2, Xilinx ProActive Timing Closure technology includes HDL analysis messages as part of the Xilinx Synthesis Technology (XST) report file. This new report feature suggests changes to the HDL code that would reduce design size and improve timing. This powerful capability is designed especially to help new HDL engineers and ASIC designers to write code that synthesizes well into an FPGA.

Timing Cross-Probing

Cross-probing for timing reports is yet another new enhancement delivered in the ProActive Timing Closure tools suite. You can select highlighted problem areas in the timing report and then see the problem net or area in either the Xilinx Floorplanner or the synthesis "technology viewer." Being able to find problem areas quickly and easily further reduces the time spent having to search through differing tools and GUIs for the same problem net, significantly speeding up design debug times.

Figure 2 - XST HDL analysis message

Conclusion

ProActive Timing Closure sets a new standard in the way programmable logic design tools can help you reach design closure faster and with better performance. Whether you're compiling six million gates or just a few thousand, you'll see the benefits in improved performance and reduced overall design times. ProActive Timing Closure will help you reach the fastest clock speeds available, and help you squeeze the most performance out of your devices.