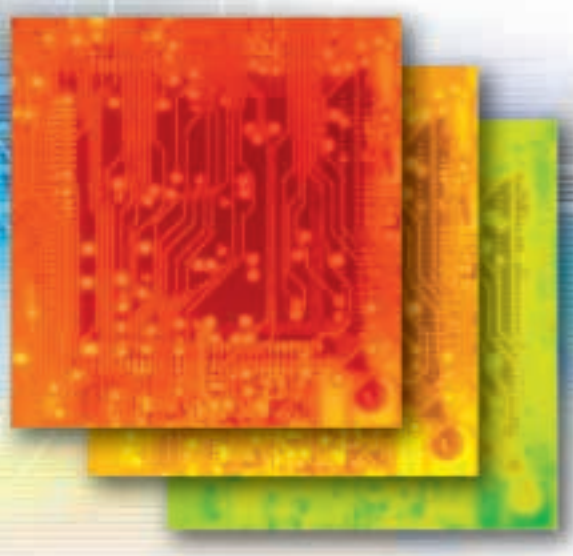
Understanding Physical Synthesis and Timing Closure



Using Xilinx Active Interconnect technology, you can achieve timing closure faster and with fewer iterations.

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In the domain of deep submicron (DSM) and nanometer ASIC technologies (180 nm and below), the predictable timing relationship between logical (synthesis) and physical (place-and-route) design often breaks down. Designs cannot meet their realistic timing objectives, creating the well-known "timing closure problem."

Timing closure is currently the biggest area of difficulty for ASIC performance-oriented designs. The underlying reason for this problem is that circuit delays in the DSM realm are dominated by net delays, which are influenced by the placement of the cells. The traditional fan-out-based wireload models for estimating interconnect delay during synthesis become inaccurate at DSM levels, thereby causing the lack of timing predictability between post synthesis and post layout results. Clearly, logical synthesis and physical placement technologies must merge to create properly placed and routed designs that meet realistic performance goals.

Physical Synthesis Defined

Physical synthesis refers to the ability to create a properly placed and routable circuit from the register transfer level (RTL) code – that is, to create a circuit that meets the realistic performance goals of the design in one pass. In cases where there are very aggressive performance goals or tight physical constraints, a second pass may be needed to achieve the desired performance goals. A properly placed design meets the design rules of the target silicon technology and is routable by a detailed router.

Physical Synthesis in an ASIC Environment

Physical synthesis tools, such as Physical Compiler™ from Synopsys® Inc. have replaced the typical synthesis tools (such as the Design Compiler from Synopsys) that many ASIC designers are using today for performance-critical designs.

Designers typically start with a design-planning tool such as the Synopsys Chip Architect™ design planner or other design planning tools such as LDP from Cadence and Planet from Avant! to decide on:

- Physical area allocated to each synthesizable module in the design
- Physical location of each synthesizable module
- Physical locations of RAM, ROM, hard IP, and other non-synthesizable blocks in the design
- Pad (I/O) locations.

Once the design is planned, the next step is to perform a top-level routing and timing analysis based on the chip-level timing constraints. Using the analysis results, designers adjust the physical port location on synthesizable modules and modify the location and orientation of non-synthesizable blocks to derive a realistic timing budget for each synthesizable module in the design.

At this point, all the necessary information is available for every synthesizable module in the design, so the designer can proceed with the physical synthesis step. For each synthesizable module, the Synopsys Physical Compiler takes in:

- RTL code
- Timing constraints derived from the design planning step
- Physical constraints (area and port locations, for instance) derived from the design planning step
- Synthesis and physical libraries.

The compiler produces a netlist and physical information (such as the proper placement of all the cells) that meet the timing goal of the particular module.

The next step is to perform the detailed routing on the circuit, based on the timing analysis, to ensure that the fully placed and routed module meets its performance goal. Cadence and Avant! Corp. are the only electronic design automation (EDA) vendors that offer proven detailed routers trusted by major ASIC vendors (such as NEC, LSI, and Texas Instruments).

Physical synthesis requires thousands of strategies to be evaluated by the software while the circuit is being properly timed, and placed and routed. Detailed routing takes a very long time, and it is not suitable during the synthesis process. Therefore, following placement, the Physical Compiler performs an estimated routing and RC parasitic extraction to assess the net delay and the impact on the module's timing objectives. If the timing goal is not met, the compiler must then decide on the next synthesis strategy.

The single most important factor is the correlation between routability analysis (obtained from the congestion map) of the physical synthesis tool and the results of the detailed router. Without correlation, the placement created by the Physical Synthesis tool may be unusable by the detailed router, thus nullifying the result of the Physical Synthesis tool. The next important factor is to properly calibrate the Physical Compiler's R&C extraction with the final parasitic extraction tool, for example, StarRC from Avant!®. Without this calibration, Physical Compiler's assessment of net delays may be inaccurate, hence compromising the synthesis results.

Merging Synthesis and Placement

Obtaining a timing correlation between logical synthesis and physical placement is not cheap – or easy.

Cost

The total cost of setting up a physical synthesis environment is about $350K. First, you must purchase a design planner or floorplanner (such as the Synopsys Chip Architect) for about $150,000. Then you must invest another $200,000 for a single license to use a Synopsys Physical Compiler.

Interoperability

The success of a physical synthesis tool is highly dependent on the routability of the placed circuits that it produces and the proper calibration of its RC extraction. If the physical synthesis vendor also provides a proven detailed router, then there is high degree of certainty that a placed circuit can be routed by the vendor's detailed router.

The Synopsys Physical Compiler is the most successful physical compiler so far and has a proven track record to work with Cadence® and Avant! detailed routers as well as Synopsys' own detailed router, the Route Compiler, to complete the physical implementation of the design.

Layout Expertise

Synthesis designers require extensive training to become comfortable with physical design concepts and components. This involves either training current staff or hiring an expert.

Solving the Timing Closure Problem with Xilinx FPGAs

Xilinx addresses the timing closure issue for Virtex™-II Platform FPGAs and Spartan™-II devices by using a three-step process of "Predict, Control, and Improve." This process allows you to implement designs that can meet their realistic timing objectives with a minimum number of iterations.

Predict

In FPGA architectures, Xilinx Active Interconnect technology predicts routing delays. This characteristic makes it possible to create interconnect models that are not based on fan-out. These models can be used during the synthesis process to estimate the interconnect timing with a high degree of predictability with respect to the placed and routed design. Xilinx has partnered with leading FPGA EDA vendors to offer synthesis tools that are aware of the Xilinx FPGA architectural details. For example, Synplicity® uses our Active Interconnect technology to produce netlists with timing within 20% of placed and routed designs. The next two steps close the remaining performance gap.

Control

Guiding the Xilinx timing-driven implementation tools with realistic timing constraints, high quality netlists, and accurate physical constraints are the keys to closing the performance gap that may exist between the synthesized netlist and the placed and routed design. Xilinx worked closely with Synplicity to develop the Amplify™ design planner and physical optimization tool for FPGAs.

Amplify software can improve the netlist quality through physical optimization techniques, such as moving registers across physical boundaries to increase performance. The Amplify program can also provide accurate area constraints and physical grouping of critical paths to the Xilinx implementation tools. Nonetheless, it is still possible to have failing paths remaining after place and route. The next step addresses the remaining failing paths.

Improve

Xilinx, in partnership with leading FPGA EDA vendors, has developed a tight interface between the vendors' synthesis tools and the Xilinx implementation tools. This interface allows re-optimization of failing paths and creates engineering change orders for new circuits into the Xilinx implementation tools. In a majority of cases, this capability can enable timing closure in no more than two passes.

Conclusion

Unpredictable interconnect timing during logical synthesis is the main reason for inaccurate timing estimation for DSM (0.18µ and below) ASICs. Xilinx has successfully applied a three-step process of "Predict, Control, and Improve" to close the timing gap for Virtex and Spartan-II architectures (0.22µ to 0.18µ). The key success factors are:

- Accurate timing estimation during synthesis
- True timing-driven place and route
- Re-optimization of failing paths.

As process technology continues to shrink, with ever more complex and higher performance designs, Xilinx Platform FPGA architectures will continue to enable designers to close the timing gap between logical synthesis and physical implementation.