Virtex-II Pro FPGAs:
The Platform for Programmable Systems Has Arrived

The Virtex-II Pro solution heralds a paradigm shift in system architecture by moving design based on zones of programmability to entire system-level programmability.

by Anil Telikepalli
Marketing Manager, Worldwide Marketing
Xilinx, Inc.
anil.telikepalli@xilinx.com

The curtains have been raised! The Virtex-II Pro™ Platform FPGA solution – the most sophisticated silicon and software product ever – is now available for programmable system design. Programmable systems represent flexible and scalable systems that are programmable at the architectural level. The goal in developing the Virtex-II Pro FPGA was to revolutionize system architecture by tightly integrating hardware and software functions on a single platform with unprecedented flexibility and scalability.

To achieve that objective, circuit engineers and system architects from IBM, Mindspeed, and Xilinx worked together to develop this advanced Platform FPGA. At the same time, engineering teams from top embedded systems companies, including Wind River Systems and Celoxica, worked alongside Xilinx software teams to develop the systems software and IP solutions that bring a new methodology to system design.

The result is the first Platform FPGA solution capable of implementing ultra-high bandwidth SOC (system-on-a-chip) designs that were previously the exclusive domain of custom ASICs. The Virtex-II Pro presents all the advantages of ASICs – and still retains all the flexibility and low development cost of programmable logic devices. The Virtex-II Pro solution enables high performance programmable systems specifically in the areas of wired and wireless networking, storage systems, professional broadcast, embedded systems, and digital signal processing systems. The new Virtex-II Pro FPGAs come in five densities, seven packages, and 15 combinations.

Virtex-II Pro FPGA Revealed

As a platform for programmable systems, the Virtex-II Pro FPGA is both flexible and scalable throughout all aspects of system architecture. By embedding processor cores within the FPGA fabric, the Virtex-II Pro architecture provides tight coupling between high-performance processors and the high-speed programmable logic. Together, the two components enable the most optimal yet flexible partitioning of hardware and software in a programmable system. The Virtex-II Pro FPGA is built upon the leading Virtex-II™ FPGA architecture with Rocket I/O™ multi-gigabit transceivers and embedded IBM PowerPC™ processors completely immersed into the FPGA fabric (Figure 1).
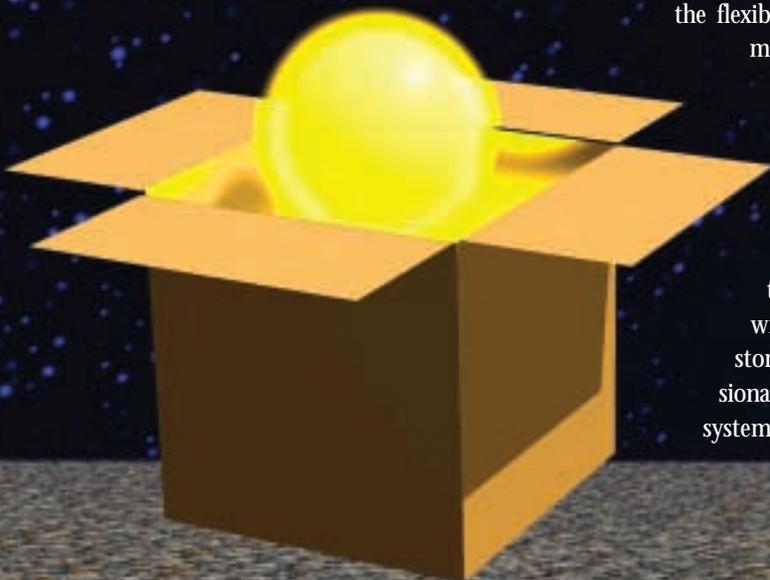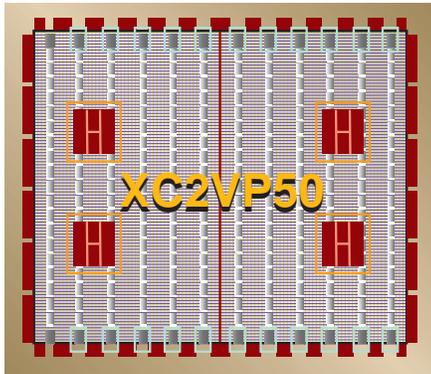
Figure 1 - The Virtex-II Pro XC2VP50 device features four IBM PowerPC 405 processors and 16 Rocket I/O multi-gigabit transceivers embedded in the FPGA fabric.

Additionally, Virtex-II Pro Platform FPGAs offer the following features:

• Five family members with 3,168 to 50,832 logic cells, and 216 Kb to 3,888 Kb of block RAM

• 0.13µ , 9-layer copper, low-k technology process

• 3.125 Gbps Rocket I/O multi-gigabit serial transceivers based on Mindspeed SkyRail™ technology, up to 16 per device

• 300+ MHz PowerPC embedded processor cores based on IBM's PowerPC 405 processor, up to four per device

• Virtex-II IP-Immersion technology powered by system-level features:

  - Flexible SelectI/O™-Ultra technology supporting 840 Mbps LVDS I/Os

  - Xilinx Controlled Impedance Technology (XCITE) capability, providing built-in digital impedance matching on all single-ended I/Os

  - Embedded 18 Kb dual-port block RAM resources

  - Embedded 18-bit x 18-bit multiplier blocks

  - DCM (digital clock manager) macros support de-skew and frequency/phase manipulation

  - Bitstream encryption (Triple-DES) for design protection.

Rocket I/O Transceivers

Rocket I/O multi-gigabit transceivers (MGTs) are based on Mindspeed SkyRail™ CMOS technology. Each full-duplex transceiver runs from 622 Mbps to 3.125 Gbps baud rate and includes the entire transceiver support circuitry (Figure 2). The Rocket I/O blocks are the first transceivers embedded in FPGAs to reach a baud rate of 3.125 Gbps. Up to 16 MGTs can be bonded together to provide an aggregate data rate of 40 Gbps for each of transmitter and receiver.

Well-designed serial transceivers have two fundamental requirements that distinguish them from others:

• Ability to operate at multi-gigabit rates to support emerging standards

• Ability to bundle multiple channels together for scalable data rate.

Each Rocket I/O transceiver consists of both a digital Physical Coding Sublayer as well as an analog Physical Media Attachment to provide a fully integrated serializer/deserializer function that enables the entire functionality and performance of emerging serial standards (Table 1).

Historically, serial transceivers have been analog components built using SiGe or GaAs processes. These transceivers generate enormous quantities of heat – and any integration of channels to increase the data rate was out of the question. However, Xilinx Rocket I/O transceivers not only provide multi-gigabit data rates, they can also be tied together to increase the aggregate bandwidth by using the built-in channel-bonding capability. This scalability is especially important as data rates increase and the industry moves

toward designing compact optical networking equipment (impossible if you must put in several heat sinks).

For example, four Rocket I/O blocks allow 16 printed circuit board (PCB) traces to support full-duplex 10 Gbps data rates. This is equivalent to 256 traces of typical busses or 68 traces of a high-speed parallel bus. Thus, the four Rocket I/O blocks allow a 16X reduction of PCB
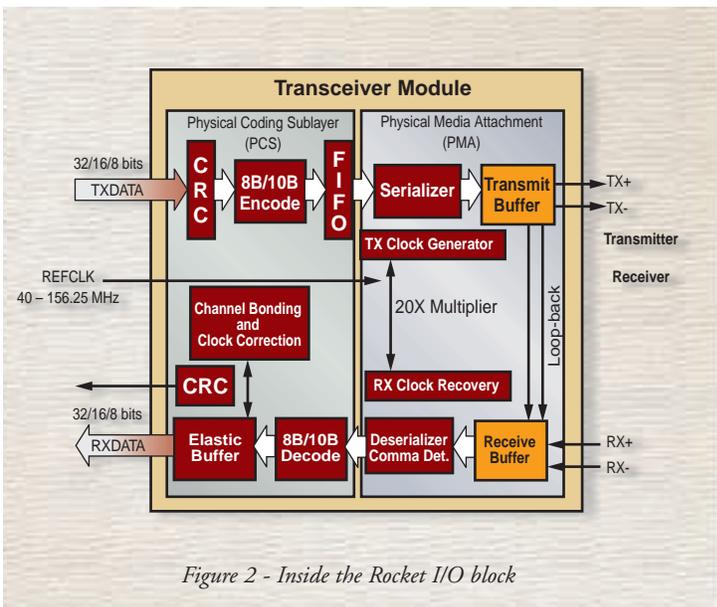

Figure 2 - Inside the Rocket I/O block

traces over conventional parallel busses, resulting in significant reduction of PCB complexity and EMI system noise. In short, Rocket I/O technology allows higher bandwidth systems than currently possible, with cost savings from faster time-to-market, reduced power consump-

Technology	Line Speed
3GIO	2.5 Gbps
Serial ATA	1.5 Gbps
InfiniBand	2.5 Gbps
Gb Ethernet	1.25 Gbps
10 GE (XAUI)	3.125 Gbps
Serial RapidIO	1.25 Gbps
FibreChannel	1.06 Gbps

Table 1 - Virtex-II Pro Platform FPGAs support these protocols and baud rates.

tion, smaller PCB size, and lower component count (Figure 3).

Ultimate Connectivity

Virtex-II Pro Platform FPGAs, equipped with Rocket I/O MGTs, support emerging serial connectivity standards – and with Xilinx SelectI/O™-Ultra technology, these next-generation Platform FPGAs also support today's parallel connectivity standards (Table 2). Thus, the Virtex-II Pro FPGA serves as an ultimate connectivity platform to bridge across various interface standards in chip-to-chip, board-to-board, or even WAN/MAN/LAN networks.

In addition to these hardware physical interface capabilities, the Virtex-II Pro solution provides PowerPC processors and soft intellectual property (IP) cores to make designing with any protocol easy.

IBM PowerPC Processors

Each IBM PowerPC processor runs at 300+ MHz and 420 Dhrystone MIPS. Even though the PowerPC 405 core occupies a small portion of the die area, it provides tremendous system flexibility. Instead of attaching the PowerPC 405 processor next to the FPGA with a bus interface (as certain vendors have attempted), the Virtex-II Pro engineering team embedded the processor entirely within the FPGA fabric. Using Xilinx IP Immersion and Active Interconnect technologies, hundreds of processor nodes are directly connected to the FPGA logic and memory array.

Such total immersion gives you the utmost flexibility in hardware/software system architecture. You can efficiently divide complex functions between high-speed implementation in hardware and high-flexibility implementation in software. This direct-connect configuration bypasses the bottleneck of using a bus to interface between the FPGA and an attached/external processor.
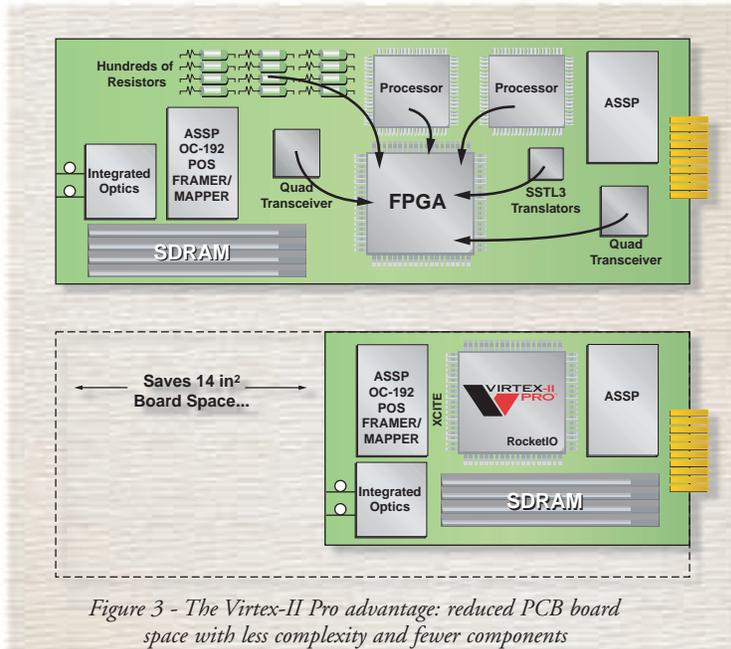

Figure 3 - The Virtex-II Pro advantage: reduced PCB board space with less complexity and fewer components

The PowerPC 405 core has unique on-chip memory (OCM) controllers that bypass the processor bus for fast, direct access to a fixed amount of instruction and data memory implemented in Xilinx SelectRAM™ modules (Figure 4). This is especially useful for data streaming applications.

The PowerPC processor is supported by IBM CoreConnect™ technology – a high-bandwidth 64-bit bus architecture that runs at 100 to 133 MHz. For maximum flexibility, the CoreConnect architecture is implemented as a soft IP within the Virtex-II Pro FPGA fabric (Figure 5). You can add CoreConnect peripherals from an extensive IP library from Xilinx and third-party part-

ners or develop proprietary peripherals of your own.

The CoreConnect bus architecture has two main buses, called the Processor Local Bus (PLB) and the On-chip Peripheral Bus (OPB). These buses can be used for interfacing high-speed and low-speed peripherals with the PowerPC processor respectively. Additionally, a third Device Control Register (DCR) bus is used for transfers to and from general purpose peripheral device registers.

The Virtex-II Pro Platform FPGA is also supported by a complete set of embedded software tools for development and debug. Through an OEM agreement, Xilinx is able to provide software tools from Wind River Systems that are customized for Virtex-II Pro FPGAs. These include:

• Diab™ XE (Xilinx Edition) compiler

• SingleStep™ XE software debugger

• visionPROBE II XE JTAG run control hardware connection probe.

In addition, a suite of GNU (open-code Linux) tools is also available.

With the Virtex-II Pro solution, you can use the FPGA fabric for highly parallel processing and fixed algorithms. You can use the PowerPC processor for sequential com-

LAN/MAN/WAN	Board-to-Board		Chip-to-Chip	
● 10/100 Ethernet	● PCI 32/33	● RapidIO	● PCI 32/33	● POS-PHY L3/L4
● 1Gb Ethernet	● PCI 64/66	● CSIX	● PCI 64/66	● Flexbus 4
● 10Gb Ethernet	● PCI-X 100	● HyperTransport	● PCI-X66 & 100	● CSIX
● 1Gb Ethernet PHY	● Serial RapidIO	● InfiniBand	● RapidIO	● HyperTransport
● 10GE XAUI	● Fibre Channel	● 3GIO	● 10GE XAUI	● 3GIO
● SONET Standards*	● 10GE XAUI			

Table 2 - Virtex-II and Virtex-II Pro FPGAs offer multiprotocol connectivity.

● Serial standards enabled by Rocket I/O technology – Virtex-II Pro FPGAs

● Parallel standards enabled by SelectI/O-Ultra technology – Virtex-II & Virtex-II Pro FPGAs
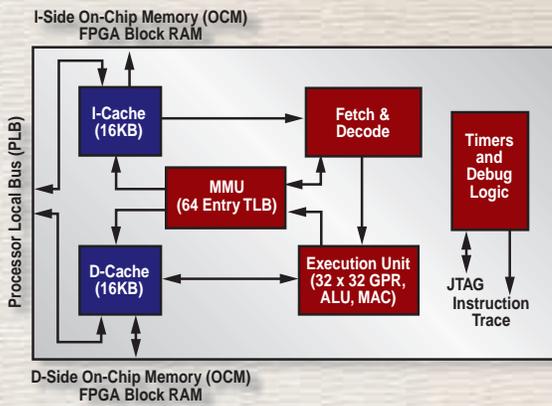
* SONET compatible, supports data rate only

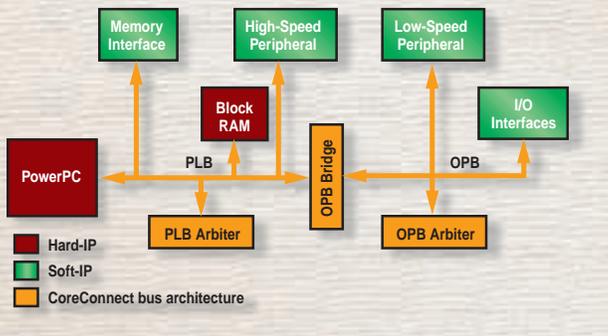*Figure 4 - Inside the PowerPC 405 processor*

Figure 5 - Hard and soft IP cores

puting, exception handling, and control functions. The Rocket I/O serial transceivers and SelectI/O-Ultra parallel technologies enable optimal data access into and out of the Virtex-II Pro FPGA.

On-Demand Architectural Synthesis

Architectural synthesis is a combination of tools and technologies that allows designers to specify high-level requirements for designing their systems. In other words, architectural synthesis is a tool-based partitioning of hardware and software.

In order for architectural synthesis to work, both the hardware and software components of the system must be tightly integrated. Virtex-II Pro Platform FPGAs enable on-demand architectural synthesis with tremendously flexible, scalable, and high-bandwidth features. You can perform architectural synthesis anytime in the product cycle – during system design and debug phases, or even after the product has shipped. With abundant resources of hardware and software, Virtex-II Pro FPGAs give you the flexibility and scalability for fine-tuned system archi-

tecture, partitioned optimally between hardware and software.

Price & Performance Leader

Leading-edge systems need high bandwidth serial I/O, which has only been achievable by interfacing an FPGA to an external serial transceiver by means of hundreds of pins. Similarly, high-performance systems typically require one or more processors on the board, creating even more connectivity problems and PCB complexity.

By immersing multi-gigabit transceiver blocks and processor cores within the FPGA fabric (Figure 6), the Virtex-II Pro Platform FPGA delivers the best price and performance. Integrating processors and transceivers within the FPGA fabric lowers costs and raises performance by:

- Saving PCB space
- Simplifying PCB complexity
- Requiring fewer components
- Eliminating complex device interconnectivity issues
- Reducing overall system power consumption
- Using XCITE digitally controlled impedance technology to do away with external termination resistors
- Enabling optimal system partitioning between hardware and software.

A New Development Paradigm

By tightly integrating flexible and scalable high-performance programmable logic with the PowerPC processor, the Virtex-II Pro Platform FPGA fundamentally changes the way systems are designed. The Virtex-II Pro solution facilitates a new paradigm in system development with signifi-
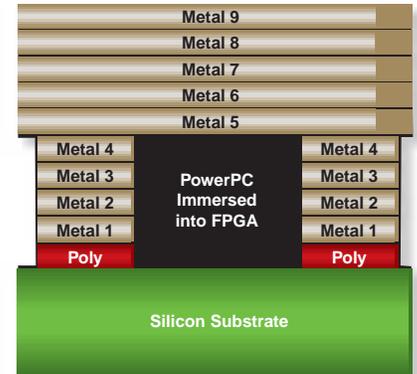

Figure 6 - Hard IP cores are deeply embedded and actively connected within the FPGA fabric

cant benefits, specifically in software engineering productivity:

- Embedded processors can be used for rapid system pre-production to facilitate accelerated software development. A preliminary hardware platform can be built quickly by emulating a C-based algorithm using the embedded processors. This creation of a preliminary hardware platform allows software development to start much earlier in the design process, compared to current practice.

- Software debugging can be performed at hardware speeds while the hardware implementation continues to be speed-optimized. Xilinx ChipScope™ Pro on-chip verification tools provide in-system observability into both the FPGA hardware and the processor bus transactions.

Conclusion

The Virtex-II Pro Platform FPGA solution encompasses the following:

- Rocket I/O transceivers and IBM PowerPC processors immersed and embedded into the high performance Virtex-II Pro FPGA fabric

- Intellectual property solutions, including soft peripherals and connectivity cores

- Complete design resources, including development tools and kits

To find out more about this revolutionary next-generation Platform FPGA for programmable systems, go to *www.xilinx.com/ virtex2pro.*