Use Rocket I/O Multi-Gigabit Transceivers to Double Your FPGA Bandwidth

Virtex-II Pro Platform FPGAs break open the I/O bottleneck.

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As FPGAs increase in size and performance, I/O resources become the main bottleneck to FPGA performance. Although the effective area of a chip grows as the square of the feature size, the perimeter I/Os grow only linearly. State of the art designs require higher performance I/O modules.

In response to this increasing demand on I/O resources, Xilinx has developed novel I/O structures called Rocket I/O™ multi-gigabit transceivers (MGTs) that enable order-of-magnitude increases in I/O performance. The Rocket I/O MGTs double the total I/O bandwidth of the Virtex-II Pro™ family of devices using only a few percent of the pins.

With up to 16 MGTs per device, the Virtex-II Pro achieves an additional 100 gigabits per second of I/O bandwidth in the larger devices over what is available with the general-purpose I/O blocks. Rocket I/O MGTs enable multiple gigabit I/O standards and maximize performance for FPGA-to-FPGA communications. Even though Rocket I/O MGTs dramatically increase performance for demanding applications, they are easy enough to use for simple FPGA-to-FPGA communications with special soft macros such as the Aurora core available from Xilinx. The interface has been simplified to the extent that no external resistive termination is required with the Rocket I/O MGTs. The transceivers can be internally configured to match 50Ω or 75Ω transmission lines.

MGTs Onboard

The Rocket I/O MGTs are shown in Figure 1, which illustrates the overall Virtex-II Pro architecture. The MGTs are located above and below columns of Block RAM, providing close availability of Block RAMs for ingress and egress FIFOs. As many as 16 MGTs are integrated on each FPGA above and below the Block RAM columns. The clock distribution networks can feed these transceivers for low-skew clock alignment between MGTs.

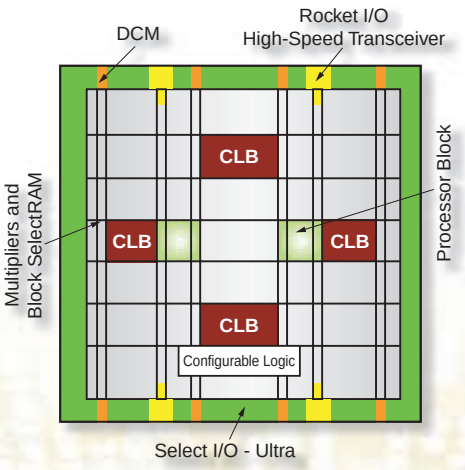


Figure 1 - Virtex-II Pro FPGA architecture, including up to 16 Rocket I/O MGTs

MGTs = Multiple Gigabit Standards

The Rocket I/O MGTs have been designed to be compliant with:

- Gigabit Ethernet
- 10 Gigabit Ethernet XAUI
- Fibre Channel
- InfiniBand™ Architecture
- Xilinx Aurora core

Configurable hardware support is provided for:

- 8B/10B encoding
- Disparity control
- Transmitter and receiver termination impedance
- Pre-emphasis
- Amplitude control
- Loopback testing.

These are the essential configurable hardware features that enable compliance with all of the main multi-gigabit signaling standards. You can find more information on Virtex-II Pro standards support on the Xilinx website at www.xilinx.com/partinfo/databook.htm.

MGTs Speed up FPGA Communications

Although MGTs have many important applications interfacing to industry standard gigabit communications protocols, they can serve another important function in boosting the bandwidth available among FPGAs.

Figure 2 shows a data communications application requiring two FPGAs. For a typical implementation, half of the I/O bandwidth is allocated to external links and half to the inter-FPGA link. With 800 general-purpose I/O pins available, running at a typical speed of 250 MHz, the pair of FPGAs can support a pipeline throughput of 100 gigabits per second.

If the 16 bidirectional MGT links are added, 16 links x 3.125 gigabits are available in each direction, for another 100 gigabits per second total. Figure 3 shows the sys-

Figure 2 - FPGA processing pipeline using general purpose I/O (GPIO) only

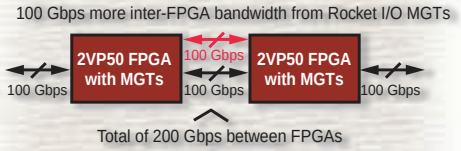


Figure 3 - FPGA processing pipeline using Rocket I/O multi-gigabit transceivers and general purpose I/O (GPIO)

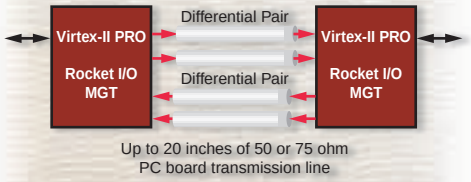


Figure 4 - Rocket I/O MGTs configured to pre-emphasize data transmission over PCB traces up to 20 inches long

tem diagram for two Virtex II Pro devices including the Rocket I/O MGTs between the devices. With Rocket I/O, the total bandwidth available between the two FPGAs increases to 200 gigabits per second. This extra bandwidth is extremely useful in switching applications that may require up to 100% internal overhead to handle control protocols over and above the datapath requirements. This 2X increase is an example of the dramatic I/O performance increase available in Virtex-II Pro Platform FPGAs.

Aurora Boosts FPGA-to-FPGA Links

Xilinx has developed a software macro called the Aurora core that provides easy 16-bit and 32-bit interfaces from FPGA-to-FPGA using one or more Rocket I/O MGTs. The Aurora core handles the framing, synchronization, and channel bonding tasks, allowing you to focus more on their application. A single MGT can provide a 16-bit or 32-bit FPGA-to-FPGA interface. The software Aurora core coupled with hard core (implemented in silicon) MGTs can create powerful serial-to-parallel and parallel-to-serial tranceivers.

Alternatively, multiple MGTs can be bonded together to form a higher-bandwidth interface. The Aurora macro ensures that channel-bonded data will appear on the same clock cycle at the other end of the communications link. The 8B/10B encoding method is used for the Aurora soft macro, giving an effective bandwidth of 10 gigabits per second for a set of four channel-bonded MGTs between two FPGAs.

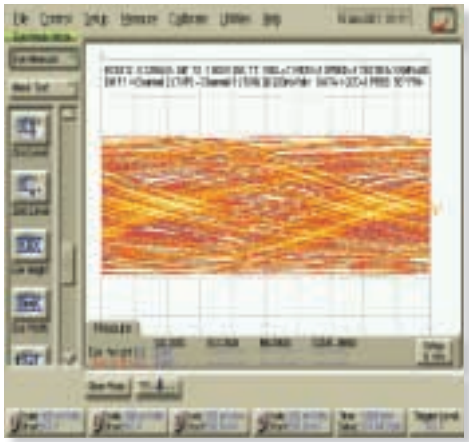
Pre-Emphasis Goes the Distance

Another important feature of the Rocket I/O solution is pre-emphasis, which compensates for the filtering effects of FR-4 PC board material at gigabit speeds. Pre-emphasis boosts the output levels to compensate for the filtering effects of extended PCB traces. With pre-emphasis, PCB runs of 20 inches or longer can be supported reliably at speeds of 3.125 gigabits per second.

Figure 4 shows how two MGTs on separate FPGAs can be easily linked up to 20 inches apart using standard PC board transmission-line traces. Pre-emphasis improves the noise and jitter performance at these high speeds for longer PC traces where dispersion affects timing and voltage margins.

You can clearly see in Figure 5, which shows oscilloscope traces at the receiver without pre-emphasis and with 30% pre-emphasis. The pre-emphasis enables reliable signal transmission at 3.125 Gigabits per second over long PC board traces in standard FR-4 PC board material. Transmitter and receiver termination is provided internally to each MGT, eliminating the need for external termination of these transmission lines. The termination impedance can be set to 50 ohms or to 75 ohms.

No Pre-Emphasis



30% Pre-Emphasis

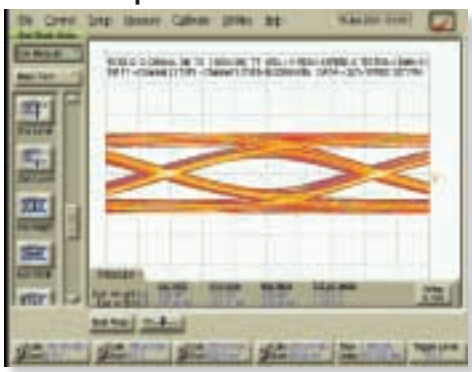


Figure 5 -Received signals after 50 inches FR-4 PC board material with no pre-emphasis and with 30% pre-emphasis in the Rocket I/O MGT.

Conclusion

The Rocket I/O MGTs enable high-speed interfaces for Virtex-II Pro Platform FPGAs. Standards such as InfiniBand Architecture, Fibre Channel, XAUI, and Gigabit Ethernet are directly supported. Inter-FPGA communications are greatly enhanced by Rocket I/O modules and the Aurora soft macro, which enable simple FPGA links with channel-bonded performance of over 10 gigabits per second. Using pre-emphasis, PCB trace runs of 20 inches or greater are possible at speeds of up to 3.125 gigabits per second per link. In the larger Virtex-II Pro devices, this represents a factor of two increase in total I/O performance available per FPGA. Clearly, Virtex-II Pro Platform FPGAs with Rocket I/O MGTs give you a competitive advantage, both in terms of performance and time to market.