The Terabit Networking Forum

Xilinx helps you meet the challenges of building next generation communication systems.

by Abhijit Athavale
System Interface Solutions Marketing Manager
abhijit.athavale@xilinx.com

In response to the networking industry's need for the latest news and technical information, Xilinx and Cahners Electronics Group, in association with other networking industry leaders, recently hosted the Terabit Networking Forum – a premier gathering of visionaries and experts who addressed the challenges and opportunities associated with today's evolving interconnect technologies. Over 2500 engineers and system architects attended, as industry experts provided insight into the future of interface standards such as InfiniBand™, RapidIO™, HyperTransport™, 3GIO, PCI-X, CSIX, 10 Gb Ethernet, and Packet-over-SONET technologies.

Here's an overview of what was discussed.

Defining the Challenge

Consumers' increasing appetite for continuous Internet access and multimedia-rich Web applications are creating a huge

*HyperTransport or RapidIO – who will win this battle of emerging system interfaces?*

Gabriele Sartori of AMD explains the HyperTransport technology.

Sam Fuller of Motorola gives his views on system interconnect technologies and RapidIO in particular.

demand for fast and efficient processing of data across wireless or wired media. In a typical terabit system, the bottleneck is at the system interconnect level – the speed at which various components inside the box communicate with each other, as well as with the outside world. Clearly, faster CPUs and optimized network packet processors, along with an efficient, fast

Jim Pappas
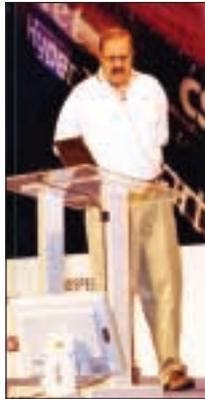
Jim Pappas of Intel explains the role of InfiniBand in Terabit Networks

data transfer mechanism, are required to solve this problem. System architects are also looking for the ability to support multiple standards, to "future proof" their products against constantly evolving interconnect standards, and to integrate many of the functions performed by various chips on a board.

With this rapidly increasing emphasis on connectivity, integration, flexibility, and re-

Solving the Connectivity Problem

The PCI local bus has been the ubiquitous system interconnect standard for the past few years. From PCs to networking to communication systems, PCI has supported systems requirements quite satisfactorily and will still be used quite heavily in applications that do not require large quantities of data to be transferred quickly. However, PCI technology – with its centralized arbitration model, limited reliability, and limited scalability – cannot effectively meet the requirements of terabit applications.

Tracy Vanik

Tracy Vanik of RHK explains why 10 Gb Ethernet is the hottest thing in town.

programmability, Xilinx FPGAs are now a mainstream solution and the central component in many new communication systems. Our Virtex-II series platform FPGAs include 3.125 Gbps serial I/O capability and a portfolio of high-performance IP cores that help you quickly implement complex functions such as PCI-X, RapidIO, 10 Gb Ethernet, CSIX, and POS PHY4, HyperTransport, and many more. In short, Virtex FPGAs are ideal for interconnecting communications systems.

Attendees viewing the technology demonstrations offered by participating companies.

Crowd enjoying the afternoon break.

Lauri Vickers, the panel moderator, listens as Elie Massabki from Mindspeed explains how multi-gigabit serial I/O will be used to build terabit systems.

Lauri Vickers

As Moore's law states, processor speed doubles every 18 months, but the PC bus performance doubles every three years. Clearly, this presents a large gap in performance that can not be overcome just by continually increasing the CPU speeds. Various system interconnect standards, notably InfiniBand, RapidIO, and HyperTransport (in addition to enhancements to the trusted PCI bus) have been proposed in the last couple of years to solve this communication bottleneck. New ones such as the recently announced third-generation I/O standard are still being proposed. It is very early to say which standard will win this battle of system standards and emerge as the new PCI.

Taking the Next Step

All the standards mentioned above and more were discussed at the Terabit Networking Forum. Various presentations and product demonstrations made on-site were recorded and are now available via Video-on-Demand at: *www.xilinx.com/terabit.*

If you are trying to create high-bandwidth systems using next generation interfaces, you should view the video on demand featuring technology overviews and detailed interface discussions by 12 industry experts, including:

• Siva Ananmalay, VP at Nortel, discussing industry requirements for High-bandwidth Network Systems

• Jim Pappas, Director at Intel, on InfiniBand architecture, discussing the serialization of server I/O.

• Gabriele Sartori, Director at AMD, discussing the role of HyperTransport in next-generation high-speed I/O.

• Sam Fuller, Director at Motorola, discussing RapidIO Interconnect Architecture.

You'll find that Xilinx programmable logic technology can satisfy the requirements of today's systems by reducing risk, improving system integration, and improving time-to-market.

Year 2001-2002 Worldwide Xilinx Events Schedule

Year 2001 - 2002 North American Event Schedule

Nov 13-15	EDA: Front-to-Back	San Jose, CA
Dec 10-11	Wind River's Worldwide Developers Conference and Exhibition	Santa Clara, CA
Jan 16-17	Portable Design	Santa Clara, CA
Feb 26-28	Wireless/Portable Symposium	San Jose, CA
March 13-15	Embedded Systems Conference	San Francisco, CA
May 14-16	ICASSP	Orlando, FL
June 10-12	Design Automation Conference	New Orleans, LA
July 15-17	NSREC	Phoenix, AZ
Sept 17-18	Applied Computing Conference	Santa Clara, CA

Year 2001 - 2002 Japanese Event Schedule

Nov 2001	MST Fair 2001	Tokyo, Japan
Jan 24-25	Electronic Design and Solution Fair	Yokohama, Japan

For more information about Xilinx Worldwide Events, please contact one of the following Xilinx team members, or see our Web site at: www.xilinx.com/company/events.htm

• **North American Shows:** Jennifer Waibel at: *jennifer.waibel@xilinx.com*

• **European Shows:** Andrea Fionda at: *andrea.fionda@xilinx.com* or Andrew Stock at: *andrew.stock@xilinx.com*

• **Japanese Shows:** Yumi Homura at: *yumi.homura@xilinx.com*

• **Asia Pacific Shows:** Mary Leung at: *mary.leung@xilinx.com*