Synplicity Announces TOPS

A Second-Generation Physical Synthesis Technology for Xilinx FPGAs

Routing interconnect delays significantly affect your overall circuit performance, and therefore, your synthesis tools must account for these delays. TOPS (Total Optimization Physical Synthesis) makes physical synthesis even more efficient.

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As FPGA process technology gets faster and denser it poses new design challenges for your development tools – challenges that must be addressed to maintain the productivity you expect from programmable logic. Your synthesis tools, which were originally designed to optimize logic, must now also consider the effects of your interconnect delays, during the synthesis process.

Synplicity was the first company to address this problem with its Amplify™ Physical Optimizer™ software, which allows you to improve performance by using physical guidance in addition to normal timing constraints during the synthesis process. By assigning critical logic to physical regions of the device, you provide the Amplify tool with important information that it uses to not only create better logic placement, but also to aggressively optimize (change) the resulting netlist for better performance.

While this interactive method continues to be preferred for getting the very best results, Synplicity's new second-generation physical synthesis technology has demonstrated up to 15% performance improvement for Virtex™ devices in a totally automated flow. This new physical synthesis technology, TOPS, supports both a fully automated and an interactive physical synthesis methodology.

Total Optimization Physical Synthesis (TOPS)

After normal synthesis, place-and-route, and timing analysis, critical path information is used to interactively create physical regions on the device. The TOPS technology uses these physical regions to perform physical synthesis on each region. The improved netlist and detailed regional placement information is passed to the final place-and-route process.

Like Synplicity's first-generation physical synthesis technology, the TOPS technology performs simultaneous placement and optimization. It includes two methods, designed to meet your needs – Automated TOPS and Interactive TOPS.

- The Automated TOPS technology fully automates physical synthesis to help you achieve higher device performance with the push of a button. Using this methodology, you need not be familiar with the physical architecture of a specific device to improve performance.

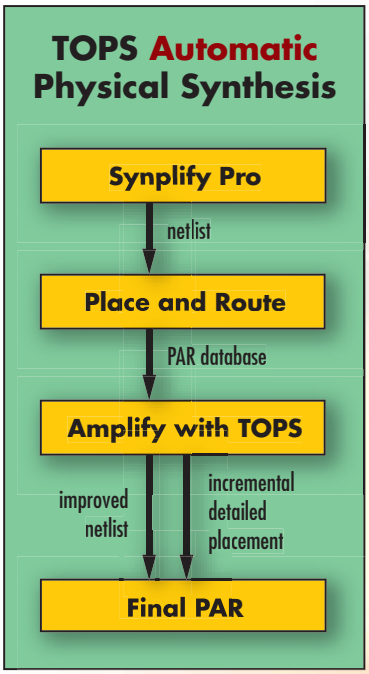

Figure 1 - Automatic physical synthesis using TOPS

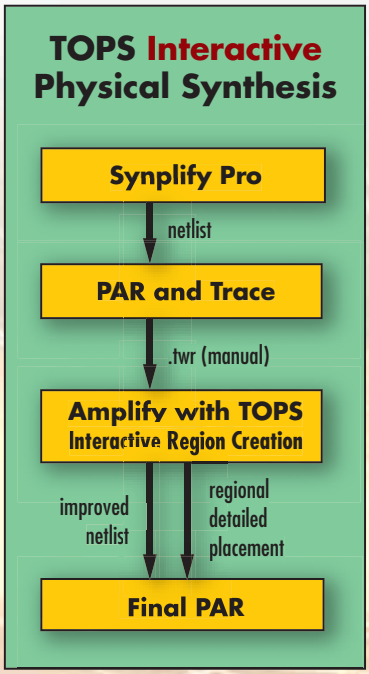

Figure 2 - Interactive physical synthesis methodology with TOPS

- The Interactive TOPS technology takes Synplicity's interactive physical synthesis approach to the next level by operating with exact placement information while re-optimizing and incrementally placing the design thereby significantly improving performance.

The automated and interactive TOPS phases may be used together to achieve maximum performance.

Automatic TOPS

After normal synthesis and place-and-route, detailed physical information from the Xilinx design database is used as input for the automated pass through the TOPS software. Amplify along with TOPS technology improves the netlist itself for performance and also generates incremental detailed placement which are passed on to the Xilinx place-and-rout software for final routing, as shown in Figure 1.

Interactive TOPS

The Interactive TOPS technology is designed to improve performance by focusing its physical synthesis algorithms on critical portions of the design as opposed to the entire chip – you create regions only for those timing-critical portions of your design as opposed to constraining the entire chip. If you are already familiar with the Amplify Physical Optimizer product's region-based interactive methodology, you know its impressive performance improvements. The new Interactive TOPS technology boosts those improvements by performing detailed incremental placement for critical regions. The interactive TOPS software then performs physical synthesis (including detailed placement) on those regions. The improved netlist and placement information for each region is then passed on to the Xilinx place-and-route software for the remainder of the placement and routing, as shown in Figure 2.

If required to meet timing performance, the Amplify software will automatically move (place) logic that you did not directly place (and report in a log file). All logic that you place in a region will remain in that region as long as it helps improve timing performance.

Conclusion

Physical synthesis is the answer to getting aggressive performance from your FPGAs – in recent designs, as much as 80% of the total timing delay is the result of routing, not logic. And, as devices get larger, interconnect delays have an increasing role in determining your chip's overall performance.

With Synplicity's second-generation physical synthesis technology (TOPS), the requirement for interactively creating physical regions is eliminated, and up to 15% performance improvements are possible with the push of a button. For even higher performance, interactive TOPS methodology uses incremental detailed placement to deliver up to 50% more speed than normal synthesis alone. For additional information visit: *www.synplicity.com.*

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The Amplify Physical Optimizer

The Amplify Physical Optimizer was introduced in March of 2000 and has helped more than one hundred companies quickly achieve aggressive timing performance in their programmable devices. Xilinx designers have seen performance improvements of as much as 45%, as a result of using the Amplify software. The average performance improvement (compared to logic synthesis alone), across the many designs tracked, is over 20%.

Until now, designers using the Amplify product have used an interactive methodology, where physical regions are created on a device, then logic from critical circuit paths is placed into the regions and then finally synthesized using Amplify's unique physical synthesis technology. Even though the Amplify software is very easy to use, it does require knowledge of the device architecture – it is important to know where to create the regions and how to assign logic to them, to get the best results.