Xilinx Takes Power Analysis to New Levels with XPower

Analyze your power consumption earlier in the design cycle to better make trade-offs that will allow you to meet specifications and get your product to market faster.

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In recent years, programmable design and device sizes have grown to astonishing levels of complexity. Average design sizes were approximately twelve thousand gates a few years ago. Now, they have bloomed into hundreds of thousands and even multimillion gate arrays. And, as design sizes increase, so does power consumption.

Meanwhile, the demand has risen for battery-powered handheld devices that are increasingly smaller and sensitive to power usage. It's clear that power consumption can no longer be ignored in programmable logic design.

Anticipating designers' needs, Xilinx has added the XPower analysis tool to its suite of ISE 4.1i design tools. XPower graphical power-analysis software is the first of its kind for programmable logic design. Now, earlier than ever in the design flow, you can analyze total device power, power per net, and routed or partially routed designs. The XPower tool can be controlled from the graphical interface or through a command line-driven batch mode. XPower delivers data in either an easy-to-use graphical interface (Figure 1) or in ASCII reports. XPower offers unmatched device support and accuracy for achieving the lowest possible power consumption.

Inside the XPower Analysis Tool

XPower works on the principle of "activity rates." Activity rates are defined as the rate at which a net or logic element capacitance switches. For dynamic power calculation and display, activity rates are expressed as a frequency. An activity rate may be relative to a clock, in that the net or logic element switches at some percentage of the clock frequency. This is often referred to as a toggle rate. Activity rates are very useful because they enable you to recalculate the power by merely changing the system clock frequency. This allows you to use your original simulation data and save time. XPower supports any number of input clocks as well as DLL/DCM derived clocks. Expressed as a percentage, an activity rate of 100% means that a signal state change happens on average once every clock cycle with the resultant frequency being half the associated clock. For nets and logic that are not synchronized with a clock, the activity rate is just the switching rate.

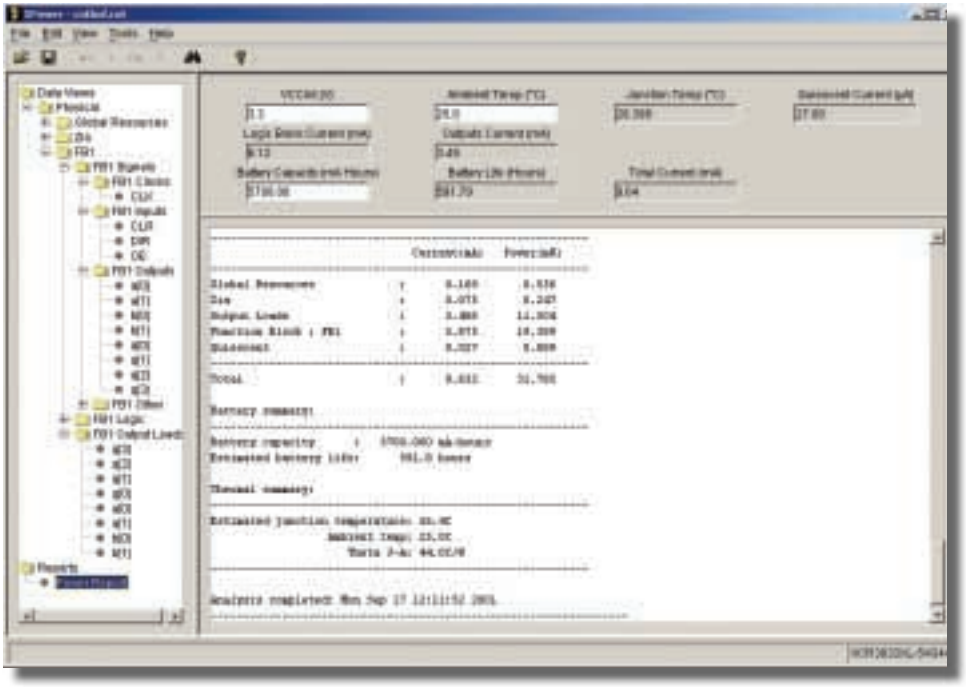

Figure 1 - XPower graphical user interface

XPower Analysis in FPGA Design

Power consumption in high-density design is becoming a serious issue as device sizes shrink and design sizes grow. For FPGA design, the XPower tool gathers design information from the following list of files:

- NCD – design topology and physical resource usage
- PCF – clock frequency and voltage
- VCD – detailed design activity rates for all nets
- XML – user setting file.

XPower accepts your post-route netlist (NCD) and physical constraints file (PCF) to determine the interconnect, I/O, and clock information of your design. With this information, XPower builds a hierarchical representation of your design – broken out by signals, clocks, logic, and outputs. In addition, XPower accepts value change dump (VCD) information from all ModelSim™ simulators. VCD information provides the XPower program with detailed design activity information that gives you a very accurate power estimate. The extensible markup language (XML) file saves the user settings data for subsequent tool usage.

The XPower program will estimate your power consumption for Virtex™, Virtex-E, Virtex-II, Spartan™, and the new Spartan-IIE FPGAs.

XPower Analysis in CPLD Design

Low-power design requires careful analysis of an application's power usage. To meet customer demands, battery-powered applications must have power budgets that can't be exceeded – deficits are unacceptable.

One of the pitfalls of power estimation lies in the maximum and minimum power corner cases. For instance, going with a maximum power estimation may require an oversized battery, creating a cost and packaging dilemma. Whereas, if you go with a minimum power estimation, an undersized battery could lead to short battery life and potential product return due to customer perceptions of poor quality. Therefore, using typical power estimation, combined with battery life tests, provides a good conservative approach.

XPower supports CoolRunner™ Fast Zero Power™ technology. Using FZP technology gives you an accurate, easy-to-use power estimation of your design. To enhance the ease of use, the application of activity rates to internal nodes is automated to minimize the data entry task. Refer to *xapp360.pdf* on the Xilinx website for additional guidance.

For CPLD design, the XPower program gathers design information from the following list of files:

- CXT – CPLD XML file that contains design topology and physical resource usage
- PCF – clock frequency and voltage
- VCD – detailed design activity rates for all nets
- XML – user setting file.

After completing and fitting your design in a CoolRunner CPLD, simulate your design using the ModelSim simulator in ISE 4.1i. To obtain the most accurate power estimation, your simulation should be as close as possible to the actual in-the-field usage of your product. The XPower analysis tool uses the CXT and VCD files to estimate the power used by your application. XPower generates a tabular report of the power used, and it lists the resources and signal names of your design. Performing end-of-life battery tests will ensure your success.

Conclusion

Increasing design sizes and the emerging handheld market are a reality. The combination of the two makes lowest possible power consumption a critical factor in programmable design today. The introduction of XPower into the ISE suite of tools gives you the new capability to address these issues and decrease your time to market.

The XPower component is now being delivered with the Alliance and Foundation Series ISE 4.1i design tool suites. It is also included in the free WebPACK™ configuration. For more information on ISE 4.1i with XPower, visit the Xilinx Design Tools Center at *www.xilinx.com/ise/xcell/*.